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PATENT SPECIFICATION

(11) 1 553 697

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(21) Application No. 24518/76 (22) Filed 14 June 1976

(31) Convention Application No. 2531945

(32) Filed 17 July 1975

(31) Convention Application No. 2548762

(32) Filed 31 Oct. 1975 in

(33) Federal Republic of Germany (DE)

(44) Complete Specification published 3 Oct. 1979

(51) INT CL² H03K 13/02

(52) Index at acceptance

H3H 12D 13D 14B 23D 3C 3D 3G 6A 6B 6D 7B 7F 7G 7L 7X
8B 8E BC



(54) IMPROVEMENTS IN OR RELATING TO DIGITAL TO ANALOGUE CONVERTER ARRANGEMENTS

(71) We, LICENTIA PATENT-
VERWALTUNGS-GESELLSCHAFT MIT
BESCHRANKTER HAFTUNG, a
company organised under the laws of
Germany, of Theodor-Stern-Kai 1, 6
Frankfurt/Main 70, Germany do hereby
declare the invention, for which we pray
that a patent may be granted to us, and the
method by which it is to be performed, to be
particularly described in and by the
following statement:—

The present invention relates to a circuit
for generating a pulse sequence and also for
converting a pulse sequence into an
analogue voltage.

It is frequently desired in circuit
engineering to convert digital signals into
analogue signals. There has been typically a
trend in recent years for replacing analogue
circuits by digital circuits. In this context it
is necessary to return to analogue data at
interfaces to additional circuits which
cannot be designed as digital circuits. There
thus exists a need for digital-to-analogue
converters.

An example of this occurs in the case of
wireless receiving sets when previously
selected tunings for various transmitters are
stored in the form of binary numbers in a
memory (e.g. a semi-conductor memory)
and can be picked for tuning whence they
must be converted into a direct potential for
(variable) capacitance diodes which are
used for tuning the receiver set.

In a circuit published in the periodical
"Funk-Technik", 1975, issue 7, pp. 180 to 184
a direct potential is generated by the passing
of a square wave voltage generated by an
oscillator in the form of periodical pulses to
a low-pass filter or integrator. An electronic
switch is provided which, in rhythm with the
pulse repetition frequency, applies a battery
voltage through a resistance to the low pass
filter. The chronological mean value of the
pulses is filtered out as the result of the

integrating action of the low pass filter, and
the analogue value (i.e. the magnitude of the
direct voltage at the output of the low pass
filter) is proportional to the keying ratio.
The keying ratio, which is determined by
the quotient of the pulse duration to the
period, is thus appropriately chosen for
generating a desired value of the direct
current.

It has been found that this known circuit
is inadequate in many cases for reasons
which will be shown in the following. The
above-mentioned known digital-to-
analogue converter comprises an electronic
switch which connects a battery voltage U_b
through a resistance to an integrating
element in rhythm with the pulse repetition
frequency. If the break time of the switch is
called τ and the cycle time T , the direct
voltage U_i occurring at the output of the
integrating element is as follows:
 $U_i = U_b \cdot \tau/T$. An alternating voltage is
superimposed on the direct voltage U_i ; it
thus exhibits residual ripple. This residual
ripple has a frequency $f_r = 1/T$ corresponding
to the pulse repetition frequency. The time
constant of the integrating element must be
large compared with the pulse repetition
frequency when a small residual ripple is
wanted, i.e. the limiting frequency of the
low pass filter acting as integrating element
must be very much smaller than the pulse
repetition frequency. Since however the
pulse repetition frequency cannot be chosen
to be excessively large, the limiting
frequency must be relatively low so that the
low pass filter must be of relatively narrow
bandwidth. This has the result that in the
event of variations in the keying ratio τ/T , a
relatively long time elapses until the direct
output voltage U_i reaches its new stationary
value due to the relatively large time
constant of the narrow band, low pass filter.

A circuit for dealing with this problem has
been described in the German ALS 23-17 851.

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In this several pulses are generated which are distributed over a fixed cycle length. This known circuit includes a comparator into one input of which is fed the contents of an input counter and into another input is fed the output of a continuous forward connected reference counter. On comparison of equivalent counter settings of the two counters in the comparator a single pulse would be formed at the comparator output on each run of the counter. The width of this pulse would be a function of the contents of the input counter. The connecting leads from the reference counter to the comparator are mutually changed over with the aim of producing several pulses distributed over the period with a direct voltage mean value corresponding to the said single pulse.

According to the invention, there is provided a circuit for generating a pulse sequence in dependence upon a number M representing the mean d.c. value of the sequence within a predetermined range of values, comprising:

means for producing a plurality P of pulses distributed within a time period T related to the minimum duration $\Delta\tau$ of a said pulse and the number of steps, each associated with the minimum duration $\Delta\tau$, in the said range, the pulses having a basic duration which is determined by a first number N derived from the number M,

means for extending the basic duration of a said pulse by the minimum duration $\Delta\tau$, and means for controlling the extending means to extend those of the said pulses selected and distributed over the period T in dependence upon a second number R derived from the number M.

An embodiment of the invention provides an apparatus for generating an analogue voltage from a pulse sequence, comprising the said circuit for generating the pulse sequence, and integrating means for operating on the said pulse sequence to provide the said analogue voltage.

For a better understanding of the invention, reference will now be made by way of example, to the accompanying drawings, in which:—

Figures 1a and 1b are pulse diagrams illustrating the operation of a known circuit,

Figure 2 shows a known electronic switch with a low-pass filter,

Figure 3 is a diagram of a known circuit for the generation of pulses of variable width and for deriving therefrom an analogue voltage,

Figure 4 is an example of an embodiment of a circuit according to the invention, and

Figures 5—7 are diagrams illustrating the operation of the circuit of Figure 4.

In the following first will be described the known circuit with the aid of Figures 1a, 1b

and 2. Figure 1a shows a pulse train of cyclical pulses, the pulse width of each which is designated by τ . These single pulses which occur once each within the period T are fed in the known way through an electronic switch 1 and 2 (Figure 2) into a low pass filter 3—8. The area of the single pulse is proportional to the magnitude of the direct voltage U_1 produced at the output from the low pass filter. As is known this can be calculated by the following formula:

$$U_1 = \frac{\tau}{T} \cdot U_{\max}$$

in which $U_{\max}$ is the amplitude of the pulse, the magnitude of which amplitude here equals the voltage U_2 in Figure 2. Whilst the single pulses of Figure 1a generate a relatively small direct voltage U_1 , a larger direct voltage is generated on the basis of the pulses shown in Figure 1b due to the longer pulse duration τ at constant period. The pulse duration τ in Figure 1b differs from the pulse duration in Figure 1a by several time elements $\Delta\tau$, whereby $\Delta\tau$ is the smallest discrete time element for changing of the pulse width (drawn in hatched lines in Figure 1a). As mentioned previously, due to the response time of the low pass filter the new direct current value takes however a relatively long time to be produced when the pulse duration is changed from that in Figure 1a to that in Figure 1b.

When the direct voltage is intended for the tuning-voltage of television sets with (variable) capacitance diodes it has to be very accurate and must have a short response time of e.g. 0.2 sec. The tuning step width will for example be 40 kHz per 3 mV at a possible direct voltage range of 0 to 30 V and a tuning range of typically 400 MHz. The 40 kHz are derived from the fact that at the stipulated official standard the human eye needs a 40 kHz change until it is able to discern a change on the screen. At a minimum frequency variation of 40 kHz, a 400 MHz range is divided into 10,000 steps (400 MHz/40 kHz=10,000). A voltage step width of $\Delta U_1=3$ mV (30 V/10,000=3mV) is obtained when a voltage range between 0 and 30 V is subdivided into 10,000 steps. Accordingly 10,000 different direct voltage values have to be realised within the cycle time T.

In the example of embodiment of the invention described in the following with reference to Figure 4 this large number of direct voltage values is achieved at a pulse repetition frequency of 3.13 kHz constant over a wide range. Short response times can be achieved with simple filters at this pulse repetition frequency.

For a better understanding of the circuit

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shown in Figure 4 it is proposed to first explain the prior art type circuit per Figure 3 with which single pulses can be generated the pulse width of which is controllable. The pulse widths may be multiples of a time element $\Delta\tau$. These time elements are the pulse durations of a clock pulse generator 65 in Figure 3 which drives two counters 66 and 67. The counter 66 has a fixed ratio of 2^n and is clocked directly by the pulse generator 65 and defines a time period T. The counter 67 has a controllable division ratio. It is clocked through a controllable gate 70 by the pulse generator 65. Provision is made for the counter 67 to be only able to count up to a value M. This can be done by means of a reference (comparator) circuit which compares the contents of the counter 67 with the contents of a register containing the value M. It is however simpler to preset the counter 67 from a register 68, which contains the value $2^n - M$ in binary number form; this is shown in Figure 3.

After a number of clock pulses corresponding to the division ratio of the counter 66, an output pulse appears at the output of the counter 66. This is used to set the flip-flop 69 causing blockage of a transistor 1 (corresponding to transistor 1 of Figure 2). The counter 67 receives clock pulses through the gate 70, which is opened by the action of the output pulse, and counts M clock pulses starting from the value $2^n - M$ until it reaches the value 2^n and thereby resets the flip-flop. As a result the transistor 1 becomes conducting again after the period $\tau = M \cdot \Delta\tau$. The cycle time is $T = 2^n \cdot \Delta\tau$. The gate 70 is controlled from an output of the flip-flop 69 and is blocked from the moment of resetting of the flip-flop 69 until the end of the run of the counter 66.

The circuit described in conjunction with Figure 3 thus permits the generation of a single pulse of controllable length in each fixed time interval T which is preset by one run of the counter 66.

Figure 4 shows an example of a circuit in accordance with the invention. In addition to the previously described pulse ratio counter of Figure 3 made up from the circuit elements 66 to 69 the circuit of Figure 4 has a programmable frequency divider made up of circuit elements 72 to 75, and a pulse extension circuit 71. The pulse extension circuit 71 is located in the signal route from the output of the counter 67 to an input of the flip-flop 69. The pulse extension circuit 71 can be used for delaying the output pulse from the counter 67 by one time element $\Delta\tau$ so that the pulse at the output of the flip-flop is extended by one time element $\Delta\tau$. The programmable frequency divider 72 to 75 is clocked from the output of the counter 66 and controls

with its output the pulse extension circuit 71.

The following abbreviations will be used in the following:

M=is number representing the direct voltage to be generated; it may take any value between 0 and 2^n .

P=number of sub-time intervals per period T. One pulse is generated in every sub-time interval.

N=the whole number (without remainder,) obtained on division of M by P, written abbreviated: $[M/P]$; i.e. the largest whole number less than or equal to M/P .

R=the remainder accruing from the division of M by P. The period $T = (U_{\max} - U_{\min})$

$\Delta\tau$

$\Delta\mu_1$

where $(U_{\max} - U_{\min})$ is the tuning voltage range,

$\Delta\tau$ is the duration of one time element, $\Delta\mu_1$ is the minimum voltage step, associated with the duration $\Delta\tau$, in the tuning voltage range.

In the circuit per Figure 4 the period $T = 2^n \cdot \Delta\tau$ is subdivided into $P = 2^k$ sub-time intervals whereby each sub-time interval is $2^m \cdot \Delta\tau = 2^{n-k} \cdot \Delta\tau$ long. In the shown case in which $n=13$ the values $k=7$ and $m=6$ have been picked for the variables k and m . The period T is thereby subdivided into 128 sub-time intervals having each a duration of 64 time elements $\Delta\tau$. The pulse ratio counter 66 to 69 generates in each sub-time interval a pulse of the basic length N. $\Delta\tau$, whereby N equals $[M/P]$; typically $P=128$, $M=3517$, $[M/P]=27$, $R=61$. The remainder $R=61$ is added to the 128 pulses which have widths of 27 time elements $\Delta\tau$ each such, that of the 128 pulses 67 have widths of 27 time elements $\Delta\tau$ and 61 widths of 27+1 time elements. The 61 extended pulses are distributed as uniformly as possible over the 128 sub-time intervals, to ensure that no low frequency spectral components are produced by agglomeration of unequally long pulses which the filter is no longer capable of equalising.

The numbers M, N, P and R have so far been represented as decimal figures to make understanding easier. In the example they are binary coded numbers.

$$M = \underbrace{0110110111101}_{N} = 3517$$

The division of a binary number by a power of two $P=2^k$ is a simple point displacement by k places. The values N and R thus stand side by side in the number M. It is only

necessary to process them separately. This is done by means of the circuit shown in Figure 4. The first m higher value bits are used to control the pulse ratio counter 66 to 70 and the remaining k bits are used to control the programmable frequency divider 72 to 75. The first m bits are in this example first numbers derived from the binary coded number and the k remaining bits second numbers derived from the binary coded number.

Without the pulse extension circuit 71, the pulses have a basic length of $N \cdot \Delta\tau$ at the output of the flip-flop circuit 69. On activation of the pulse extension circuit 71 by the programmable frequency divider 72 to 75 acting as residue distributor the output pulse will be $N+1$ time elements long. The programmable frequency divider 72 to 75 is controlled by a k -bit counter 72. A gate array 74 activated with the remainder R stored in a register 75 fixes which transition from logic "0" to logic "1" of the stages of the counter 72 has to effect a pulse extension by a time element $\Delta\tau$. In this context the stage of the register 75 with the smallest valence controls that gate 74 which is applied to the stage of the divider 72 with the rarest transitions i.e. the highest valence. The sequence of the valences is changed over correspondingly also for the other gates.

The principle of the programmable frequency divider 72 to 75 can be used for binary coded numbers and any desired number of places. In integrated circuit engineering it is typically possible to employ as counter 72 a synchronous counter in which the transitions from logic "0" to logic "1" of one counter stage are selected with the aid of gates. Small extensions of these then permit the selection of transitions controlled by the register 75. The mode of working of the programmable frequency divider 72 to 75 will now be explained with the aid of Figures 5 and 6. To keep the diagrams simple only eight sub time intervals (t_p) are given the counter settings of which on the counter 72 are marked on top of the columns in Figure 6. It is thus necessary to imagine that the counter 72 and the register 75 consist of three binary stages. The lines are all assigned to the residual values R shown in the left hand column. The crossed squares show the place locations at which extended pulses are generated.

The example of Figure 5 shows pulses of basic length and the distributed extension time elements for the value $R = "1" "0" "0"$ (binary) = 4 (decimal).

It can be seen in Figure 6 that the stage of the register (75 in Figure 4) with the lowest valence (this stage contains the third place of R) determines whether the transition

from logic "0" to logic "1" of the third stage of the counter 72 (maximum valence, third place of t_p) is transmitted to the NOR gate 73. Similar applies for the stage with the next higher valence and the maximum valence. The largest non-uniformity in distribution which may occur amounts to one time element $\Delta\tau$ over the cycle duration T . It occurs with uneven number residue (remainder) R .

The function of the uniform distribution of the residual pulses can also be realised with one of the known programmable binary counters e.g. with the integrated circuit 7497. The modules 72, 73, 74 shown in Figure 4 may be replaced by the said programmable dual counter whereby the outputs from the register 75 are wired to the control inputs of the there installed counter and the output of the circuit are wired to the pulse extension circuit 71.

For an assessment of the voltage variations caused by the aforesaid maximum non-uniformity (1 time element $\Delta\tau$ per period T) at the output of the filter the pulse reply of the system for a pulse of length $\Delta\tau$ (76 in Figure 7) is imagined to be superimposed on the measured or calculated curve for the response to a voltage jump 77. Since the filter is capable of equalising pulses lasting $N \cdot \Delta\tau$ ($0 < N < 2^m$) up to the permissible residual rippling 78 the effect of this pulse response 76 and 77 remains below the value of a direct voltage step ($2 \cdot U$) and does therefore not interfere.

The known circuit of German ALS 23 17851 represents an improvement over the circuit disclosed in the periodical Funk-Technik mentioned hereinbefore, as far as ripple factor and transient response is concerned.

The known circuit is badly affected by temperature variations. The extent of the effect of temperature variations is to a considerable extent dependent upon the magnitude of the pulse repetition frequency. The pulse repetition frequency varies for different direct voltage values in this circuit and increases towards the mean direct voltage range linearly to a very large value corresponding to half of the cycle frequency at which the circuit is run. Temperature variations affect mainly the shape of the pulse flanks. As a result the temperature dependency increases proportionally with the pulse repetition frequency.

The exemplary circuit according to the invention attempts to provide a circuit the direct current generated in which has a low ripple factor, and or the circuit has a low transient response and/or is unaffected by temperature variations.

WHAT WE CLAIM IS:—

1. A circuit for generating a pulse sequence in dependence upon a number M representing the mean d.c. value of the sequence within a predetermined range of values, comprising:

means for producing a plurality P of pulses distributed within a time period T related to the minimum duration $\Delta\tau$ of a said pulse and the number of steps, each associated with the minimum duration $\Delta\tau$, in the said range, the pulses having a basic duration which is determined by a first number N derived from the number M,

means for extending the basic duration of a said pulse by the minimum duration $\Delta\tau$,

and means for controlling the extending means to extend those of the said pulses selected and distributed over the period T in dependence upon a second number R derived from the number M.

2. A circuit for generating a pulse sequence in dependence upon a number M representing the mean d-c value of the sequence within a predetermined range of values, comprising:

means for producing a plurality P of pulses distributed within a period T which has the magnitude.

$$T = (U_{\max} - U_{\min}) \cdot \frac{\Delta\tau}{\Delta\mu_1}$$

where $(U_{\max} - U_{\min})$ is the predetermined range,

$\Delta\tau$ is the minimum duration of a said produced pulse, and $\Delta\mu_1$ is the minimum step in the range, associated with the minimum pulse duration $\Delta\tau$, the P pulses each having a basic duration dependent on a first number N which is the largest whole number less than or equal to, (M/P) ,

means for extending the basic duration of selected ones of the P pulses by the minimum duration $\Delta\tau$, and

means for causing the extending means to extend the duration of pulses selected and distributed over the period T in dependence upon a selected number R where $R = M - N \cdot P$.

3. A circuit according to Claim 1 or 2, wherein the P pulses are uniformly distributed over the period T.

4. A circuit according to Claim 1, 2 or 3, wherein P is a constant.

5. A circuit according to Claim 1, 2, 3 or 4, wherein the P pulses have constant amplitude.

6. A circuit according to Claim 2, or to Claim 3, 4 or 5 when appended to Claim 2,

wherein: the producing means comprises a first digital store for storing m binary digits representing the first number N and means responsive to these m binary digits to produce the said P pulses; the controlling means comprises a second digital store for storing k binary digits representing the second number R and means responsive to those k binary digits to control the extending means; and $P = 2^k$, $T = 2^{m+k}$, the said m digits are the m digits of higher valence of the number M in binary coded decimal form and the said k digits are the remaining k digits of lower valence of the number M in binary coded decimal form.

7. A circuit according to Claim 6 wherein the means responsive to the said m binary digits includes:

a clock for producing clock pulses of duration $\Delta\tau$,

a first frequency divider having a fixed division ratio of $2^m:1$ coupled to receive the clock pulses for determining the distribution of the P pulses over the period T,

a second frequency divider having a division ratio controllable by the said k binary digits and coupled to receive the clock pulses for determining the basic durations of the P pulses, and

a bistable circuit having a first input coupled to the output of the first divider and a second input coupled to the output of the second divider via the extending means, to produce the P pulses.

8. A circuit according to Claim 6 or 7, wherein the controlling means includes:

a k -bit counter coupled to the output of the first frequency divider and arranged to count the P pulses; and an array of gating means responsive to predetermined relationships mixed between the count of the said counter and the k binary digits stored in the second digital store to cause the extending means to extend the basic duration of selected ones of the P pulses.

9. An apparatus for generating an analogue voltage from a pulse sequence, comprising a circuit according to any preceding claim for generating the pulse sequence, an integrating means for operating the said pulse sequence to provide the said analogue voltage.

10. Apparatus for generating an analogue voltage from a pulse sequence substantially as hereinbefore described with reference to Figures 4 to 7 of the accompanying drawings.

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