22 SEP 2003

A NOVEL SPACER TECHNOLOGY FOR MAKING LIQUID-CRYSTAL-ON-SILICON DISPLAYS WITH ALIGNMENT POSTS

BACKGROUND OF THE INVENTION

(1) Field of the Invention

This invention relates to new method of photolithographic fabrication of alignment posts directly on liquid-crystal-on-silicon displays.

(2) Description of the Prior Art

The picture quality of liquid crystal displays from the simple seven segments to millions of pixels is determined by the structure used to control the variation of thickness and position leads after wafer processing. There are known processes for creating insulated alignment posts based on preformed glass microspheres or cylinders or rods; relatively low series resistance posts can be obtained by means of selective deposition of polysilicon and metallic

silicide. (The making of metallic vias and contacts is a comparatively well known processing art.)

US Patent 5,498,925 to Bell et al describes the formation of posts in flat panel displays using processes based on a heat-treated slurry or paste upon a glass plate. US Patent 5,597,736 teaches the function of a light-blocking layer deposited upon a semiconductor substrate material that can emit light. US Patent 5,744,824 and US 5,748,828 show various LCD structures and external optics.

Until now, it has been difficult to construct alignment posts using photolithography onto a semiconductor substrate material used to control the gray-level of each pixel. The thickness of the liquid crystal is limited to the available preformed spacer sizes supplied by the manufacturers of such preforms.

BRIEF SUMMARY OF THE INVENTION

A principal object of the present invention is to describe two novel methods for building a flat-panel liquid-crystal display upon an integrated circuit (IC) die. There is a controlled inter-relationship between the height of the alignment posts supporting the overlaying glass cover plate

and the image quality viewed from the liquid-crystal-on-silicon display devices.

Another object of this invention is to describe effective and very manufacturable methods of photolithographic formation of insulating spacers or alignment posts (also called studs or pillars). These methods can be used in processing many different device types, and are described in this application for liquid crystal display devices as a way of illustrating their embodiment at a pixel density beyond that achievable with preformed micro-glass spheres and rods.

A further object of the present invention is to describe two methods of deposition for the alignment posts that retain their desired structure during deposition of subsequent features. The process methods are classified into two method categories: 1) patterned insulating material; 2) alignment posts formed in the peripheral sealant of the top glass cover over liquid-crystal-on-silicon display devices.

1. NO DISCONTINUITIES NEAR THE SPACERS DUE TO THERMAL FLUCTUATIONS, HENCE CONTINUOUS LIQUID FILMS.
2. PREVENTION OF SEAL RING BREAKAGE AND SUBSEQUENT LEAKAGE OF THE LIQUID CRYSTAL.

Two new methods for the formation of an improved liquid-crystal-on-silicon display are described, in which the device structure is enhanced by the photolithographic building of alignment posts in the presence of the mirror pixels of the microdisplay. These two methods are:

1. Photolithographic Alignment Posts Formed in Active Area - wherein a photolithographic method forms patterned oxide spacers or alignment posts in the active area of the device structures.

2. Photolithographic Alignment Posts Formed in Peripheral Sealant - wherein said alignment posts are deposited by the photolithographic process in the area of the ring sealant/glue for the glass top cover.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings becoming a material part of this description, there is shown:

Figs. 1 through 3 schematically illustrate in cross-sectional representation a preferred embodiment of the device structure of the present invention. The base silicon substrate with the formed metallic pixels on the display device is shown in Fig. 4.

The process flow for making the alignment posts by the two process methods is shown in Figs. 5 to 9.

Fig. 5 shows the structure of the liquid-crystal-on-silicon display device with sprayed SiO2 particles used as spacers or alignment posts, which illustrates the prior art used before the invention of the two novel methods described herein.

Fig. 6 shows the metallic pixels passivated with layers of silicon nitride and USG and the insulation material, such as SiO2 and Si3N4, located there over.

Fig. 7 shows the structure of the liquid-crystal-on-silicon display device with photolithographic alignments posts used as spacers.

Fig. 8 shows the top view of the structure of the liquid-crystal-on-silicon display device with the spacers or alignment posts located in the ring sealant.

Fig. 9 shows a cross-sectional view of the same structure illustrated in Fig. 8.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

22 SEP 2003

Referring now more particularly to Fig. 1, here is shown a portion of a partially completed integrated circuit liquid-crystal display. The glass cover plate 10 provides the transparent enclosure for the external incident light to be reflected back to an observer. The strength of reflected light is dependent on the light polarization, absorption and light scattering properties of each liquid-crystal display pixel, which is controlled by the electrical field established within the liquid crystal material 11. The IC die 12, separated from the glass plate 10 by the alignment posts 14 generates these E-fields. The resultant space or thickness gap between the glass plate 10 and the silicon wafer 12 is filled with the chosen liquid crystal material 11. Incident light, either provided or ambient, enters the open face of the liquid-crystal-on silicon and is reflected from the underlying pixels to form a viewable pattern of polarized light, i.e. the image is viewed directly or projected through an optical polarized system.

Fig.2 illustrates the bonding pads 20 on the IC die to which the external wires 22 are attached. The silicon wafer contains the embedded control circuits that activate the pixel patterns in the viewable area 24. The refractive index anisotropy of the liquid crystal is influenced by the electric fields above the IC surface. A small change in voltage makes a large change in the optical transmission.

Because this invention teaches the photolithographic making of patterns of alignment posts, the ratio of pixels 30 to posts 14 is often fabricated in the range 0.25 to 0.125. As shown in Fig. 3, the photolithographic method permits these alignment posts to be constructed in the space between adjacent pixels.

The base silicon substrate with the formed metallic pixels on the display device is shown in Fig. 4. A typical LCD microdisplay contains metallic pixels (measured 19 by 19 microns) with 0.7 microns thickness gap to the glass top cover, and a total pixel array count of 1024 by 768. The distance between the pixels when measured in the top view of the LCD display can be about one micron.

The process steps for making the alignment posts by means of the various photolithographic categories is shown in Figures 5 to 9.

Starting with Fig. 5, the conductive metallic (or polysilicon) layer 30 is formed over the silicon oxide 40, which is formed on top of the first metal layer 41 on the IC. Prior to formation of the silicon oxide 40, the metal 20 as bond pad is deposited and connected to metal layer 41 with a barrier/glue layer 26 composed of Ti/TiN. On top of the metal 20 is a tungsten plug 21, placed there by the method of CVD. Another barrier/glue layer 23 made of Ti/TiN

is formed on top of metal 20 and another barrier/glue layer 28 made of Ti/TiN on top of the silicon oxide 40. For all three layers (23, 26 and 28), the process of PVD is used to deposit these barrier/glue layers of thickness about one micron. A silicon semiconductor substrate 15 has active devices therein and an insulating layer 16 upon which metal layer 41 is formed.

Then a photoresist layer is deposited over the metal 30 to construct the pixels. The photoresist is exposed and a portion of the metallic layer 30 is removed so that each pixel retains a metallic surface, which shall act as a mirror reflector for the light incident upon the pixel. (The unprotected barrier/glue layer 28 is also removed in this process step.) In both these novel methods, the metallic pixels 30 are not coated with either an anti-reflective coating ARC or an optical interference filter OIL.

After the photoresist is stripped, as shown in Fig. 5, the device is prepared for subsequent deposition of the insulation material from which the spacers, also called alignment posts, will be patterned. (The purpose of this passivation preparation is the protection of the existing metallic pixels 30 from any corrosion or damage from the liquid crystal material.) At this point in the novel method, two protective layers of passivation are formed.

1) An optically transparent coating of undoped silicon glass USG 65 of the thickness between about 1000 and 2000 Angstroms is formed over the metallic pixels 30 and the silicon oxide 40 by the process of CVD.
2) An optically transparent coating of silicon nitride 66 of thickness between about 2500 and 10000 Angstroms is formed over the layer USG 65 by the process of CVD. (Careful attention is required in constructing these optical transparent layers so as not to disturb any underlying device structures.)

In one form of prior art, the spacers between these optical transparent protective layers and the glass top cover have been fabricated by spraying SiO2 glass particles 55. A process step of particle spray cannot be well controlled in terms of the size of the resultant particles, i.e. clusters of particles 56 can form and cause a defective deviation in the film thickness of the liquid crystal, as illustrated in Fig. 5.

Fig. 6 shows the insulation material 60 deposited onto the silicon nitride protective layer 66 of thickness between about two and three microns by the process of high-density plasma oxide (HDP) undoped or HDP FSG-doped oxide, which is then followed by a 1.2 micron plasma-enhanced tetraethyl orthosilicate (PETEOS) glass film.

This film of insulating material is then smoothed using chemical-mechanical polish CMP for two purposes: 1) to attain the desired height of the gap between the metallic pixels and the lower surface of the glass top cover; 2) to planarize the surface by making the whole surface flat. The thickness gap now becomes a design parameter for the liquid-crystal-on-silicon display device, and any topographic non-uniformity in gap thickness has been eliminated by CMP. The resultant structure is now ready for the photolithographic fabrication of the alignment posts.

The alignment posts are constructed from the insulation material layer by the following methods described herein:

Method 1 - Photolithographic Alignment Posts Formed in Active Area

A photomask, not shown, is formed on top of the layer of insulating material 60. The photomask protects the insulation material when the insulating material 60 is removed by a dry or wet etch process. The photomask, about 4 microns across at the location of each alignment post, is resistant to the removal process, resulting in the formation of the spacers or alignment posts. After the formation of these spacers or alignment posts, the remaining photoresist

is removed by the conventional developer method. The resultant alignment posts 71 are shown in Fig. 7.

For the final step, a film of liquid crystal placed on the silicon nitride protective layer and the top glass cover placed down. The spacers (alignment posts) hold the glass plate to a uniform thickness of the liquid crystal film above the metallic pixels, as shown in Fig. 7.

Method 2 - Photolithographic Alignment Posts Formed in Peripheral Sealant

In this method the spacers (alignment posts) 72 are located in the peripheral area of the liquid-crystal-on-silicon display device. In particular this novel method locates the spacers in the adhesive sealant 81 of the glass top cover. Adhesive sealants glue the top cover to the silicon substrate 12. There are many types of seal ring adhesive/glue, including thermosetting epoxy resin, which can be chosen for this novel method. The liquid crystal film material is inserted through the orifice in the right hand side of Fig. 8 after this seal ring adhesive is mate pressed and cured. A cross-sectional view, taken at position 79, of one display-device-design example is illustrated in Fig. 9.

The device design layout for the photolithography described in this method may include spacers within the active area (in addition to the spacers formed in the location planned for the ring sealant). The actual design choice depends upon the dimensions of the active area 76 inside the ring 81, and the stiffness plus weight of the glass top cover 10,

For the two methods of photolithographic formation of alignment posts on LCD-on-silicon display devices, the existence of numerous alignment posts permits the usage of an ultra-thin glass plate or cover over the liquid crystal material. This implementation results in lightweight displays for portable applications. Glass covers supported by alignment posts are typically 0.5 millimeters in thickness, and can range between about 0.1 millimeters to 2 millimeters.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

22 SEP 2003

Claims

1. A method of forming insulating material alignment posts over active device structures comprising:

providing a silicon semiconductor wafer, said silicon semiconductor wafer having been provided with active semiconductor devices in or on its surface, further having been provided with conductive posts in a layer of dielectric that align with said patterned active devices, said semiconductor wafer further having been provided with patterned metallic layers that align with and symmetrically extend over a measurable distance in a plane that is parallel with the surface of said substrate whereby said metallic layers are optionally provided with a barrier layer interposed between said posts and said metallic layers; and

forming said insulating material alignment posts in a polished layer of insulating material by creating a photolithographic pattern over said pattern of active device structures.

2. A method according to Claim 1 wherein said photolithographic alignment posts improve the thickness uniformity of a liquid crystal film.

3. The method of claim 1 wherein said alignment posts are composed of the materials: HDP oxide, PETEOS, FSG Doped PETEOS and Sillyoxide.

4. The method according to Claim 1 wherein said alignment posts are of height between about 1 micron and 10 microns, wherein furthermore a cross section of said alignment posts is a design parameter that is applied for the creation of liquid-crystal-on-silicon micro-displays, said cross section extending over the surface of said semiconductor wafer over a measurable distance.

5. The method according placed on to Claim 1 wherein a said alignment posts are placed on a passivation layer deposited over metallic pixels on said silicon wafer.

6. The method according to Claim 1, in addition building alignment posts over a periphery of an active area in a vicinity of a ring sealant.

7. A method of forming insulating materials alignment posts over active device regions in or on the surface of a silicon body comprising:
providing a silicon semiconductor wafer having a pattern of active device structures therein and thereon;
depositing a layer of insulation over the surface of said wafer;
forming a first metallic layer over the surface of said layer of insulation;
forming a silicon-oxide insulating layer over the surface of said first metallic layer;
forming conductive plugs in said silicon-oxide insulation layer that align with planned pixel locations of a liquid-crystal-on-silicon display device, said conductive plugs comprising a conductive pedestal of conductive material overlaying and in electrical contact with said first metallic layer of under and over which a barrier or seed layer has been

created, said conductive plug further comprising a pedestal extension that overlays and aligns with said pedestal and has a cross section in a plane that is parallel with the surface of said wafer that is smaller that a cross section of said pedestal by a measurable amount, the plane of the surface of said pedestal extension coinciding with the plane of the surface of said silicon-oxide insulation layer;

forming a second metallic layer over the said silicon-oxide insulation layer;

forming a photoresist mask over said second metallic layer having a covering over planned pixel locations of a liquid-crystal-on-silicon display device;

removing said second metallic layer not covered by said photoresist mask, creating a patterned second metallic layer having a surface, leaving said second metallic layer in place in regions surrounding and aligned with said surface of said conductive pedestal extension;

removing said photoresist mask to provide that each said planned pixel retains said second metallic layer having a surface over planned pixel locations of a liquid-crystal-on-silicon display device, which shall act as a mirror reflector for the light incident upon

said liquid-crystal-on-silicon display device,

partially exposing the surface of said layer of silicon-oxide insulation;

depositing a first layer of passivation over the surface of said patterned second metallic layer and said partially exposed surface of said layer of silicon-oxide insulation over which a second layer of passivation is deposited;

depositing a thick layer of insulation over the surface of the second layer of passivation;

planarizing the surface of said deposited layer of insulation using methods of Chemical Mechanical Polishing;

patterning and etching said thick layer of insulation leaving said layer of insulation in place where planned alignment posts locations of a liquid-crystal-on-silicon display device are located, creating openings in said thick layer of insulation;

filling said openings created in said thick layer of insulation with a layer of liquid crystal material; and

depositing a glass cover plate having a lower surface over the surface of said liquid crystal in which alignment posts have been provided.

22 SEP 2003

8. The method of claim 7 wherein said thick layer of insulation in which said alignment posts are created are deposited by chemical vapor deposition.

9. The method of claim 8 wherein said thick layer of insulation comprises a silicon dioxide layer with a thickness of about one micron to achieve the desired height of the alignment posts.

10. The method of claim 7, additional alignment posts being created by a photolithographic process, said additional alignment posts being located in a ring sealant/glue area of said device structure provided for a glass top cover, said additional alignment posts being in addition to said alignment posts over active device regions of a silicon body.

11. The method of Claim 10 with the addition of reducing by methods of chemical mechanical polish (CMP) the thickness of the insulation material layer to a controlled thickness between about one and ten microns in the area of the ring sealant.

12. The method of Claim 10 whereby a uniform thickness gap is created between the surface of the second layer of metal, which function as metallic pixels, to the lower surface of the glass top cover.

13. The method of Claim 10, wherein said patterning and etching said thick layer of insulation being adjusted such that a distance between said openings and a cross section of said openings created in said thick layer of insulation are design parameters that are applied for creation of liquid-crystal-on-silicon micro-displays, said cross section extending over the surface of said silicon semiconductor wafer over a measurable distance.

14. The method of claim 10 whereby said patterning and etching said thick layer of insulation uses a photoresist mask over said thick insulation material in a vicinity of a ring sealant of a glass top cover for a location of each planned alignment post.

15. The method of claim 10 wherein said patterning and etching said insulation material is performed by etching to form the said alignment posts.

16. Alignment posts for a device structure that combines insulating materials for alignment posts associated with an active device structure in a silicon body comprised of:

a silicon semiconductor wafer having a pattern of active device structures therein and thereon;

metallic pixels on said semiconductor wafer;

bonding pads on said silicon body having wires attached whereby said wires are connected to external contacts through which control logic and power is supplied;

alignment posts having been made by means of photolithography rather than pre-formed glass beads or rods;

liquid crystal material located in the valleys below the surface of the alignment posts;

glass top cover placed upon and supported by the alignment posts to encapsulate said liquid crystal material while not encapsulating the area outside the liquid- crystal material, further not encapsulating the

area outside the liquid crystal material where bonding pads are located.

17. A device structure according to Claim 16 that combines the insulating material for the alignment posts combines with passivation layer above the active device silicon body structure in a silicon body.

18. A device structure according to Claim 16 that combines the insulating material for the alignment posts with a sealant ring for the glass top cover.