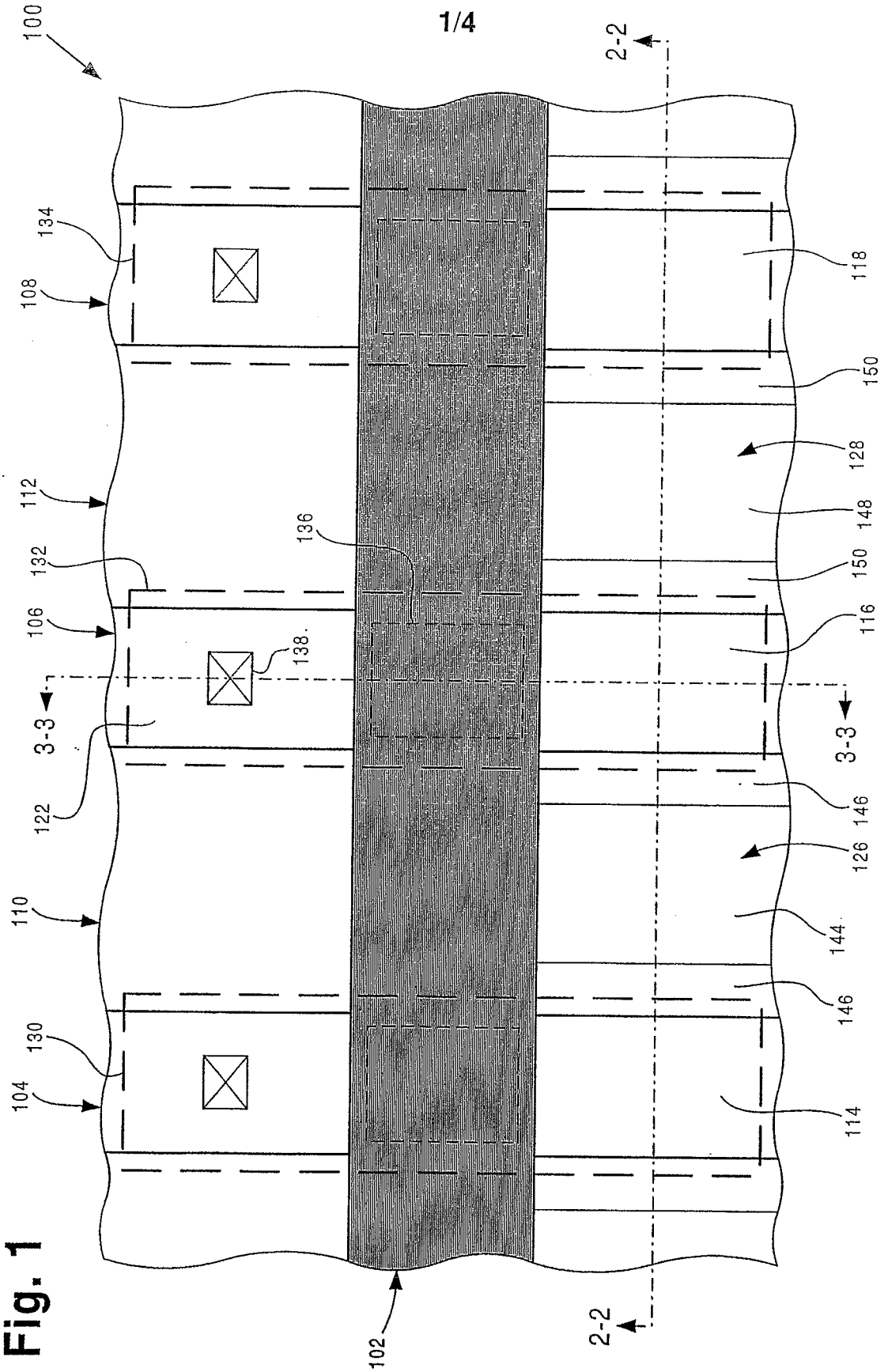

100
2-2
134
108
118
150
128
112
148
136
132
150
106
116
138
3-3
3-3
122
146
126
110
144
146
130
104
114
102
2-2

Fig. 1

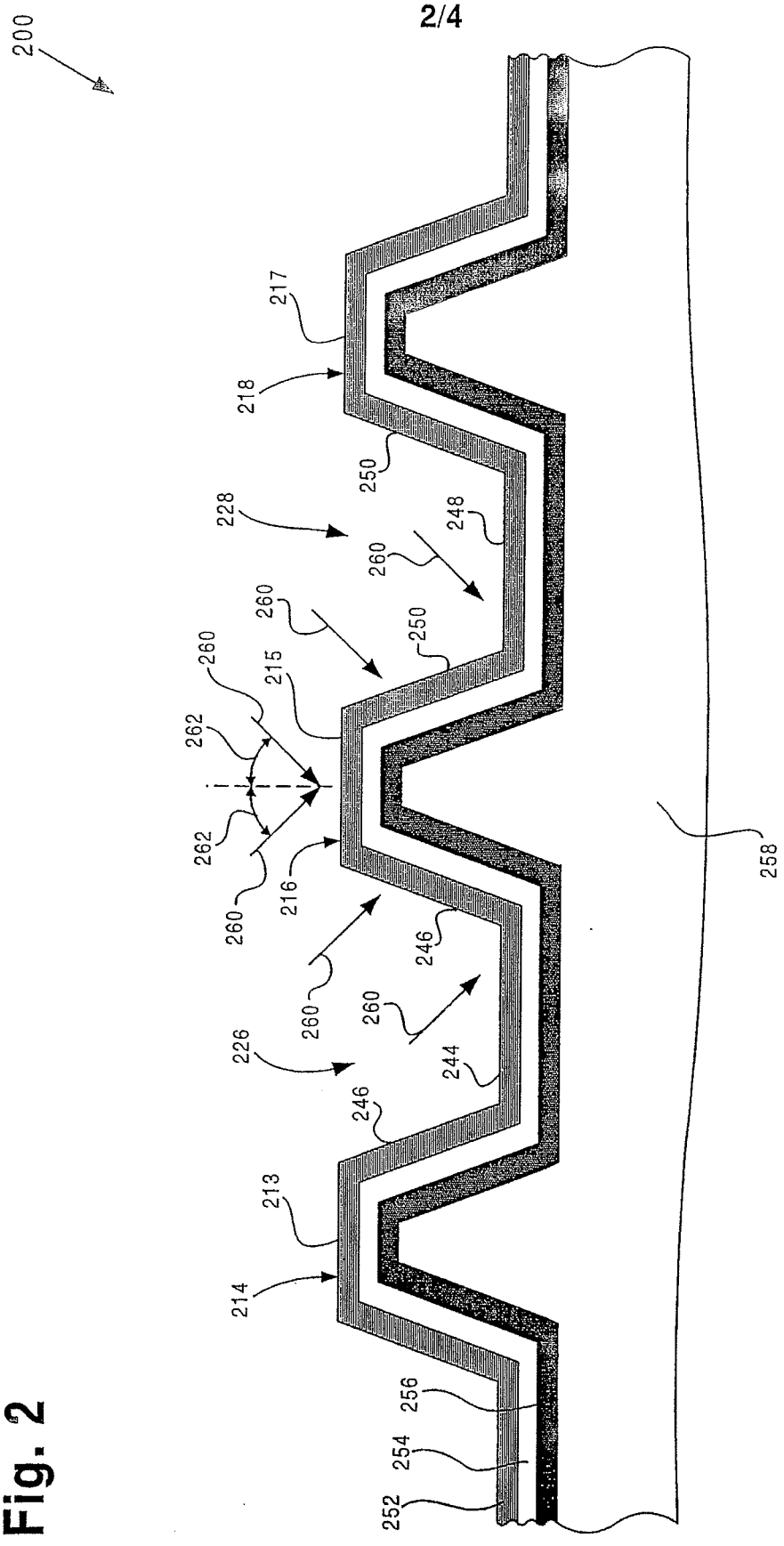

200
217
218
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228
248
260
260
250
260
215
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262
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244
246
213
214
256
254
252
258

Fig. 2

Fig. 3

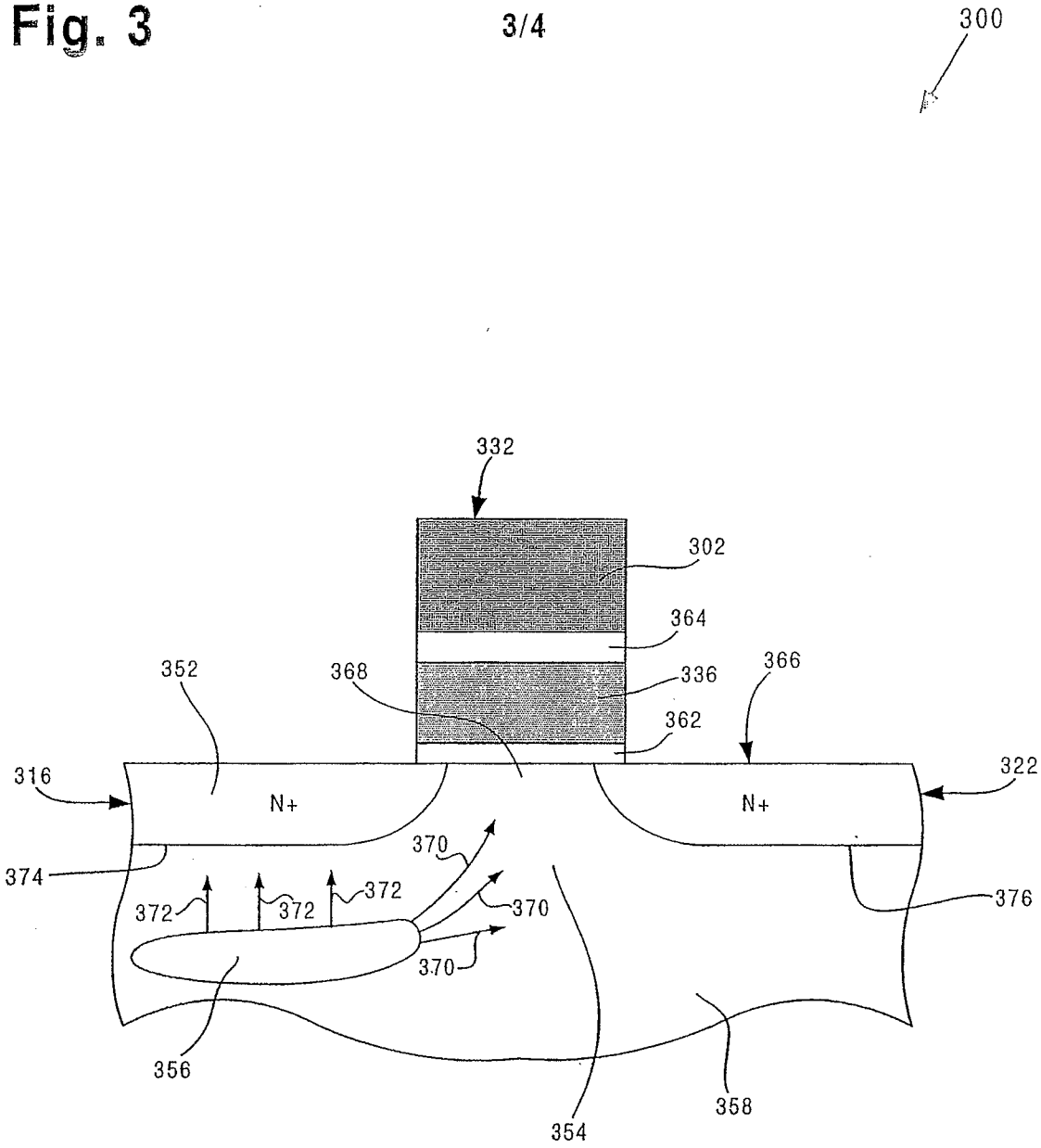
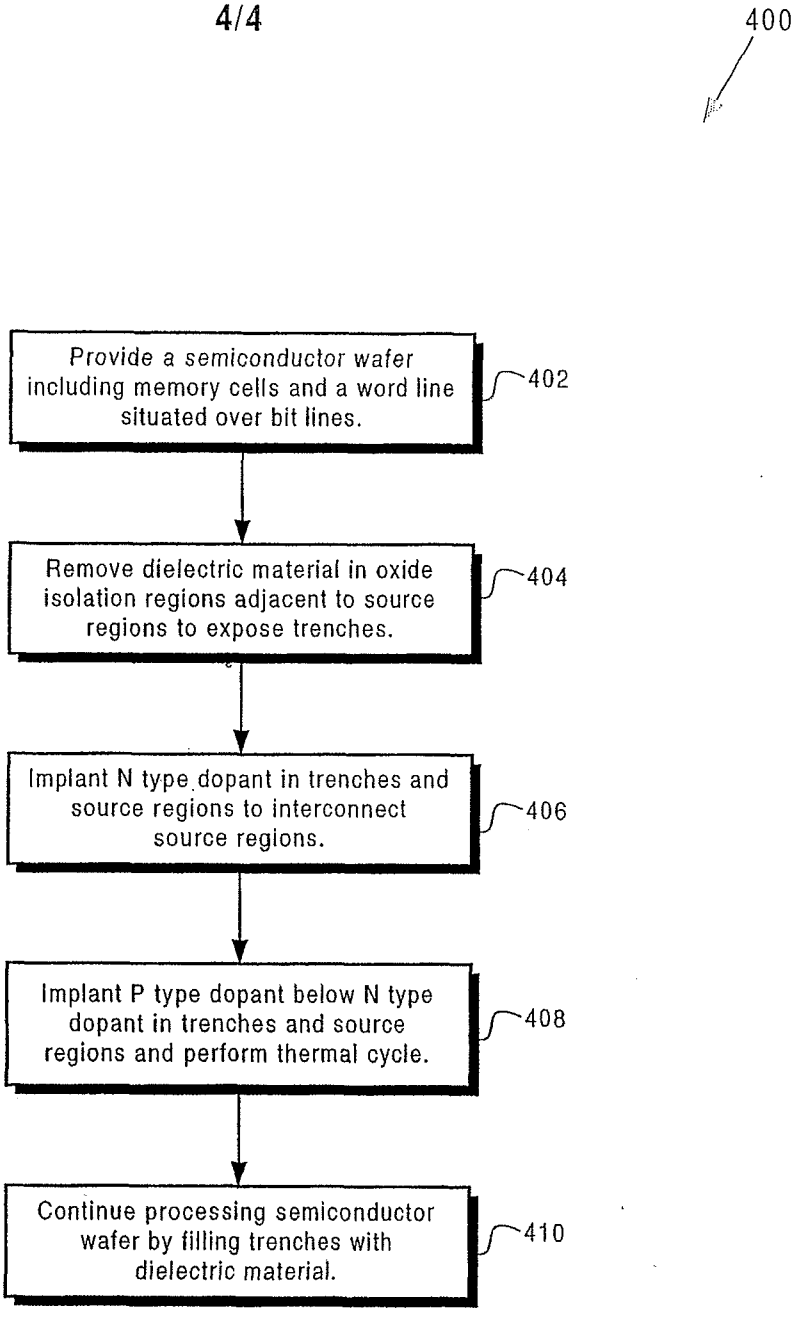

300
332
302
364
352
368
336
366
362
316
322
N+
N+
370
374
372
372
372
370
370
376
356
354
358

Fig. 4


400
Provide a semiconductor wafer including memory cells and a word line situated over bit lines.
402
Remove dielectric material in oxide isolation regions adjacent to source regions to expose trenches.
404
Implant N type dopant in trenches and source regions to interconnect source regions.
406
Implant P type dopant below N type dopant in trenches and source regions and perform thermal cycle.
408
Continue processing semiconductor wafer by filling trenches with dielectric material.
410