METAL GATE ELECTRODE USING SILICIDATION AND METHOD OF FORMATION THEREOF

BACKGROUND OF THE INVENTION

Technical Field

This invention relates generally to semiconductor technology, and more particularly, to semiconductor devices which incorporate a silicidation process.

Background Art

A common trend in modern integrated circuit manufacture is to produce transistors having feature sizes as small as possible. To achieve a high density integrated circuit, features such as the conductors, source and drain junctions, and interconnections to the junctions must be made as smallest possible. As feature sizes decrease, the sizes of the resulting transistors as well as the interconnections between transistors also decrease. Having smaller transistors allows more transistors to be placed on a single monolithic substrate. Accordingly, relatively large circuits can be incorporated on a single and relatively small die area. Furthermore, smaller transistors typically have lower turn on threshold voltages and faster switching speeds and consume less power in their operation. These features, in combination, allow for higher speed integrated circuits.

As semiconductor transistors are scaled to reduce their dimensions, a number of problems have been presented. For example, use of a very thin gate dielectric causes high gate current leakage, which diminishes device performance. Furthermore, as a transistor is scaled, a higher doping level is needed in the channel to reduce short channel effect, in order to ensure that the transistor properly turns off. This very high concentration of dopant in the channel decreases current drive and can lead to undesirable drain-to-channel tunneling current.

Furthermore, use of polysilicon gate technology, as is typical, carries with it additional problems. For example, polysilicon gates tend to suffer from polysilicon depletion or boron penetration effects, causing degradation in performance.

Additionally, a polysilicon gate has a fixed work function defined by a certain high level of doping of a particular specie or kind. For example, in a typical process, in an N type transistor wherein the gate, source and drain are doped with arsenic to a chosen (high) concentration, the resulting work function would be approximately 4.1 eV, while in a P type transistor, wherein the gate, source and drain are doped with boron to a chosen (high) concentration, the resulting work function would be approximately 5.0 eV. While such values are acceptable for typical devices, as such devices are scaled as described above, increasing the work function value to an extent in an N type device, and decreasing the work function value to an extent in a P type device, would allow a reduced level of doping concentration in the channel for the same threshold voltage, overcoming the problems associated with a high dopant level in the channel described above.

The use of metal in place of polysilicon as the gate of a transistor provides many advantages. For example, a typical such metal has a higher conductivity than polysilicon. Furthermore, there is the opportunity to choose a metal so that its particular work function is suited to the device, allowing reduction in the level of doping concentration in the channel. Additionally, the problems of polysilicon depletion and

boron penetration are avoided, allowing one to use a thicker gate oxide with a metal gate, substantially reducing gate current leakage. However, proposed processes typically involve deposition of metal instead of polysilicon, requiring complex process integration schemes.

Therefore, a process and a device which overcome the above problems are needed.

DISCLOSURE OF THE INVENTION

In the present method, a semiconductor structure is fabricated by providing a substrate, and providing a dielectric on the substrate. A polysilicon body is provided on the dielectric, and a metal layer is provided on the polysilicon body. A silicidation process is undertaken to silicidize substantially the entire polysilicon body to form a gate on the dielectric. In an alternative process, a cap layer is provided on the polysilicon body, which cap layer is removed prior to the silicidation process. The polysilicon body is doped with a chosen specie prior to the silicidation process, which dopant is driven during the silicidation process toward the dielectric to form a gate portion having a high concentration thereof adjacent the dielectric, the type and concentration of this specie being instrumental in determining the work function of the formed gate.

The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings. As will become readily apparent to those skilled in the art from the following description, there are shown and described embodiments of this invention simply by way of the illustration of the best mode to carry out the invention. As will be realized, the invention is capable of other embodiments and its several details are capable of modifications and various obvious aspects, all without departing from the scope of the invention. Accordingly, the drawings and detailed description will be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as said preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figures 1-6 illustrate process steps in a first embodiment of the invention; and

Figures 7-14 illustrate process steps in a second embodiment of the invention.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

Reference is now made in detail to specific embodiments of the present invention which illustrate the best mode presently contemplated by the inventors for practicing the invention.

Figure 1 illustrates a semiconductor device 30 including a silicon substrate 32 having formed thereon a dielectric in the form of a gate oxide 34, which in turn has thereon a polysilicon body 36, as is well known. An ion implantation 38 is undertaken (Figure 2), using for example arsenic for an N type device, or boron for

a P type device, so that ions 39 are implanted in the silicon substrate 32 (using the polysilicon body 36 and the oxide 34 as an overall mask 41) to form lightly doped regions 40, 42 in the substrate 32, and in the polysilicon body 36. For an N type device, the dopant specie arsenic may be implanted at an energy level of for example 3keV and a dosage level of for example $1e15cm^{-2}$, while for a P type device, the dopant specie boron may be implanted at an energy level of for example 4keV and a dosage level of for example $2.5e14cm^{-2}$. Thereafter, an oxide layer 44 is deposited over the resulting structure (Figure 3), which oxide layer 44 is anisotropically etched to form spacers 46, 48 on the sides of the polysilicon body 36 (Figure 4).

With further reference to Figure 4, another ion implantation step 50 is undertaken, again for example using arsenic for an N type device, or boron for a P type device, so that ions 39 are implanted in the silicon substrate 32 to form heavily doped regions 52, 54 (using the polysilicon body 36, gate oxide 34, and spacers 46, 48 as an overall mask 51), and in the polysilicon body. For an N type device, arsenic may be implanted at an energy level of for example 30keV and a dosage level of for example $4e15cm^{-2}$, while for a P type device, boron may be implanted at an energy level of for example 3.5keV and a dosage level of for example $2e15cm^{-2}$.

Subsequent to formation of these implants, active annealing (such as rapid thermal anneal) is undertaken at a temperature of for example 1050° C for 30 seconds to activate the implants to form the source and drain regions 56, 58 of the device 30.

Next, with reference to Figure 5, a metal layer 60, for example, nickel, is deposited over the resulting structure, i.e., over the polysilicon body 36, the spacers 46, 48, and the substrate 32 over the source and drain regions 56, 58. Then, the resulting structure undergoes a rapid thermal anneal at a temperature of for example 500° C, causing the nickel 60 to react with the silicon of the substrate 32 and the polysilicon body 36 to grow nickel silicide 62, 64, 66 into the polysilicon body 36 and into the source and drain regions 56, 58. The nickel layer 60 is thick enough in relation to the thickness of the polysilicon body 36, and the silicidation step is undertaken long enough, to provide that substantially the entire polysilicon body 36 is silicidized (since in this process the polysilicon 36 is consumed at approximately twice the rate of the nickel 60, the thickness of the nickel layer 60 is chosen to be more than one-half that of the thickness of the polysilicon body 36. For example, for a polysilicon body 36 thickness of 700 angstroms, a nickel layer 60 more than 350 angstroms in thickness is with advantage chosen). This process step forms nickel silicide gate 62 and nickel silicide regions 64, 66 in the source 56 and drain 58. The unreacted nickel portions are then removed, leaving the structure shown in Figure 6.

It will be seen that through complete consumption of the polysilicon body 36 during the silicidation step, a metal gate 62 is formed. Thus, the problems described above with regard to a polysilicon gate are overcome. That is, conductivity of the gate is improved as compared to a polysilicon gate, and the problems of polysilicon depletion and boron penetration are avoided.

During the silicidation process, the dopant specie 39 in the polysilicon body 36 (arsenic in the case of an N type device and boron in the case of a P type device in the above example), previously substantially evenly distributed within the polysilicon body 36, is driven downward by the downwardly advancing interface of nickel silicide and polysilicon until a substantial amount of the dopant specie 39 is in a portion 68 of the gate 62 adjacent the gate oxide 34, so that the portion 68 of the gate 62 adjacent the gate oxide 34 contains a substantially higher dopant concentration than the gate portion 70 further away from the gate oxide 34. The

"snowplowing" of the dopant specie 39 as described above causes an unexpected resulting gate work function. For example, in the case of an N type device where the dopant specie 39 is arsenic, with process steps taken as described above, the resulting work function of the gate 62 has been found to be 4.35 - 4.4 eV, as compared to the work function 4.15 eV of a polysilicon gate. This increase in work function in an N type device allows a reduced level of dopant concentration in the device channel for the same device threshold voltage. With such a reduced level of dopant concentration in the channel, it can be ensured that proper transistor turn off will be provided, meanwhile avoiding the problems of decreased current drive and undesirable drain-to-channel tunneling current, all as described above.

Likewise, in the case of a P type device where the dopant specie 39 is boron, with process steps undertaken as described above, the resulting work function of the gate 62 has been found to be 4.9 eV, as compared to the work function 5.05 eV of a polysilicon gate. This decrease in work function in a P type device allows a reduced level of dopant concentration in the device channel for the same device threshold voltage, overcoming the problems described above.

By practicing this process, it will be understood that various work functions of the resulting gate can be selected as needed, depending on for example the dopant specie type, the dopant specie concentration (or indeed the lack of doping specie), the type of metal layer, and/or the silicidation process steps. By appropriate selection of these parameters, the work function of the resulting gate can be tailored to specific needs.

Figures 7-14 illustrate a second embodiment of the invention. Figure 7 shows a device 80 including a silicon substrate 82, a dielectric in the form of an oxide layer 84 thereover, and a polysilicon layer 86 (substantially thinner than that in the process of Figure 1-6) formed over the oxide layer 84. The polysilicon layer 86 is implanted (88) with a dopant specie 89 of a chosen type and concentration which can be different from that which will be implanted to form the source and drain regions of the device, or the polysilicon layer 86 may be left undoped. The choice and concentration of dopant specie (or alternatively the lack of such dopant specie) will be instrumental in determining a work function of the gate of the resulting structure as will be described further on.

A mask layer, for example a nitride layer 90, is formed over the polysilicon layer 86, and polysilicon body 86, cap body 90 and gate oxide 84 (Figure 8) are formed therefrom by well-known means.

Then, an ion implantation step 92 is undertaken (Figure 9) to form lightly doped regions 94, 96, selection of this dopant specie 98 being appropriate to the type of device to be fabricated, for example arsenic for an N type device, or boron for a P type device, using the cap body 90, polysilicon body 86 and gate oxide 84 as an overall mask 100. With reference to Figure 10, an oxide layer 102 is deposited over the resulting structure, and is anisotropically etched to form spacers 104, 106 on the opposite sides of the polysilicon body 86 and cap body 84 (Figure 11). Then, an ion implantation step 108 is undertaken using the spacers 104, 106, along with the cap body 90, polysilicon body 86 and oxide layer 84 as an overall mask 110 to form heavily doped regions 112, 114, again with selection of this dopant specie 98 being appropriate to the type of device to be fabricated, i.e., for example arsenic for an N type device, or boron for a P type device. (Figure 11).

Annealing (such as rapid thermal anneal) is undertaken to activate the implants to form the source drain regions 116, 118 of the device 80. With reference to Figure 12, the cap body 90 is removed by appropriate means such as etching (as noted, the cap body 90 and spacers 104, 106 may be of different materials so that the removal of the cap body 90 does not affect the spacers 104, 106).

Next, with reference to Figure 13, a metal layer 120, for example, nickel, is deposited over the resulting structure, i.e., over the polysilicon body the 6, the spacers 104, 106, and the substrate 82 over the source and drain regions 116, 118, the nickel layer 120 being more than one-half as thick as the polysilicon body 86.

Then, the resulting structure undergoes a rapid thermal anneal, causing the nickel 120 to react with the silicon of the substrate 82 and the polysilicon body 86 to grow nickel silicide 122, 124, 126 into the polysilicon body 86 (to form gate 122) and into the source and drain regions 116, 118. Again, the nickel layer 120 is thick enough in relation to the thickness of the polysilicon body 86, and the silicidation step is undertaken long enough, to provide that substantially the entire polysilicon body 86 is silicidized. However, because the polysilicon body 86 is substantially thinner than the polysilicon body 36 of the embodiment of Figure 1-6, the resulting silicide gate 122 and the silicide regions 124, 126 in the source and drain regions 116, 118 are substantially thinner or shallower than in the embodiment of Figure 1-6, i.e., the silicide regions 124, 126 do not extend into the source and drain regions as deeply as in that embodiment, avoiding possible problems of shorting of the source and/or drain regions. Thus, proper device configuration is achieved even with relatively shallow source and drain regions. Inclusion of the cap body 90 over the polysilicon body 86 during the ion implantation step 108 (Figure 11) allows for provision of a thinner polysilicon body 86, while insuring that proper masking of the semiconductor body 82 under the overall mask 110 is achieved.

Similar to the previous process, the dopant 89 in the polysilicon body 86, previously generally evenly distributed therewithin, is driven downward by the downwardly advancing interface of nickel silicide and polysilicon until a substantial amount of the dopant specie 89 is pushed into a portion 150 of the gate 122 adjacent the gate oxide 84, so that the portion 150 of the gate 122 adjacent the gate oxide 84 contains a substantially higher dopant concentration than the portion 152 further away from the gate oxide 84. This results in a work function of the gate 122 being determined as described above. However, in this embodiment, instead of the work function of the gate 122 being determined by the dopant specie 98 used for the source 116 and drain 118 of the device 80, the work function of the gate 122 is determined by independent selection of the dopant specie 89 in the polysilicon body 86. It will thus be seen that the work function of the gate 122 can be selected and tailored to specific needs, independent of the dopant specie chosen for the source and drain of the device 80.

The unreacted nickel portions are then removed, leaving the structure shown in Figure 14.

It will be understood that while specific N type and P type dopants are described above, any appropriate dopant specie, including N type, P type, or neither N type nor P type, can with advantage be utilized.

Initially, it will be seen that the advantages of a metal gate device are provided, i.e., increased conductivity as compared to a polysilicon gate device, and avoidance of problems of polysilicon depletion and for a penetration. Additionally, tailoring of the work function of the gate can be achieved, allowing reduction of dopant concentration in the device channel (with its attendant advantages) without compromising device performance.

The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Other modifications or variations are possible in light of the above teachings.

The embodiments were chosen and described to provide the best illustration of the principles of the invention and its practical application to thereby enable one of ordinary skill of the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally and equitably entitled.

CLAIMS:

What is claimed is:

1. A method of fabricating a semiconductor structure characterized by:

providing a substrate (32);

providing a dielectric (34) on the substrate (32);

providing a polysilicon body (36) on the dielectric (34), the polysilicon body (36) containing a dopant specie (39);

providing a metal layer (60) on the polysilicon body (36); and

undertaking a silicidation process to silicidize substantially the entire polysilicon body (36) and provide a conductive body (62) on the dielectric (34); and

selecting the dopant specie (39) in the polysilicon body (36), the selection thereof being dependent upon the desired work function of the conductive body (36).

2. The method of claim 1 characterized by the step of undertaking the silicidation process to drive a substantial portion of the dopant specie (39) to adjacent the dielectric (34).

3. The method of claim 2 and further characterized by the step of providing that the conductive body (62) is a gate.

4. A method of fabricating a semiconductor structure characterized by:

providing a substrate (82);

providing a dielectric (84) on the substrate (82);

providing a polysilicon body (86) on the dielectric (84);

providing a cap body (90) on the polysilicon body (86);

introducing dopant (98) into the substrate (82) using the cap body (90) and polysilicon body (86) as a mask;

removing the cap body (90) from the polysilicon body (86);

providing a metal layer (120) on the polysilicon body (86); and

undertaking a silicidation process to silicidize substantially the entire polysilicon body (86).

5. The method of claim 4 and further characterized by providing spacers (104, 106) on opposite sides of the cap body (90) and polysilicon body (86), the spacers (104, 106), along with the cap body (90) and polysilicon body (86), acting as a mask for introducing dopant (98) into the substrate (82).

6. The method of claim 4 and further characterized by the step of providing that the metal layer (120) on the polysilicon body is a nickel layer more than one-half as thick as the polysilicon body (86).

7. The method of claim 4 characterized by the step of undertaking a silicidation process to silicidize substantially the entire polysilicon body to form a gate (122) on the dielectric (84).

8. The method of claim 4 characterized by the step of providing the polysilicon body (86) containing a dopant specie (89).

9. A semiconductor structure characterized by:

a substrate (32);

a dielectric (34) on the substrate (32);

a gate (62) on the dielectric (34), the gate (62) containing a dopant specie (39), a portion (68) of the gate (62) adjacent the dielectric (34) having a higher concentration of dopant specie (39) than a portion (70) of the gate (62) further from the dielectric (34).

10. The semiconductor structure of claim 9 characterized by the gate (62) comprising a silicide.