

DESCRIPTION

DISPLAY DEVICE AND DRIVE METHOD THEREFOR

5 TECHNICAL FIELD

[0001] The present invention relates to a display device and, more particularly to a display device using current-driven elements such as an organic EL display, and a drive method therefor.

10

BACKGROUND ART

[0002] As a thin, high image quality, and low power consumption display device, an organic EL (Electro Luminescence) display is known. The organic EL display includes a plurality of pixel circuits including an organic EL element and a driving transistor. When providing display on the organic EL display, there is a need to compensate for variations in the threshold voltage of the driving transistors and an increase in resistance caused by deterioration over time of the organic EL elements.

15

[0003] Various types of pixel circuits that perform compensation operation are conventionally known. Patent Document 1 describes a pixel circuit 80 shown in Fig. 18. The pixel circuit 80 includes TFTs (Thin Film Transistors) 81 to 85, a capacitor 86, and an organic EL element 87. When writing to the pixel circuit 80, first, the TFTs 82 and 84 are controlled to an on state to initialize the gate-source voltage of the TFT 85 (driving transistor). Then, the TFT 84 and the TFT 83 are controlled to an off state in turn to allow the capacitor 86 to hold the threshold voltage of the TFT 85. Then, a data potential is applied to a data line DTL and the TFT 81 is

25

30

controlled to an on state. Accordingly, variations in the threshold voltage of the TFT 85 and an increase in resistance caused by deterioration over time of the organic EL element 87 can be compensated for.

5 [0004] The pixel circuit 80 is connected to the data line DTL, four control lines WSL, AZL1, AZL2, and DSL, and three power lines (a wiring line for Vofs, a wiring line for Vcc, and a wiring line for Vss). In general, the larger the number of wiring lines (particularly, control lines) connected to a pixel circuit, the
10 more complex the circuit becomes, increasing manufacturing cost. Hence, Patent Document 1 describes a pixel circuit where the source terminal of the TFT 82 or the TFT 84 is connected to the control line WSL. Patent Document 2 describes a pixel circuit where the gate terminal of the TFT 82 is connected to a control
15 line WSL in a previous row. By thus commonizing a control line and a power line, the number of wiring lines can be reduced. [0005] Patent Document 3 describes a pixel circuit 90 shown in Fig. 19. The pixel circuit 90 includes TFTs 91 and 92, a capacitor 93, and an organic EL element 94. When writing to
20 the pixel circuit 90, first, the TFT 91 is controlled to an on state. Then, an initialization potential is applied to a power line DSL to provide the initialization potential to the anode terminal of the organic EL element 94. Then, a power supply potential is applied to the power line DSL to allow the capacitor
25 93 to hold the threshold voltage of the TFT 92 (driving transistor). Then, a data potential is applied to a data line DTL. By thus providing an initialization potential from the power line, variations in the threshold voltage of the TFT 92 can be compensated for with a small number of elements. Patent
30 Document 4 describes a pixel circuit where an initialization

potential is provided from a power line and a reference potential is provided from a data line. Patent Document 5 describes a pixel circuit that performs compensation operation during a plurality of horizontal periods before writing.

5

PRIOR ART DOCUMENTS

PATENT DOCUMENTS

[0006] [Patent Document 1] Japanese Laid-Open Patent Publication No. 2006-215275

10 [Patent Document 2] Japanese Laid-Open Patent Publication No. 2007-316453

[Patent Document 3] Japanese Laid-Open Patent Publication No. 2007-310311

15 [Patent Document 4] Japanese Laid-Open Patent Publication No. 2007-148129

[Patent Document 5] Japanese Laid-Open Patent Publication No. 2008-33193

SUMMARY OF THE INVENTION

20 PROBLEMS TO BE SOLVED BY THE INVENTION

[0007] By applying the methods described in Patent Documents 1 and 2 to the pixel circuit 80 shown in Fig. 18, the number of wiring lines connected to the pixel circuit can be reduced. However, a pixel circuit obtained according to the methods has
 25 a problem that there are a large number of TFTs. On the other hand, the pixel circuit 90 shown in Fig. 19 has a small number of TFTs. However, when the pixel circuit 90 is used, the power line DSL needs to be driven in conjunction with a control line WSL. Hence, a power control circuit requires output buffers
 30 which are of the same number as the power lines DSLs. In

addition, since the potential of the power line DSL needs to change in a short time in accordance with a selection period of the control line WSL, the output buffers provided in the power control circuit require high current capability. Therefore, the pixel circuit 90 has a problem that the circuit size and power consumption of the power control circuit increase.

[0008] An object of the present invention is therefore to provide a display device having a configuration in which an initialization potential is provided to pixel circuits from power lines, and having a power control circuit small in circuit size.

MEANS FOR SOLVING THE PROBLEMS

[0009] According to a first aspect of the present invention, there is provided a current-driven type display device, including: a plurality of pixel circuits arranged two-dimensionally; a plurality of control lines provided for respective rows of the pixel circuits; a plurality of data lines provided for respective columns of the pixel circuits; a plurality of power lines provided to supply a power supply potential to the pixel circuits; a single or a plurality of common power lines, each connected to two or more of the power lines; a drive circuit that drives the control lines and the data lines; and a power control circuit that drives the power lines, wherein each of the pixel circuits includes: an electro-optic element; a driving transistor provided on a path of a current flowing through the electro-optic element; a write control transistor provided between a control terminal of the driving transistor and a corresponding one of the data lines; a light emission control transistor provided between one

conduction terminal of the driving transistor and a corresponding one of the power lines; and a capacitor provided between an other conduction terminal and the control terminal of the driving transistor, and the power control circuit applies
5 the power supply potential and an initialization potential to the common power line(s) in a switching manner.

[0010] According to a second aspect of the present invention, in the first aspect of the present invention, the drive circuit selects initialized pixel circuits on a row basis, and controls
10 to allow each of the selected pixel circuits to perform detection of a threshold of the driving transistor, writing, and light emission in turn.

[0011] According to a third aspect of the present invention, in the second aspect of the present invention, the light
15 emission control transistor is placed in an on state upon initialization, and the initialization potential is a potential at which the driving transistor is placed in an on state when the potential is applied to the power line upon initialization.

[0012] According to a fourth aspect of the present invention, in the third aspect of the present invention, the light emission
20 control transistor is placed in an off state upon completion of the initialization and is placed in an on state upon threshold detection.

[0013] According to a fifth aspect of the present invention, in the fourth aspect of the present invention, the light
25 emission control transistor is placed in an on state for a fixed period of time upon light emission.

[0014] According to a sixth aspect of the present invention, in the second aspect of the present invention, each of the pixel
30 circuits further includes a reference potential application

transistor provided between the control terminal of the driving transistor and a reference potential line.

[0015] According to a seventh aspect of the present invention, in the second aspect of the present invention, each of the pixel circuits further includes a reference potential application transistor that is provided between the control terminal of the driving transistor and a control line connected to the write control transistor, and that has a control terminal connected to a control line provided for pixel circuits in another row.

[0016] According to an eighth aspect of the present invention, in the second aspect of the present invention, upon threshold detection, a reference potential is applied to the data line and the write control transistor is placed in an on state.

[0017] According to a ninth aspect of the present invention, in the first aspect of the present invention, the display device includes a single common power line.

[0018] According to a tenth aspect of the present invention, in the first aspect of the present invention, the display device includes a plurality of common power lines, wherein the power lines are provided for the respective rows of the pixel circuits, and the power control circuit applies the initialization potential to the common power lines at different timings.

[0019] According to an eleventh aspect of the present invention, in the tenth aspect of the present invention, a plurality of power lines disposed adjacent to each other are connected to each of the common power lines.

[0020] According to a twelfth aspect of the present invention, in the tenth aspect of the present invention, a plurality of power lines selected every predetermined number of lines according to order of disposition are connected to each of the

common power lines.

[0021] According to a thirteenth aspect of the present invention, in the first aspect of the present invention, all of the transistors included in the pixel circuit are of an N-channel type.

[0022] According to a fourteenth aspect of the present invention, there is provided a method of driving a current-driven type display device including a plurality of pixel circuits arranged two-dimensionally; a plurality of control lines provided for respective rows of the pixel circuits; a plurality of data lines provided for respective columns of the pixel circuits; a plurality of power lines provided to supply a power supply potential to the pixel circuits; and a single or a plurality of common power lines, each connected to two or more of the power lines, the method including the steps of: when each of the pixel circuits includes: an electro-optic element; a driving transistor provided on a path of a current flowing through the electro-optic element; a write control transistor provided between a control terminal of the driving transistor and a corresponding one of the data lines; a light emission control transistor provided between one conduction terminal of the driving transistor and a corresponding one of the power lines; and a capacitor provided between an other conduction terminal and the control terminal of the driving transistor, applying, using a power control circuit, the power supply potential and an initialization potential to the common power line(s) in a switching manner; controlling states of the transistors included in the pixel circuits by driving the control lines; and applying potentials corresponding to display data to the data lines.

EFFECTS OF THE INVENTION

[0023] According to the first or fourteenth aspect of the present invention, by applying an initialization potential to the common power line(s) using the power control circuit, the initialization potential can be provided to the pixel circuits from the power lines. Accordingly, the number of elements in each pixel circuit can be reduced. In addition, the power control circuit drives the common power line(s), each connected to two or more power lines. Therefore, compared to the case of individually driving the power lines, the number of output buffers provided in the power control circuit is reduced, making it possible to reduce the circuit size of the power control circuit.

[0024] According to the second aspect of the present invention, initialized pixel circuits are selected on a row basis, and the selected pixel circuits perform threshold detection, writing, and light emission in turn. Accordingly, threshold voltages of the driving transistors are compensated for and then a screen can be displayed.

[0025] According to the third aspect of the present invention, by controlling the light emission control transistor to an on state by applying an initialization potential to the power line, the initialization potential can be applied to the other conduction terminal of the driving transistor.

[0026] According to the fourth aspect of the present invention, by controlling the light emission control transistor to an off state upon completion of initialization and controlling the light emission control transistor to an on state upon threshold detection, the pixel circuit can be allowed to turn off during

a period from the initialization to the threshold detection. In addition, upon threshold detection, by supplying a current from the power line, a threshold of the driving transistor can be detected.

5 [0027] According to the fifth aspect of the present invention, by controlling the light emission control transistors to an on state for a fixed period of time upon light emission, the lengths of the light emission periods of the pixel circuits are made the same, making it possible to suppress variations in luminance.

10 In addition, since the pixel circuits turn off during periods other than the light emission period, moving image performance can be improved as in the case of performing black insertion.

[0028] According to the sixth aspect of the present invention, by controlling the reference potential application transistor
15 to an on state upon threshold detection, a reference potential is applied to the control terminal of the driving transistor from the reference potential line, making it possible to detect a threshold of the driving transistor. In addition, since the reference potential application transistor can be controlled
20 to an on state at relatively flexible timing, a threshold detection period can be freely set.

[0029] According to the seventh aspect of the present invention, by controlling the reference potential application transistor to an on state upon threshold detection, a reference potential
25 is applied to the control terminal of the driving transistor from the control line, making it possible to detect a threshold of the driving transistor. In addition, reference potential lines and control lines for reference potential application transistors can be removed.

30 [0030] According to the eighth aspect of the present invention,

by controlling the write control transistor to an on state upon threshold detection, a reference potential is applied to the control terminal of the driving transistor from the data line, making it possible to detect a threshold of the driving transistor. In addition, without adding a transistor or a wiring line, a reference potential can be provided from the data line.

[0031] According to the ninth aspect of the present invention, the number of output buffers provided in the power control circuit is reduced to one, making it possible to reduce the circuit size of the power control circuit.

[0032] According to the tenth aspect of the present invention, the number of output buffers provided in the power control circuit is made smaller than the number of power lines, making it possible to reduce the circuit size of the power control circuit. In addition, by applying an initialization potential to the common power lines at different timings, initialization of the pixel circuits can be performed at suitable timing in accordance with a selection period of the pixel circuits.

[0033] According to the eleventh aspect of the present invention, writing can be performed to the pixel circuits according to the order on a display screen.

[0034] According to the twelfth aspect of the present invention, the amounts of current flowing through the common power lines are made the same, making it possible to prevent the occurrence of a difference in luminance on a screen.

[0035] According to the thirteenth aspect of the present invention, by configuring the transistors included in the pixel circuit by the same conductive type of transistors, the manufacturing cost of a display device including pixel circuits

can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] Fig. 1 is a block diagram showing a configuration of a display device according to a first embodiment of the present invention.

Fig. 2 is a circuit diagram of a pixel circuit included in the display device shown in Fig. 1.

Fig. 3 is a timing chart showing a method of driving the pixel circuits in the display device shown in Fig. 1.

Fig. 4 is a diagram showing a connection configuration of power lines in a display device according to a first example.

Fig. 5 is a diagram showing operations of pixel circuits in each row in the display device according to the first example.

Fig. 6 is a diagram showing a connection configuration of power lines in a display device according to a second example.

Fig. 7 is a diagram showing operations of pixel circuits in each row in the display device according to the second example.

Fig. 8 is a diagram showing a connection configuration of power lines in a display device according to a third example.

Fig. 9 is a diagram showing operations of pixel circuits in each row in the display device according to the third example.

Fig. 10 is a diagram showing a connection configuration of power lines in a display device according to a fourth example.

Fig. 11 is a diagram showing operations of pixel circuits in each row in the display device according to the fourth example.

Fig. 12 is a block diagram showing a configuration of a display device according to a second embodiment of the present

invention.

Fig. 13 is a circuit diagram of a pixel circuit included in the display device shown in Fig. 12.

Fig. 14 is a timing chart showing a method of driving the
5 pixel circuits in the display device shown in Fig. 12.

Fig. 15 is a block diagram showing a configuration of a display device according to a third embodiment of the present invention.

Fig. 16 is a circuit diagram of a pixel circuit included
10 in the display device shown in Fig. 15.

Fig. 17 is a timing chart showing a method of driving the pixel circuits in the display device shown in Fig. 15.

Fig. 18 is a circuit diagram of a pixel circuit included in a conventional display device.

Fig. 19 is a circuit diagram of a pixel circuit included
15 in a conventional display device.

MODES FOR CARRYING OUT THE INVENTION

[0037] (First Embodiment)

Fig. 1 is a block diagram showing a configuration of a
20 display device according to a first embodiment of the present invention. A display device 100 shown in Fig. 1 is an organic EL display including a display control circuit 1, a gate driver circuit 102, a source driver circuit 3, a power control circuit
25 4, and $(m \times n)$ pixel circuits 10. In the following, m and n are integers not smaller than 2, i is an integer between 1 and n inclusive, and j is an integer between 1 and m inclusive.
[0038] In the display device 100, n control lines G_i parallel to one another and m data lines S_j parallel to one another and
30 intersecting with the control lines G_i perpendicularly are

provided. The $(m \times n)$ pixel circuits 10 are arranged two-dimensionally at respective intersections of the control lines G_i and the data lines S_j . In addition, n control lines R_i , n control lines E_i , and n power lines V_{Pi} are provided parallel to the control lines G_i . Furthermore, to connect the power control circuit 4 to the power lines V_{Pi} , p common power lines 9 (p is an integer not smaller than 1) are provided. The control lines G_i , R_i , and E_i are connected to the gate driver circuit 102, and the data lines S_j are connected to the source driver circuit 3. The power lines V_{Pi} are connected to the power control circuit 4 through the common power lines 9. A reference potential V_{ref} and a common potential V_{com} are supplied to the pixel circuits 10 by means which are not shown.

[0039] The display control circuit 1 outputs control signals to the gate driver circuit 102, the source driver circuit 3, and the power control circuit 4. More specifically, the display control circuit 1 outputs a timing signal OE , a start pulse YI , and a clock YCK to the gate driver circuit 102, outputs a start pulse SP , a clock CLK , display data DA , and a latch pulse LP to the source driver circuit 3, and outputs a control signal CS to the power control circuit 4.

[0040] The gate driver circuit 102 includes a shift register circuit, a logic operation circuit, and a buffer (none of which are shown). The shift register circuit sequentially transfers the start pulse YI in synchronization with the clock YCK . The logic operation circuit performs a logic operation between a pulse outputted from each stage of the shift register circuit and the timing signal OE . An output from the logic operation circuit is provided to corresponding control lines G_i , R_i , and E_i through the buffer. To each control line G_i are connected

m pixel circuits 10, and m pixel circuits 10 are selected collectively using a corresponding control line Gi.

[0041] The source driver circuit 3 includes an m-bit shift register 5, a register 6, a latch circuit 7, and m D/A converters 8. The shift register 5 has m cascade-connected registers, and transfers the start pulse SP supplied to the first-stage register, in synchronization with the clock CLK and outputs timing pulses DLPs from the registers of the respective stages. Display data DA is supplied to the register 6 in accordance with the output timing of the timing pulses DLPs. The register 6 stores the display data DA according to the timing pulses DLPs. When display data DA for one row is stored in the register 6, the display control circuit 1 outputs the latch pulse LP to the latch circuit 7. When the latch circuit 7 receives the latch pulse LP, the latch circuit 7 holds the display data stored in the register 6. The D/A converters 8 are provided for the respective data lines Sj. The D/A converters 8 convert the display data held in the latch circuit 7 into analog voltages and apply the obtained analog voltages to the corresponding data lines Sj.

[0042] The power control circuit 4 has p output terminals for the p common power lines 9. The power control circuit 4 applies, based on the control signal CS, a power supply potential and an initialization potential to the common power lines 9 in a switching manner. When $p = 1$, all of the power lines VPi are connected to a single common power line 9. In this case, the power control circuit 4 applies the initialization potential to the single common power line 9 at predetermined timing. When $p \geq 2$, the power lines VPi are grouped into p groups and power lines included in each group are connected to the same common

power line 9. In this case, the power control circuit 4 applies the initialization potential to the p common power lines 9 at different timings. In the following, it is assumed that the power supply potential is a high-level potential and the initialization potential is a low-level potential.

[0043] Fig. 2 is a circuit diagram of the pixel circuit 10. As shown in Fig. 2, the pixel circuit 10 includes TFTs 11 to 14, a capacitor 15, and an organic EL element 16. The TFTs 11 to 14 are all N-channel type transistors. The TFTs 11 to 14 respectively function as a write control transistor, a driving transistor, a light emission control transistor, and a reference potential application transistor. The organic EL element 16 functions as an electro-optic element.

[0044] As shown in Fig. 2, the pixel circuit 10 is connected to the control lines G_i , R_i , and E_i , the data line S_j , the power line V_{Pi} , a wiring line having a reference potential V_{ref} , and an electrode having a common potential V_{com} . One conduction terminal of the TFT 11 is connected to the data line S_j and the other conduction terminal of the TFT 11 is connected to the gate terminal of the TFT 12. The drain terminal of the TFT 13 is connected to the power line V_{Pi} and the source terminal of the TFT 13 is connected to the drain terminal of the TFT 12. The reference potential V_{ref} is applied to the drain terminal of the TFT 14 and the source terminal of the TFT 14 is connected to the gate terminal of the transistor T12. The source terminal of the TFT 12 is connected to the anode terminal of the organic EL element 16. The common potential V_{com} is applied to the cathode terminal of the organic EL element 16. The capacitor 15 is provided between the gate and source terminals of the TFT 12. The gate terminals of the TFTs 11, 13, and 14 are connected

to the control lines G_i , E_i , and R_i , respectively.

[0045] Fig. 3 is a timing chart showing a method of driving the pixel circuits 10. In Fig. 3, V_{Gi} indicates the gate potential of the TFT 12 included in a pixel circuit in an i -th row, and V_{Si} indicates the source potential of the TFT (the anode potential of the organic EL element 16). Each pixel circuit 10 performs initialization, threshold detection (detection of a threshold of a TFT 12), writing, and light emission each once during one frame period, and turns off during periods other than a light emission period.

[0046] With reference to Fig. 3, the operation of the pixel circuits in the first row will be described below. Prior to time t_{11} , the potentials of control lines G_1 , R_1 , and E_1 are at a low level and the potential of a power line VP_1 is at a high level. At time t_{11} , the potential of the control line E_1 changes to a high level and the potential of the power line VP_1 changes to a low level (hereinafter, the low-level potential of the power line VP_i is referred to as VP_L). For the potential VP_L , a sufficiently low potential, specifically, a potential lower than the gate potential of the TFT 12 immediately before time t_{11} , is used. Hence, after time t_{11} , the TFT 12 is placed in an on state. In addition, since the TFT 13 is also placed in an on state, the source potential VS_1 of the TFT 12 is substantially equal to VP_L .

[0047] At time t_{12} , the potential of the control line E_1 changes to a low level and the potential of the power line VP_1 changes to a high level. After time t_{12} , the TFT 13 is placed in an off state. Hence, even if the potential of the power line VP_1 is changed, the source potential VS_1 of the TFT 12 remains at substantially VP_L .

[0048] At time t13, the potentials of the control lines R1 and E1 change to a high level. After time t13, the TFTs 13 and 14 are placed in an on state and the reference potential Vref is applied to the gate terminal of the TFT 12. The reference potential Vref is determined such that the TFT 12 is placed in an on state immediately after time t13 and the voltage applied to the organic EL element 16 does not exceed a light emission threshold voltage after time t13. Hence, after time t13, the TFT 12 is placed in an on state but a current does not flow through the organic EL element 16. Therefore, a current flows into the source terminal of the TFT 12 from the power line VP1 through the TFT 13 and the TFT 12 and thus the source potential VS1 of the TFT 12 rises. The source potential VS1 of the TFT 12 rises until the gate-source voltage Vgs becomes equal to the threshold voltage Vth, and reaches (Vref-Vth).

[0049] At time t14, the potential of the control line E1 changes to a low level. After time t14, the TFT 13 is placed in an off state. At time t15, the potential of the control line R1 changes to a low level. After time t15, the TFT 14 is placed in an off state.

[0050] At time t16, the potential of the control line G1 changes to a high level and the potential of a data line Sj (not shown) reaches a level corresponding to display data (hereinafter, the potential of the data line Sj at this time is referred to as a data potential Vda). After time t16, the TFT 11 is placed in an on state and the gate potential VG1 of the TFT 12 changes from Vref to Vda. The gate-source voltage Vgs of the TFT 12 after time t16 is given by the following equation (1):

$$V_{gs} = \{C_{OLED} / (C_{OLED} + C_{st})\} \times (V_{da} - V_{ref}) + V_{th} \quad \dots (1).$$

Note that in equation (1) C_{OLED} is the capacitance value of the organic EL element 16 and C_{st} is the capacitance value of the capacitor 15.

[0051] The capacitance value of the organic EL element 16 is sufficiently large and thus $C_{\text{OLED}} \gg C_{\text{st}}$ holds true. Hence, equation (1) can be transformed into the following equation (2):

$$V_{\text{gs}} = V_{\text{da}} - V_{\text{ref}} + V_{\text{th}} \quad \dots (2).$$

As such, when the gate potential V_{G1} of the TFT 12 is changed from V_{ref} to V_{da} , the source potential V_{S1} of the TFT 12 does not change almost at all and the gate-source voltage V_{gs} of the TFT 12 reaches substantially $(V_{\text{da}} - V_{\text{ref}} + V_{\text{th}})$.

[0052] At time t_{17} , the potential of the control line G_1 changes to a low level. After time t_{17} , the TFT 11 is placed in an off state. Hence, even if the potential of the data line S_j changes, the gate-source voltage V_{gs} of the TFT 12 remains at substantially $(V_{\text{da}} - V_{\text{ref}} + V_{\text{th}})$.

[0053] At time t_{18} , the potential of the control line E_1 changes to a high level. After time t_{18} , the TFT 13 is placed in an on state and the drain terminal of the TFT 12 is connected to the power line VP_1 through the TFT 13. Since the potential of the power line VP_1 is at a high level at this time, a current flows into the source terminal of the TFT 12 from the power line VP_i through the TFT 13 and the TFT 12 and thus the source potential V_{S1} of the TFT 12 rises. At this time point, the gate terminal of the TFT 12 is in a floating state. Therefore, when the source potential V_{S1} of the TFT 12 rises, the gate potential V_{G1} of the TFT 12 also rises. At this time, the gate-source voltage V_{gs} of the TFT 12 is maintained substantially constant.

[0054] The high-level potential applied to the power line VP_i is determined such that the TFT 12 operates in a saturation

region during a light emission period (time t18 to t19). Hence, a current I flowing through the TFT 12 during the light emission period is given by the following equation (3), ignoring the channel-length modulation effect:

$$I = 1/2 \cdot W/L \cdot \mu \cdot C_{ox} (V_{gs} - V_{th})^2 \quad \dots (3).$$

Note that in equation (3) W is the gate width, L is the gate length, μ is the carrier mobility, and C_{ox} is the capacitance of a gate oxide film.

[0055] The following equation (4) is derived from equation (2) and equation (3):

$$I = 1/2 \cdot W/L \cdot \mu \cdot C_{ox} (V_{da} - V_{ref})^2 \quad \dots (4).$$

The current I shown in equation (4) changes corresponding to the data potential V_{da} but does not depend on the threshold voltage V_{th} of the TFT 12. Therefore, even if the threshold voltage V_{th} varies or if the threshold voltage V_{th} changes over time, it is possible to make a current corresponding to the data potential V_{da} flow through the organic EL element 16 and to make the organic EL element 16 emit light at a desired luminance.

[0056] At time t19, the potential of the control line E1 changes to a low level. After time t19, the TFT 13 is placed in an off state. Hence, a current does not flow through the organic EL element 16 and thus the pixel circuit 10 turns off.

[0057] As such, the pixel circuits in the first row perform initialization at time t11 to t12, perform threshold detection at time t13 to t14, perform writing at time t16 to t17, and emit light at time t18 to t19, and turn off during time other than time t18 to t19. Pixel circuits in the second row perform initialization at time t11 to t12 as with the pixel circuits in the first row, and perform threshold detection, writing, and light emission, delayed by a predetermined time T_a from the

pixel circuits in the first row. In general, pixel circuits in an i -th row perform initialization during the same period as that during which pixel circuits in other rows do, and perform threshold detection, writing, and light emission, delayed by a time T_a from pixel circuits in an $(i-1)$ -th row.

[0058] As examples of the display device according to the present embodiment, the case of $p = 1$ (first example), the case of $p = 2$ (second and third examples), and the case of $p = 3$ (fourth example) will be described below. Fig. 4 is a diagram showing a connection configuration of power lines V_{Pi} in a display device according to the first example. In the display device according to the first example, a single common power line 111 is provided to connect a power control circuit 4a to the power lines V_{Pi} . One end of the common power line 111 is connected to one output terminal provided in the power control circuit 4a, and all of the power lines V_{Pi} are connected to the common power line 111.

[0059] Fig. 5 is a diagram showing operations of pixel circuits in each row in the display device according to the first example. The power control circuit 4a applies a low-level potential to the common power line 111 for a predetermined period of time at the start of one frame period. Hence, the pixel circuits in all rows perform initialization at the start of one frame period. Then, pixel circuits in the first row are selected and the pixel circuits in the first row perform threshold detection and writing. Then, pixel circuits in the second row are selected and the pixel circuits in the second row perform threshold detection and writing. Thereafter, likewise, pixel circuits in the third to the n -th rows are selected in turn on a row-by-row basis, and the selected pixel

circuits perform threshold detection and writing.

[0060] The pixel circuits in each row turn off during a period from initialization to threshold detection. The pixel circuits in each row need to emit light for the same amount of time, and light emission of pixel circuits in the n-th row needs to be completed before the end of one frame period. Hence, the pixel circuits in each row emit light for a fixed period of time T_1 after writing and turn off during other periods of time.

[0061] In a common display device, writing to pixel circuits is performed over one frame period. On the other hand, in the example shown in Fig. 5, writing to pixel circuits is performed over about a $1/2$ frame period. Hence, the scanning speed of the pixel circuits is about twice the normal scanning speed. In addition, in this example, the length T_1 of the light emission period of the pixel circuits is about a $1/2$ frame period. Note that the length of the light emission period may be made shorter than a $1/2$ frame period, with the scanning speed of the pixel circuits remaining about twice the normal scanning speed. Alternatively, the scanning speed of the pixel circuits may be made faster than about twice the normal scanning speed and the length of the light emission period may be made longer than a $1/2$ frame period.

[0062] Fig. 6 is a diagram showing a connection configuration of the power lines VP_i in a display device according to the second example. In the display device according to the second example, two common power lines 121 and 122 are provided to connect a power control circuit 4b to the power lines VP_i . Ends of the respective common power lines 121 and 122 are respectively connected to two output terminals provided in the power control circuit 4b. The power lines VP_1 to $VP_{n/2}$ are connected to the

common power line 121, and the power lines $VP(n/2+1)$ to VPn are connected to the common power line 122.

[0063] Fig. 7 is a diagram showing operations of pixel circuits 10 in each row in the display device according to the second example. The power control circuit 4b applies a low-level potential to the common power line 121 for a predetermined period of time at the start of one frame period, and applies a low-level potential to the common power line 122 for the predetermined period of time after a lapse of a $1/2$ frame period.

10 Hence, pixel circuits in the first to the $(n/2)$ -th rows perform initialization at the start of one frame period, and pixel circuits in the $(n/2+1)$ -th to the n -th rows perform initialization, delayed by a $1/2$ frame period. After the first initialization the pixel circuits in the first to the $(n/2)$ -th rows are selected in turn on a row-by-row basis, and after the second initialization the pixel circuits in the $(n/2+1)$ -th to the n -th rows are selected in turn on a row-by-row basis. The selected pixel circuits perform threshold detection and writing. The pixel circuits in each row emit light for a fixed period of time $T2$ after writing and turn off during other periods of time.

[0064] In the display device according to the second example, as in the first example, the pixel circuits in each row need to emit light for the same amount of time, but unlike the first example, light emission of pixel circuits in the n -th row does not need to be completed before the end of one frame period. In the example shown in Fig. 7, the scanning speed of the pixel circuits is the same as the normal scanning speed, and the length $T2$ of the light emission period of the pixel circuits is about a $1/2$ frame period.

[0065] Fig. 8 is a diagram showing a connection configuration of the power lines VP_i in a display device according to the third example. In the display device according to the third example, two common power lines 131 and 132 are provided to connect a power control circuit 4c to the power lines VP_i . Ends of the respective common power lines 131 and 132 are respectively connected to two output terminals provided in the power control circuit 4c. The power lines $VP_1, VP_3, \dots$ for the odd-numbered rows are connected to the common power line 131, and the power lines $VP_2, VP_4, \dots$ for the even-numbered rows are connected to the common power line 132.

[0066] Fig. 9 is a diagram showing operations of pixel circuits in each row in the display device according to the third example. The power control circuit 4c applies a low-level potential to the common power line 131 for a predetermined period of time at the start of one frame period, and applies a low-level potential to the common power line 132 for the predetermined period of time after a lapse of a $1/2$ frame period. Hence, pixel circuits in the odd-numbered rows perform initialization at the start of one frame period, and pixel circuits in the even-numbered rows perform initialization, delayed by a $1/2$ frame period. After the first initialization the pixel circuits in the odd-numbered rows are selected in turn, and after the second initialization the pixel circuits in the even-numbered rows are selected in turn. The selected pixel circuits perform threshold detection and writing. The pixel circuits in each row emit light for a fixed period of time T_3 after writing and turn off during other periods of time. In the example shown in Fig. 9, the scanning speed of the pixel circuits is the same as the normal scanning speed, and the length

T3 of the light emission period of the pixel circuits is about a 1/2 frame period.

[0067] According to the display device according to the second example, writing can be performed to the pixel circuits according to the order on a display screen. However, when there is a big difference between the amounts of current flowing through the common power lines 121 and 122, such as when there is a big difference in luminance between the upper and lower halves of the screen, a difference in luminance may occur at the center of the screen. According to the display device according to the third example, in many cases, the amounts of current flowing through the common power lines 131 and 132 are substantially the same, and thus, a difference in luminance occurring at the center of the screen can be prevented.

[0068] Fig. 10 is a diagram showing a connection configuration of the power lines VP_i in a display device according to the fourth example. In the display device according to the fourth example, three common power lines 141 to 143 are provided to connect a power control circuit 4d to the power lines VP_i . Ends of the respective common power lines 141 to 143 are respectively connected to three output terminals provided in the power control circuit 4d. The power lines VP_1 to $VP_{n/3}$ are connected to the common power line 141, the power lines $VP_{(n/3+1)}$ to $VP_{(2n/3)}$ are connected to the common power line 142, and the power lines $VP_{(2n/3+1)}$ to VP_n are connected to the common power line 143.

[0069] Fig. 11 is a diagram showing operations of pixel circuits 10 in each row in the display device according to the fourth example. The power control circuit 4d applies a low-level potential to the common power line 141 for a predetermined

period of time at the start of one frame period, applies a low-level potential to the common power line 142 for the predetermined period of time after a lapse of a $1/3$ frame period, and applies a low-level potential to the common power line 143
 5 for the predetermined period of time further after a lapse of a $1/3$ frame period. Hence, pixel circuits in the first to the $(n/3)$ -th rows perform initialization at the start of one frame period, pixel circuits in the $(n/3+1)$ -th to the $(2n/3)$ -th rows perform initialization, delayed by a $1/3$ frame period, and pixel
 10 circuits in the $(2n/3+1)$ -th to the n -th rows perform initialization, further delayed by a $1/3$ frame period.

[0070] After the first initialization the pixel circuits in the first to the $(n/3)$ -th rows are selected in turn on a row-by-row basis, and after the second initialization the pixel circuits
 15 in the $(n/3+1)$ -th to the $(2n/3)$ -th rows are selected in turn on a row-by-row basis, and after the third initialization the pixel circuits in the $(2n/3+1)$ -th to the n -th rows are selected in turn on a row-by-row basis. The selected pixel circuits perform threshold detection and writing. The pixel circuits
 20 in each row emit light for a fixed period of time T_4 after writing and turn off during other periods of time. In the example shown in Fig. 11, the scanning speed of the pixel circuits is the same as the normal scanning speed, and the length T_4 of the light emission period of the pixel circuits is about a $2/3$ frame
 25 period.

[0071] Note that the number p of the common power lines 9 may be 4 or more. When $p \geq 4$, the connection configuration of the power lines V_{Pi} and operations of pixel circuits 10 in each row are the same as those described above. In addition, when $p \geq$
 30 3, (n/p) power lines disposed adjacent to each other may be

connected to the same common power line, or (n/p) power lines selected every p -th line may be connected to the same common power line. For example, when $p = 3$, the power lines VP_i may be selected every third line and the power lines $VP_1, VP_4, \dots$ may be connected to a first common power line, the power lines $VP_2, VP_5, \dots$ to a second common power line, and the power lines $VP_3, VP_6, \dots$ to a third common power line. When $p = 1$, instead of providing n power lines VP_i for the respective rows of the pixel circuits 10, m power lines may be provided for the respective columns of the pixel circuits 10.

[0072] As such, there is a trade-off relationship between the number p of the common power lines 9, the scanning speed of the pixel circuits 10, and the length of the light emission period of the pixel circuits 10. For example, by increasing the number p of the common power lines 9, the scanning speed of the pixel circuits 10 can be reduced or the light emission period of the pixel circuits 10 can be made longer. Note, however, that at this time the number of output buffers provided in the power control circuit 4 increases and thus the circuit size of the power control circuit 4 increases. Therefore, these parameters may be determined taking into account the specifications, cost, etc., of the display device.

[0073] As described above, the display device 100 according to the present embodiment includes a plurality of pixel circuits 10 arranged two-dimensionally; a plurality of control lines $G_i, R_i,$ and E_i provided for the respective rows of the pixel circuits 10; a plurality of data lines S_j provided for the respective columns of the pixel circuits 10; a plurality of power lines VP_i provided to supply a power supply potential to the pixel circuits 10; p common power lines 9, each connected to two or

more power lines V_{Pi} ; a gate driver circuit 102 that drives the control lines G_i , R_i , and E_i ; a source driver circuit 3 that drives the data lines S_j and; and a power control circuit 4 that drives the power lines V_{Pi} . Each pixel circuit 10 includes an
5 organic EL element 16 (electro-optic element); a TFT 12 (driving transistor) provided on a path of a current flowing through the organic EL element 16; a TFT 11 (write control transistor) provided between the gate terminal of the TFT 12 and a corresponding data line S_j ; a TFT 13 (light emission control
10 transistor) provided between the drain terminal of the TFT 12 and a corresponding power line V_{Pi} ; and a capacitor 15 provided between the source and gate terminals of the TFT 12. The power control circuit 4 applies the power supply potential and an initialization potential to the p common power lines 9 in a
15 switching manner.

[0074] By thus applying the initialization potential to the common power lines 9 using the power control circuit 4, the initialization potential can be provided to the pixel circuits
20 10 from the power lines V_{Pi} . Accordingly, the number of elements in each pixel circuit 10 can be reduced. In addition, the power control circuit 4 drives the common power lines 9, each connected to two or more power lines V_{Pi} . Therefore, compared to the case of individually driving the power lines
25 V_{Pi} , the number of output buffers provided in the power control circuit 4 is reduced, making it possible to reduce the circuit size of the power control circuit 4.

[0075] In addition, the gate driver circuit 102 and the source driver circuit 3 (drive circuit) select initialized pixel
30 circuits 10 on a row basis, and control to allow each of the selected pixel circuits 10 to perform detection of a threshold

of the TFT 12, writing, and light emission in turn. Accordingly, the threshold voltage of the TFT 12 is compensated for and then a screen can be displayed.

[0076] In addition, the TFT 13 is placed in an on state upon initialization and the initialization potential is a potential at which the TFT 12 is placed in an on state when the potential is applied to the power line V_{Pi} upon initialization. Therefore, by controlling the TFT 13 to an on state by applying an initialization potential to the power line V_{Pi}, the initialization potential can be applied to the source terminal of the TFT 12. In addition, the TFT 13 is placed in an off state upon completion of initialization and is placed in an on state upon threshold detection. Accordingly, the pixel circuit 10 can be allowed to turn off during a period from the initialization to the threshold detection. In addition, upon threshold detection, by supplying a current from the power line V_{Pi}, the threshold of the TFT 12 can be detected. In addition, the TFT 13 is placed in an on state for a fixed period of time upon light emission. Accordingly, the lengths of the light emission periods of the pixel circuits 10 are made the same, making it possible to suppress variations in luminance. In addition, since the pixel circuits 10 turn off during periods other than the light emission period, moving image performance can be improved as in the case of performing black insertion.

[0077] In addition, each pixel circuit 10 includes a TFT 14 (reference potential application transistor) provided between the gate terminal of the TFT 12 and a wiring line having a reference potential V_{ref} (reference potential line). Therefore, by controlling the TFT 14 to an on state upon threshold detection, the reference potential V_{ref} is applied

to the gate terminal of the TFT 12 from the reference potential line, making it possible to detect a threshold of the TFT 12. In addition, since the TFT 14 can be controlled to an on state at any timing, a threshold detection period can be freely set.

5 [0078] In addition, according to the display device according to the first example (Fig. 4) that includes a single common power line 9, the number of output buffers provided in the power control circuit 4 is reduced to one, making it possible to reduce the circuit size of the power control circuit 4. In addition, 10 according to the display devices according to the second to fourth examples (Figs. 6, 8, and 10) that include a plurality of common power lines 9 and has power lines VPi provided for the respective rows of the pixel circuits 10, the number of output buffers provided in the power control circuit 4 is made 15 smaller than the number of power lines VPi, making it possible to reduce the circuit size of the power control circuit 4. In addition, by applying the initialization potential to the common power lines 9 at different timings, initialization of the pixel circuits 10 can be performed at suitable timing in 20 accordance with a selection period of the pixel circuits 10. By connecting a plurality of power lines VPi disposed adjacent to each other to each common power line 9, as in the display devices according to the second and fourth examples, writing can be performed to the pixel circuits 10 according to the order 25 on a display screen. By connecting a plurality of power lines VPi selected every predetermined number of lines according to the order of disposition to each common power line 9, as in the display device according to the third example, the amounts of current flowing through the common power lines 9 are made the 30 same, making it possible to prevent the occurrence of a

difference in luminance on a screen. In addition, all of the transistors included in the pixel circuit 10 are of an N-channel type. By thus configuring the transistors included in the pixel circuit 10 by the same conductive type of transistors, the cost of the display device can be reduced.

[0079] Note that the gate potential of the TFT 12 upon the start of initialization is a data potential written previously and thus is not constant. Therefore, to securely place the TFT 12 in an on state upon initialization, the low-level potential VP_L of the power line VPi needs to be sufficiently low. In addition, to securely place the TFT 12 in an on state upon initialization, a potential at which the TFT 12 is placed in an on state may be provided to the gate terminal of the TFT 12 from the data line Sj or the reference potential line and the TFT 11 or the TFT 14 may be controlled to an on state.

[0080] (Second Embodiment)

Fig. 12 is a block diagram showing a configuration of a display device according to a second embodiment of the present invention. A display device 200 shown in Fig. 12 includes a gate driver circuit 202 and pixel circuits 20 instead of the gate driver circuit 102 and the pixel circuits 10. Of the components of the present embodiment, the same components as those of the first embodiment are denoted by the same reference characters and description thereof is omitted.

[0081] In the display device 200, (n+1) control lines G0 to Gn are provided and n control lines Ei and n power lines VPi are provided parallel to the (n+1) control lines G0 to Gn. The control lines G0 to Gn and Ei are connected to the gate driver circuit 202. Though not shown, pixel circuits in an i-th row are also connected to a control line Gi-1 in a previous row.

The display device 200 does not include control lines R_i or wiring lines for a reference potential V_{ref} .

[0082] Fig. 13 is a circuit diagram of the pixel circuit 20. As shown in Fig. 13, the pixel circuit 20 includes TFTs 21 to 24, a capacitor 25, and an organic EL element 26. The pixel circuit 20 is connected to the control lines G_i and E_i , a control line G_{i-1} in a previous row, the data line S_j , a power line V_{Pi} , and an electrode having a common potential V_{com} . In the pixel circuit 20, the drain terminal of the TFT 24 is connected to the control line G_i and the gate terminal of the TFT 24 is connected to the control line G_{i-1} in the previous row. The configuration of the pixel circuit 20 is the same as that of a pixel circuit 10 except for the above-described points.

[0083] Fig. 14 is a timing chart showing a method of driving the pixel circuits 20. With reference to Fig. 14, the operation of the pixel circuits in the first row will be described below. The potential of the control line G_0 is at a high level at time t_{23} to t_{24} and is at a low level during other time. For the pixel circuits in the first row, the waveforms prior to time t_{23} are the same as those prior to time t_{13} in Fig. 3.

[0084] At time t_{23} , the potentials of the control lines G_0 and E_1 change to a high level. After time t_{13} , the TFTs 23 and 24 are placed in an on state and thus the potential of the control line G_1 is applied to the gate terminal of a TFT 22. At this time point, the potential of the control line G_1 is at a low level (hereinafter, the low-level potential of the control line G_i is referred to as V_{G_L}) and thus the potential V_{G_L} is applied to the gate terminal of the TFT 22. The potential V_{G_L} is determined such that the TFT 22 is placed in an on state immediately after time t_{23} and the voltage applied to the

organic EL element 26 does not exceed a light emission threshold voltage after time t_{23} . Hence, after time t_{23} , the TFT 22 is placed in an on state but a current does not flow through the organic EL element 26. Therefore, a current flows into the source terminal of the TFT 22 from the power line VP1 through the TFT 23 and the TFT 22 and thus the source potential VS1 of the TFT 22 rises. The source potential VS1 of the TFT 22 rises until the gate-source voltage Vgs becomes equal to the threshold voltage Vth, and reaches (Vref-Vth).

[0085] At time t_{24} , the potentials of the control lines G0 and E1 change to a low level, the potential of the control line G1 changes to a high level, and the potential of the data line Sj (not shown) reaches a data potential Vda. After time t_{24} , the TFTs 23 and 24 are placed in an off state, the TFT 21 is placed in an on state, and the gate potential VG1 of the TFT 22 changes from Vref to Vda. For the pixel circuits in the first row, the waveforms after time t_{24} are the same as those after time t_{17} in Fig. 3.

[0086] As such, in the pixel circuit 20, compared to the pixel circuit 10 according to the first embodiment, the control line Ri and the control line Gi are commonized. Pixel circuits in an i-th row perform threshold detection during a selection period of pixel circuits in an (i-1)-th row (a period during which the potential of a control line Gi-1 is at a high level). During the threshold detection period, the reference potential is applied to the gate terminals of the TFTs 22 from a control line Gi.

[0087] As described above, in the display device 200 according to the present embodiment, a pixel circuit 20 includes a TFT 24 (reference potential application transistor) that is

provided between the gate terminal of a TFT 22 (driving transistor) and a control line G_i connected to a TFT 21 (write control transistor), and that has a gate terminal connected to a control line G_{i-1} provided for pixel circuits in another row.

5 Therefore, by controlling the TFT 24 to an on state upon threshold detection, a reference potential is applied to the gate terminal of the TFT 22 from the control line G_i , making it possible to detect a threshold of the TFT 22. In addition, the numbers of wiring lines for the reference potential V_{ref} and of control lines for the TFTs 24 can be reduced over the
10 first embodiment.

[0088] Note that although in the pixel circuit 20 the gate terminal of the TFT 14 is connected to the control line G_{i-1} in the previous row, the gate terminal of the TFT 14 may be
15 connected to a control line G_{i-x} in an x -th previous row (x is an integer not smaller than 1). A display device according to this variant can also obtain the same advantageous effects.
[0089] (Third Embodiment)

Fig. 15 is a block diagram showing a configuration of a
20 display device according to a third embodiment of the present invention. A display device 300 shown in Fig. 15 includes a gate driver circuit 302 and pixel circuits 30 instead of the gate driver circuit 102 and the pixel circuits 10. Of the components of the present embodiment, the same components as
25 those of the first embodiment are denoted by the same reference characters and description thereof is omitted.

[0090] In the display device 300, n control lines E_i and n power lines V_{Pi} are provided parallel to n control lines G_i . The control lines G_i and E_i are connected to the gate driver circuit
30 302. The display device 300 does not include control lines R_i

or wiring lines for a reference potential V_{ref} .

[0091] Fig. 16 is a circuit diagram of the pixel circuit 30. As shown in Fig. 16, the pixel circuit 30 includes TFTs 31 to 33, a capacitor 35, and an organic EL element 36. The pixel circuit 30 is connected to the control lines G_i and E_i , the data line S_j , a power line VP_i , and an electrode having a common potential V_{com} . The pixel circuit 30 does not include a TFT (reference potential application transistor) corresponding to the TFT 14. The configuration of the pixel circuit 30 is the same as that of the pixel circuit 10 except for the above-described points.

[0092] Fig. 17 is a timing chart showing a method of driving the pixel circuits 30. With reference to Fig. 17, the operation of pixel circuits in the first row will be described below. For the pixel circuits in the first row, the waveforms prior to time t_{33} are the same as those prior to time t_{13} in Fig. 3.

[0093] At time t_{33} , the potentials of the control lines G_i and E_i change to a high level. After time t_{33} , the TFTs 31 and 33 are placed in an on state and the potential of the data line S_j is applied to the gate terminal of the TFT 32. At time t_{33} to t_{34} , a reference potential V_{ref} is applied to the data line S_j (not shown). Hence, the reference potential V_{ref} is applied to the gate terminal of the TFT 32. The reference potential V_{ref} is determined such that the TFT 32 is placed in an on state immediately after time t_{33} and the voltage applied to the organic EL element 36 does not exceed a light emission threshold voltage after time t_{33} . Hence, after time t_{33} , the TFT 32 is placed in an on state but a current does not flow through the organic EL element 36. Therefore, a current flows into the source terminal of the TFT 32 from the power line VP_i through

the TFT 33 and the TFT 32 and thus the source potential VS1 of the TFT 32 rises. The source potential VS1 of the TFT 32 rises until the gate-source voltage Vgs becomes equal to the threshold voltage Vth, and reaches (Vref-Vth).

5 [0094] At time t34, the potential of the control line E1 changes to a low level and the potential of the data line Sj changes to a data potential Vda. After time t34, the TFT 33 is placed in an off state and the gate potential VG1 of the TFT 32 changes from Vref to Vda. For the pixel circuits in the first row, the
10 waveforms after time t34 are the same as those after time t17 in Fig. 3.

[0095] As such, compared to the pixel circuit 10 according to the first embodiment, the pixel circuit 30 does not include a transistor for providing a reference potential to the gate
15 terminal of the TFT 32. Pixel circuits in an i-th row perform threshold detection and writing during a selection period of the pixel circuits in the i-th row (a period during which the potential of a control line Gi is at a high level). During the threshold detection period, a reference potential is applied
20 to the gate terminal of the TFT 32 from the data line Sj.

[0096] As described above, in the display device 300 according to the present embodiment, upon threshold detection, a reference potential is applied to a data line Sj and a TFT 31 (write control transistor) is placed in an on state. Therefore,
25 upon threshold detection, by controlling the TFT 31 to an on state, a reference potential is applied to the gate terminal of a TFT 32 (driving transistor) from the data line Sj, making it possible to detect a threshold of the TFT 32. In addition, without adding a transistor or a wiring line, the reference
30 potential can be provided to the pixel circuit 30 from the data

line Sj.

[0097] Note that although in the description made so far a threshold detection period is inserted immediately before a write period, the present invention is not limited thereto. It is also possible to provide a threshold detection period in any period prior to a selection period of pixel circuits to be selected just before.

[0098] As described above, according to the present invention, a display device can be obtained that has a configuration in which an initialization potential is provided to pixel circuits from power lines and that has a power control circuit small in circuit size.

INDUSTRIAL APPLICABILITY

[0099] Display devices of the present invention have features that the display devices have a configuration in which an initialization potential is provided to pixel circuits from power lines, and have a power control circuit small in circuit size, and thus, can be used as display devices using current-driven elements such as organic EL displays.

DESCRIPTION OF REFERENCE CHARACTERS

[0100] 1: DISPLAY CONTROL CIRCUIT

102, 202, and 302: GATE DRIVER CIRCUIT

25 3: SOURCE DRIVER CIRCUIT

4: POWER CONTROL CIRCUIT

5: SHIFT REGISTER

6: REGISTER

7: LATCH CIRCUIT

30 8: D/A CONVERTER

9, 111, 121, 122, 131, 132, and 141 to 143: COMMON POWER
LINE

10, 20, and 30: PIXEL CIRCUIT

11, 21, and 31: TFT (WRITE CONTROL TRANSISTOR)

5 12, 22, and 32: TFT (DRIVING TRANSISTOR)

13, 23, and 33: TFT (LIGHT EMISSION CONTROL TRANSISTOR)

14 and 24: TFT (REFERENCE POTENTIAL APPLICATION
TRANSISTOR)

15, 25, and 35: CAPACITOR

10 16, 26, and 36: ORGANIC EL ELEMENT (ELECTRO-OPTIC
ELEMENT)

100, 200, and 300: DISPLAY DEVICE

Gi, Ri, and Ei: CONTROL LINE

Sj: DATA LINE

15 VPi: POWER LINE

CLAIMS

1. A current-driven type display device, comprising:
a plurality of pixel circuits arranged
5 two-dimensionally;

a plurality of control lines provided for respective rows
of the pixel circuits;

a plurality of data lines provided for respective columns
of the pixel circuits;

10 a plurality of power lines provided to supply a power
supply potential to the pixel circuits;

a single or a plurality of common power lines, each
connected to two or more of the power lines;

a drive circuit that drives the control lines and the data
15 lines; and

a power control circuit that drives the power lines,
wherein

each of the pixel circuits includes:

an electro-optic element;

20 a driving transistor provided on a path of a current
flowing through the electro-optic element;

a write control transistor provided between a
control terminal of the driving transistor and a corresponding
one of the data lines;

25 a light emission control transistor provided
between one conduction terminal of the driving transistor and
a corresponding one of the power lines; and

a capacitor provided between an other conduction
terminal and the control terminal of the driving transistor,

30 and

the power control circuit applies the power supply potential and an initialization potential to the common power line(s) in a switching manner.

- 5 2. The display device according to claim 1, wherein the drive circuit selects initialized pixel circuits on a row basis, and controls to allow each of the selected pixel circuits to perform detection of a threshold of the driving transistor, writing, and light emission in turn.

10

3. The display device according to claim 2, wherein the light emission control transistor is placed in an on state upon initialization, and

15 the initialization potential is a potential at which the driving transistor is placed in an on state when the potential is applied to the power line upon initialization.

4. The display device according to claim 3, wherein the light emission control transistor is placed in an off state upon completion of the initialization and is placed in an on state upon threshold detection.

20

5. The display device according to claim 4, wherein the light emission control transistor is placed in an on state for a fixed period of time upon light emission.

25

6. The display device according to claim 2, wherein each of the pixel circuits further includes a reference potential application transistor provided between the control terminal of the driving transistor and a reference potential line.

30

7. The display device according to claim 2, wherein each of the pixel circuits further includes a reference potential application transistor that is provided between the control terminal of the driving transistor and a control line connected to the write control transistor, and that has a control terminal connected to a control line provided for pixel circuits in another row.

8. The display device according to claim 2, wherein upon threshold detection, a reference potential is applied to the data line and the write control transistor is placed in an on state.

9. The display device according to claim 1, comprising a single common power line.

10. The display device according to claim 1, comprising a plurality of common power lines, wherein

the power lines are provided for the respective rows of the pixel circuits, and

the power control circuit applies the initialization potential to the common power lines at different timings.

11. The display device according to claim 10, wherein a plurality of power lines disposed adjacent to each other are connected to each of the common power lines.

12. The display device according to claim 10, wherein a plurality of power lines selected every predetermined number

of lines according to order of disposition are connected to each of the common power lines.

13. The display device according to claim 1, wherein all of
5 the transistors included in the pixel circuit are of an N-channel type.

14. A method of driving a current-driven type display device including a plurality of pixel circuits arranged
10 two-dimensionally; a plurality of control lines provided for respective rows of the pixel circuits; a plurality of data lines provided for respective columns of the pixel circuits; a plurality of power lines provided to supply a power supply potential to the pixel circuits; and a single or a plurality
15 of common power lines, each connected to two or more of the power lines, the method comprising the steps of:

when each of the pixel circuits includes: an electro-optic element; a driving transistor provided on a path of a current flowing through the electro-optic element; a write
20 control transistor provided between a control terminal of the driving transistor and a corresponding one of the data lines; a light emission control transistor provided between one conduction terminal of the driving transistor and a corresponding one of the power lines; and a capacitor provided
25 between an other conduction terminal and the control terminal of the driving transistor,

applying, using a power control circuit, the power supply potential and an initialization potential to the common power line(s) in a switching manner;

30 controlling states of the transistors included in the

pixel circuits by driving the control lines; and
applying potentials corresponding to display data to the
data lines.