

CIRCUIT AND TEST METHOD

Abstract of the Disclosure

5 A circuit (100) comprises a built-in test circuit (150) which verifies the proper
operation of input cells (130) when they receive signals at a first level (71) and at a second
level (72). The test circuit (160) comprises a first and a second logic (110, 120) which
receive power only when a test is performed. Thereby power consumption of the test
circuit (160) is reduced. The first and the second logic (110, 120) are conveniently formed
10 by a combination of parallel coupled transistors acting in an logical OR-function.

Fig. 2 accompanies this abstract.