Semiconductor Device with High-k Gate Dielectric and Quasi-Metal Gate, and Method of Forming Thereof

[0001] This application claims the benefit of U.S. Provisional Application No. 60/590,060, filed on July 21, 2004, entitled "Semiconductor Device with High-k Gate Dielectric and Quasi Metal Gate," which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] This invention and the various embodiments described generally relate to the fabrication of semiconductor devices, and more particularly to transistors having high-k gate dielectrics.

BACKGROUND

[0003] In the semiconductor art, it is desirable to improve transistor performance even as devices become smaller due to ongoing scaling. Reduced device scaling with conventional gate dielectrics creates problems in manufacturing reliable MOS transistors, including short channel effects (SCE). It is known in the prior art to use high-k dielectric materials as the gate dielectric material to improve device performance. For purposes of this description, a high-k dielectric is a material having a dielectric constant k greater than that of silicon dioxide, the traditional dielectric material, which has a dielectric constant of approximately 3.9. Materials with a dielectric constant of greater than 3.9 are said to be "high-k" dielectrics. High-k dielectrics provide a similar equivalent oxide thickness (EOT) to larger scaled devices while using a reduced actual dielectric thickness, which meets the reduced scaling requirements of advanced CMOS processes. The use of such materials creates additional problems, however, in the

manufacturing and reliability of the transistor devices, including a threshold voltage (V_t) variability in the MOS transistors, particularly of p-type MOS transistors, which makes commercial devices using the high-k dielectric materials less desirable. Further, reduction in scale and the use of certain desirable high-k dielectric materials on silicon substrates is believed to contribute to a reported degradation in carrier mobility, which has a negative effect on the performance of transistors manufactured using these materials.

[0004] A paper entitled "A Highly Manufacturable Low Power and High Speed HfSiO CMOS FET with Dual Poly-Si Gate Electrodes," by Iwamoto et al., International Electronics Devices Meeting of the IEEE (IEDM), December 2003, describes a MOSFET of the p-type which uses a particular high-k gate dielectric material, HfSiO, over a silicon substrate, and describes the use of certain sidewalls and a channel controlling step to improve the V_t variability effects. This paper describes the threshold voltage shift problem particularly observed in p-type MOS transistors that are fabricated using high-k dielectric materials.

[0005] A paper entitled "Fermi Level Pinning at the PolySi/Metal Oxide Interface", by Hobbs et al., 2003 Symposium on VLSI Technology Digest of Technical Papers, describes the role of the poly Si/metal oxide interface on threshold voltage and how it influences poly Si depletion.

[0006] A paper entitled "55 nm High Mobility SiGE(:C) pMOSFETS with HfO_2 Gate Dielectric and TiN Metal Gate for Advanced CMOS," by Weber et al., 2004 Symposium on VLSI Technology, Digest of Technical Papers, describes the improved transistor performance obtained for a pMOS transistor fabricated using a SiGe channel material grown by epitaxial deposition of a compressively strained SiGe layer, with a high-k gate dielectric of HfO_2, and a metal gate electrode of TiN, having improved carrier mobility and improved V_t

[0007] A paper entitled "Mobility Enhancement in Surface Channel SiGe PMOSFETs with HfO_2 Gate Dielectrics", by Shi et al., IEEE Electron Device Letters, Vol. 24, No. 1, January 2003, describes PMOS transistors fabricated using strained SiGe as the channel layer and HfO_2 as the dielectric, the paper describes enhanced mobility for the devices over conventional silicon devices but also describes a variance in the threshold voltages.

[0008] A paper entitled " <100> Strained SiGe Channel p MOSFET with Enhanced Hole Mobility and Lower Parasitic Resistance", by Shima, Fujitsu Science and Technology Journal 39, Vol. 1, pp. 78-83 (June 2003), describes results obtained in carrier mobility experiments with strained SiGe as a channel material in PMOS devices.

[0009] The need for a process and apparatus for a producible, enhanced performance, scalable MOS transistor with a high-k gate dielectric thus exists. These needs are addressed in the present invention.

SUMMARY OF THE INVENTION

[0010] Various embodiments of the present invention provide a novel process and structure for a planar MOS transistor using a high-k gate dielectric material and a doped gated electrode material.

[0011] A process and apparatus for a semiconductor device is provided. A preferred semiconductor device comprises a first and second transistor. The first transistor has a first conductive channel, wherein the first transistor comprises a high-k gate dielectric and a first doped electrode. Preferably, the first conductive channel comprises one of p-type and n-type and the first doped electrode comprises the other of p-type and n-type. The second transistor has a second conductive channel opposite the first conductive channel. Preferably, the second transistor comprises the high-k gate dielectric, and a second doped electrode, wherein the second doped electrode comprises the other of p-type and n-type.

[0012] An alternative semiconductor comprises at least one n-channel device having a high-k gate dielectric and at least one p-channel device having a high-k gate dielectric. Preferably, the n-channel device and the p-channel device have the same doping type of the gate. Preferably, the gate doping concentration is different for the n-channel device and for the p-channel device.

[0013] In preferred embodiments of the invention, the dielectric layer comprises an oxide such as SiO_2 or a nitrided oxide such as SiON. In another preferred embodiment, the dielectric layer comprises a high-k dielectric, preferably a hafnium or an aluminum-based dielectric. Nitrides and high-k dielectric stacks may be used as the dielectric including Si, O, and N. Tantalum (Ta) or lanthanum (La) oxides, aluminates, aluminum oxide and/or nitrides, combination or stacked dielectrics and other known high-k dielectrics may be used.

[0014] A preferred embodiment of the invention comprises an n-channel transistor having a hafnium-based, high-k gate dielectric and a p+ polysilicon gate electrode. Another preferred embodiment comprises a p-channel transistor having an aluminum-based, high-k gate dielectric and an n+ poly gate. In other embodiments, an NMOS and PMOS device may independently include an n+ or p+ doped poly gate. In still other embodiments, an NMOS and PMOS device may independently include a gate dielectric comprising Hf, Al, silicon oxide, nitrided silicon oxide, and combinations thereof.

[0015] Embodiments of the invention avoid too large a threshold voltage for PMOS with n+ doped poly gate and for NMOS with p+ doped poly gate. A net concentration of n-type poly dopants in PMOS is preferably at least two times smaller than a net concentration of n-type dopants in NMOS. Such a doping reduces the threshold voltage for PMOS with an n+ doped poly gate. For the same reason, a net concentration of p-type poly dopants in NMOS is preferably at least two times smaller than a net concentration of p-type dopants in PMOS.

[0016] Another method for threshold voltage reduction includes forming a counter-doping channel. Embodiments may include a strained channel region beneath the dielectric material. Optionally this channel material may be counter doped to further provide enhanced transistor performance. For example, counter doping by implantation or SiGe may be introduced if the threshold voltage for either NMOS or PMOS devices is too large. In another embodiment, an integrated circuit having both core and peripheral areas may be defined on a substrate, wherein processing steps in the core and peripheral areas may be asymmetric. The substrate may comprise a silicon-on-insulator (SOI), alternatively the substrate may comprise SiGe, Ge, strained Si, strained Ge or a combination or stacked arrangement of Si/SiGe layers. In another

embodiment, a metal gate electrode or a combination material including a metal may be used for the gate electrode.

[0017] Preferred embodiments of the invention advantageously limit poly gate depletion. Such advantages achieve thinner EOT and higher performance such as are normally achieved with metal gates. In this way, desired metal gate properties are achieved in embodiments of the invention.

[0018] Additional features and advantages of embodiments of the invention will be described hereinafter, which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the specific embodiments disclosed might be readily utilized as a basis for modifying or designing other structures or processes for carrying out the purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions and variations on the example embodiments described do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0020] Figure 1 depicts a cross-sectional view of a substrate prior to isolation trench formation including a deposited oxide and a deposited nitride layer;

[0021] Figure 2 depicts a cross-sectional view of the substrate following the trench isolation formation and oxide deposition;

[0022] Figure 3 depicts a cross-sectional view of the substrate following the trench isolation formation and subsequent planarization and following deposition of the high-k gate dielectric;

[0023] Figure 4 depicts the substrate following deposition of a gate electrode material over the high-k gate dielectric and following the formation of a pattern mask material;

[0024] Figure 5 depicts the substrate following the patterning of the gate electrode material by etching the gate electrode material and the high-k gate dielectric using the mask material; and

[0025] Figure 6 depicts the substrate following the completion of transistors having source and drain regions aligned to the gate electrodes of Figure 5.

[0026] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0027] The operation and fabrication of the presently preferred embodiments are discussed in detail below. However, the embodiments and examples described herein are not the only applications or uses contemplated for the invention. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention or the appended claims.

[0028] Figure 1 depicts a cross sectional view of a semiconductor device 100 not drawn to scale, but drawn as an illustration only. Semiconductor substrate 101 will provide the basic material for the manufacture of the device. The semiconductor substrate 101 includes silicon, germanium, strained silicon, strained germanium, silicon germanium or SOI substrate, or their combination substrate. Silicon substrate can be epitaxial silicon on silicon and SOI. Germanium substrate includes epitaxial silicon germanium on silicon. The substrate 101 is shown with a pad oxide layer 103 and a nitride layer 105 deposited over it using typical deposition processes, for example the depositions may be a chemical vapor deposition, a plasma enhanced deposition, or any other blanket deposition known in the art, such as reduced pressure CVD or others.

[0029] Figure 2 depicts the device 100 after the nitride layer 105 and pad oxide layer 103 are patterned and etched using photolithography techniques to form a hardmask, then an etch is performed and the hardmask is removed, the etch may be for example an HF or piranha etch, an STI oxide 108 is then conformally deposited. The trenches 107 may be about 1000-5000 Angstroms deep or more or less, in an example the completed STI trenches were 2000 Angstroms deep. The STI oxide 108 may be deposited using high density plasma (HDP) or

other techniques, for example sub-atmospheric chemical vapor deposition (SACVD) may be used.

[0030] Figure 3 depicts the device 100 following the removal of the excess trench oxide, the nitride oxide layer 105 and the pad oxide layer 103, and the deposition of a gate dielectric layer 110. In the removal steps, chemical mechanical polishing (CMP) processes are used to chemically and mechanically remove the trench oxide, nitride, and pad oxide layers to complete the oxide filled shallow trench isolation regions 107 which extend to, or even above, the surface of the substrate. Following the CMP and a clean up step, in a first preferred embodiment of the method of the invention, a high-k gate dielectric 110 is deposited directly onto the substrate 101 and the STI regions 107. In a second preferred embodiment of the method of the invention, an interfacial layer 111 is thermally grown onto the substrate 101 and then the high-k gate dielectric 110 is deposited onto the interfacial layer 111.

[0031] Deposition of the dielectric material may be performed by conventional methods including remote plasma CVD (RPCVD), plasma enhanced CVD (PECVD), atomic layer deposition (ALD), MOCVD, PVD, sputtering or other methods known in the art. High-k dielectrics are those dielectrics that have a dielectric constant k of greater than silicon dioxide, about 3.9. Possible high-k dielectrics substantially include silicon nitride, tantalum pentoxide, hafnium oxide, hafnium silicon oxynitride, aluminum oxide, lanthanum oxides, and other high-k dielectric materials known in the art. A range of dielectric constant materials is known, for example for the range of $3.9<k<9$, the high-k gate dielectric may include oxy-nitride, oxygen containing dielectrics, nitrogen containing dielectrics, combinations of these and multiple layers of these. For $k > 9.0$, the dielectrics may include any of HfO_2, $HfSiO_x$, zirconium oxide such as ZrO_2, aluminum oxide such as Al_2O_3, titanium oxide such as TiO_2, tantalum pentoxide,

lanthanum oxide such as La_2O_3, barium strontium compounds such as BST, lead based compounds such as $PbTiO_3$, similar compounds such as $BaTiO_3$, $SrTiO_3$, $PbZrO_3$, PST, PZN, PZT, PMN, metal oxides, metal silicates, metal nitrides, combinations and multiple layers of these.

[0032] In preferred embodiments, the high-k dielectric includes HfSiON, preferably amorphous HfSiON. The dielectric region may further include Si, Ge, F, C, B, O, Al, Ti, Ta, La, Ce, Bi, and W, for example. The dielectric layer is typically fairly thin, for example 1-100 Angstroms. In one example a high-k dielectric layer of HfSiON was deposited to about 40 Angstroms thickness and having an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.

[0033] Figure 4 depicts the device 100 following the deposition of gate electrode material 112 over the high-k gate dielectric 110 and the formation of a patterned mask 114 for use in etching the gate electrodes. The gate electrode material 112 may be of polysilicon, doped polysilicon, metal compositions such as titanium nitride (TiN), silicides, or other metal gate electrode materials used in the art. A metal gate with a work function of greater than or equal to 1 may be used.

[0034] In a preferred embodiment, the gate electrode material 112 is a doped polysilicon gate electrode material. The electrode may be deposited, for example, by a conventional CVD process to a thickness less than about 1000 Angstroms. In preferred embodiments, the gate electrode includes a dopant of a first conductivity type, while the device source and drain regions include a dopant having a second conductivity type. In preferred embodiments, the second conductivity type is opposite to the first conductivity type. For example, for a PMOS or p-channel device, the PMOS gate electrode is preferably n+ doped, while for an NMOS or n-

channel device, the NMOS gate electrode is preferably p+ doped. The n+ poly-Si gate or n-type gate is preferably doped with a 25 keV, $1x10^{15}$ cm^{-2} implant dose of phosphorus. The p+ poly-Si gate or p-type gate is preferably doped with a 10 keV $3.5x10^{15}$ cm^{-2} implant dose of boron. A spike activation anneal is done at approximately at 1050 °C. In this situation, conductive channels of NMOS and PMOS transistors in the substrate are counter doped using conventional methods, such as ion implantation. Typically a boron dopant is used to counter dope the channel for a PMOS transistor. Other dopants that can be used are Al, Ga, and In for p-channels. On the other hand, typically a phosphorus dopant is used to counter dope the channel for an NMOS transistor. Other dopants that can be used are N, As, and Sb for n-channels.

[0035] In alternative preferred embodiments, the n-channel device and the p-channel device have the same doping type of the gate, and the gate doping concentrations of the n-channel and the p-channel devices are different respectively. For example, the gate doping concentration of an n-type gate in an n-channel device is higher than that of a p-channel device. Alternatively, the gate doping concentration of a p-type gate in a p-channel device is higher than that of an n-channel device.

[0036] Electrodes may be conventionally doped *in situ* with conventional dopants. Preferred n-type dopants, include antimony, phosphorous, or arsenic, for example. Examples of preferred p-type dopants include boron, aluminum, gallium, or indium.

[0037] The hard mask 114 defines areas for forming transistor gate electrodes over the substrate, and areas for making connectivity at the polysilicon level over the STI regions 107. The formation of the gate electrode material 112 will not create an active device over the STI regions 107 (as there is no active silicon area for receiving subsequent source and drain diffusions) but instead provides additional connectivity areas to those portions of the gate

electrodes, which may in fact overly other active areas in the substrate in regions that are not visible in the cross section of the figure.

[0038] Figure 5 depicts the device 100 in the same cross sectional view as in the prior figures following an etch step which patterns the gate electrode material 112, the high-k gate dielectric 110 and the interfacial layer 111. The etch is then allowed to continue into the substrate 101 and into the STI regions 107, to extend the etched region to a depth which lies below the bottom of the high-k gate dielectric 110. In figure 5 the substrate 101 is shown removed to a depth below the bottom of the high-k gate dielectric 110 by some amount, the etch used is also highly selective for the STI oxide and removes significantly more of the STI oxide 108 than it does of the silicon substrate 101.

[0039] Figure 6 depicts the substrate 101 of the device 100 in accordance with a preferred embodiment of the present invention after sidewalls 120 are deposited and patterned on either side of the gate electrodes 112 and gate dielectric 110.

[0040] Sidewall spacer 120 is deposited using a dielectric to provide a protective spacer over the sidewalls of the electrode and extending beneath the bottom of the high-k dielectric 110. The sidewall is preferably nitrogen containing oxide or silicon nitride material, and may be deposited by low temperature deposition techniques including PECVD and remote plasma CVD (RPCVD). The sidewall spacers 120 may comprise silicon nitride or silicon oxynitrides. In a preferred embodiment the oxide or nitride sidewall spacer may be some 40 Angstroms wide. In an example the sidewall spacer is SiO_xN_y. A lightly doped drain (LDD) may be formed in the substrate areas using ion implantation as is known in the conventional art prior to the sidewall spacer region formation described here.

[0041] Figure 6 further depicts the formation of source and drain diffusions 122 and 124 which are formed in the substrate areas using ion implantation and thermal anneal procedures as are known in the conventional art. In this figure source and drain diffusions 122 and 124 with a lightly doped drain structure are shown. The gate electrode 112, gate dielectric 110, and the source and drain diffusions 122, 124 together form a planar MOS transistor. Depending on the type of dopants used in the source and drain and the substrate, the transistors may be of a p-type MOS transistor or an n-type MOS transistor. In CMOS device 100, the transistors may be formed in well diffusions (not shown) that were performed prior to the STI region formation described here, as is known in the art, the wells being isolated by the STI regions.

[0042] Therefore, the semiconductor device 100 comprises a first transistor having a first conductive channel, the first transistor comprises a high-k gate dielectric and a first doped electrode, the first conductive channel comprises one conductive typeof p-type and n-type and the first doped electrode comprises the other conductive type of p-type and n-type, that is, the first conductive channel and the first doped electrode have different conductive types The semiconductor device 100 also comprises a second transistor having a second conductive channel opposite the first conductive channel, the second transistor comprises the high-k gate dielectric, and a second doped electrode, the second doped electrode and the first doped electrode have the same conductive type. At least one of the first and second transistor comprises a counter doping conductive channel. In this situation, the conductive channels of NMOS and PMOS transistors in the substrate are counter doped using conventional methods, such as ion implantation. The counter doping conductive channel for a PMOS transistor is p-type. Typically a boron dopant is used to counter dope the channel for a PMOS transistor. Other dopants that can be used are Al, Ga, and In for p-channels. On the other hand, the counter doping conductive

channel for an NMOS transistor is n-type. Typically a phosphorus dopant is used to counter dope the channel for a NMOS transistor. Other dopants that can be used are N, As, and Sb for n-channels.

[0043] Following the steps described so far to form the cross section shown in Figure 6, the integrated circuit is completed using conventional semiconductor processing steps as are known in the art; for example silicide may be formed by depositing a metal such as titanium or cobalt and then treated to form self-aligned silicide, or salicide, on top of the gate electrode 112, the source and drain regions 122, 124, and other areas to provide a lower resistance and improve device performance, however this step is optional. Following the salicide step, if used, interlevel insulation layers are formed above the substrate using deposition steps to deposit oxide, nitride or other conventional insulation layers, typically silicon dioxide is formed. Contact areas are patterned and etched into the insulators to expose the source, drain, and gate electrodes, the resulting vias are filled with conductive material to provide electrical connectivity from metallization layers above the interlevel insulating layers down to the gate electrodes, the source and the drain regions. Metallization layers of aluminum or copper, may be formed over the interlevel insulation layers using known techniques such as an aluminum metallization process or a dual damascene copper metallization process to provide one, or several, wiring layers that may contact the vias and make electrical connections to the gate electrodes 112 and the source and drain regions 122, 124. Conventional clean up, passivation, die saw, singulation, packaging, assembly and test steps are used to complete the integrated circuit devices formed on the substrate 101.

[0044] The embodiments of the invention described above are exemplary and not limiting and variations that are apparent to those skilled in the art that include the features of the invention are within the scope of the invention and the appended claims.

[0045] Although embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, it will be readily understood by those skilled in the art that many of the features, functions, processes, and materials described herein may be varied while remaining within the scope of the present invention. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first transistor having a first conductive channel, wherein the first transistor comprises a high-k gate dielectric and a first doped electrode, wherein the firstconductive channel comprises one of p-type and n-type and the first doped electrode comprises the other of p-type and n-type; and

a second transistor having a second conductive channel opposite the first conductive channel, wherein the second transistor comprises the high-k gate dielectric, and a second doped electrode, wherein the second doped electrode comprises the other of p-type and n-type.

2. The semiconductor device according to claim 1, wherein the high-k gate dielectric comprises a material having a gate dielectric constant greater than 3.9.

3. The semiconductor device of claim 1, wherein the high-k gate dielectric comprises aluminum oxide.

4. The semiconductor device of claim 1, wherein the high-k gate dielectric comprises hafnium oxide.

5. The semiconductor device of claim 1, wherein an effective oxide thickness for the high-k gate dielectric is less than about 2 nm.

6. The semiconductor device of claim 1, wherein the first transistor comprises an n-channel transistor, the second transistor comprises a p-channel transistor, and the first and second doped electrodes comprise p-type.

7. The semiconductor device of claim 1, wherein the first transistor comprises a p-channel transistor, the second transistor comprises an n-channel transistor, and the first and second doped electrodes comprise n-type.

8. The semiconductor device of claim 1, wherein the high-k gate dielectric comprises a material selected from the group consisting essentially of silicon, silicon nitride, tantalum, lanthanum, hafnium, aluminum, oxides, and combinations thereof.

9. The semiconductor device of claim 1, wherein the first and second doped electrodes comprise a material selected from the group consisting essentially of silicon, germanium, polysilicon, amorphous silicon, and combinations thereof.

10. The semiconductor device of claim 1, wherein at least one of the first transistor and the second transistor further comprise a counter doping channel formed under the high-k gate dielectric.

11. The semiconductor device according to Claim 10, wherein the counter doping channel comprises a material selected from the group consisting essentially of silicon, germanium, carbon, strained silicon, strained carbon, strained germanium, strained silicon germanium, and combinations thereof.

12. A semiconductor device comprising: at least one n-channel device having a high-k gate dielectric and at least one p-channel device having a high-k gate dielectric, wherein the n-channel device and the p-channel device have the same doping type of gate, and wherein a gate doping concentration is different for the n-channel device and for the p-channel device.

13. The semiconductor device according to claim 12, wherein the high-k gate dielectric comprises a material having a gate dielectric constant greater than 3.9.

14. The semiconductor device of claim 12, wherein the high-k gate dielectric comprises aluminum oxide.

15. The semiconductor device of claim 12, wherein the high-k gate dielectric comprises hafnium oxide.

16. The semiconductor device of claim 12, wherein at least one of the n-channel device and the p-channel device further comprise a counter doping channel formed under the high-k gate dielectric.

17. The semiconductor device of claim 12, wherein an effective oxide thickness for the high-k gate dielectric is less than about 2 nm.

18. The semiconductor device of claim 12, wherein the n-channel device and the p-channel device have the same n-type gate, and the gate doping concentration of the n-type gate in the n-channel device is higher than that of the p-channel device.

19. The semiconductor device of claim 12, wherein the n-channel device and the p-channel device have the same p-type gate, and the gate doping concentration of the p-type gate in the p-channel device is higher than that of the n-channel device.