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Electronic circuit for timer applications having
5 minimal power consumption and methods for calibrating
and operating the same

The present invention relates to an externally
programmable electronic circuit which, after a
10 programmable time has lapsed, outputs an appropriate
output signal to prompt the execution of a prescribed
action, wherein the programming is effected by
modulating a carrier frequency. The invention also
relates to a method for calibrating and a method for
15 operating such a circuit.

The electronic circuit specified above, which is also
called an electronic timer circuit and today usually
has a microprocessor, is normally programmed digitally
20 via an interface using an amplitude modulated carrier
frequency method. The high-precision carrier frequency
used by an external programming appliance in this
context is quartz stabilized.

25 After the programming of such an electronic timer
circuit, i.e. after transmission, for example
inductive, and storage of the data for the time lapse
in the microprocessor, a short pause is followed by a
processor-internal or processor-external start signal
30 being output which represents the start of the lapse of
the programmed time. When this time has lapsed, a
digital output signal is produced which prompts further
action. Such an electronic timer circuit is used in a
detonation process, for example.

35 There is now the need for the programmed time to lapse
very precisely even though the microprocessor has only

one or more relatively imprecise RC oscillators (oscillator with RC element) available as a clock generator for the time lapse for other limiting reasons. By way of example, only relative time errors
5 of 100 ppm are permitted for the lapse of time, whereas the frequency precision of RC oscillators today is approximately 1 to 20%.

The document DE 195 25 202 C1 discloses a method for
10 programming an electronic detonator which achieves a high level of time precision. The known method involves calibration to the quartz precision carrier frequency delivered by the external programming appliance using a microprocessor-internal oscillator, the clock frequency
15 of which is more than a power of 10 above the external carrier frequency. Such a high clock frequency is customary for the operation of a microprocessor, since it is also used to clock the command execution. In addition, the high clock rate is necessary in order to
20 provide sufficiently precise time resolution for the calibration interval which forms the basis for the later time lapse. In the case of the known method for calibration, the programming involves the high precision carrier frequency of the programming
25 appliance in the electronic circuit being counted to a prescribed counter reading, and at the same time the relatively imprecise oscillator frequency of the circuit being counted. When the prescribed counter reading is reached for the high precision carrier
30 frequency, the counter reading reached with the imprecise oscillator frequency is stored in the electronic circuit as an internal time standard and used for executing the programmed time.

35 A continuously applied high processor clock rate, which is necessary for the known methods outlined above, generates a high power draw for the processor, however. This is disadvantageous for the execution of the programmed time, since during the lapse of the

programmed time the microprocessor is intended to be powered not from a battery but rather from capacitors or similar energy stores with low volume, which have been charged during the programming. It is therefore
5 desirable for the current draw by the microprocessor to be drastically reduced while maintaining the required maximum operating time and the necessary precision.

The object of the present invention is therefore to
10 provide a precisely operating electronic timer circuit which has drastically reduced current draw during the execution of the programmed time. Similarly, the object is to specify a method for calibrating an electronic circuit and a method for operating a programmable
15 electronic circuit which allow precise lapse of a programmed time and at the same time a reduction in the current draw.

The above object is achieved by an electronic circuit
20 which has not only the first oscillator but additionally a second oscillator as a clock generator, wherein the frequency of the second oscillator is lower than the frequency of the first oscillator. The electronic circuit also has means for carrying out the
25 calibration method explained below and for carrying out the method for operating the circuit which is explained below.

The above object is furthermore achieved by a method
30 for calibration in which the known carrier frequency is used to ascertain the present period duration (T) of the first oscillator and a ratio which corresponds to the ratio between the period duration of the first oscillator and the period duration of the second
35 oscillator.

The electronic circuit according to the invention furthermore implements a method for operation according to the invention in which after or during the

calibration of the circuit the time (t_p) is programmed by modulating the carrier frequency, wherein after termination of the calibration and a start signal the transmitted time lapses by virtue of an appropriate fourth period number of the second oscillator and an appropriate third period number of the first oscillator, which operates no more than intermittently in parallel, being counted off.

10 The present electronic circuit according to the invention and the methods according to the invention use the insight that the main cause of the high current draw is the clock oscillator (first oscillator) and the associated speed of the clocking of the internal
15 processor components. On account of the frequent charge reversal of parasitic capacitances which is necessary as a result, the power consumption of the microprocessor rises mostly linearly with rising clock frequency. This means that the clock frequency needs to
20 be reduced in order to lower the current draw. This is achieved in the case of the present invention for the use of the additional second, processor-external oscillator with a low frequency as a clock generator during the lapse of the programmed time. In one
25 preferred exemplary embodiment, the clock frequency of the second oscillator is below the external carrier frequency of the programming appliance by more than a power of ten in order to push the power consumption of the circuit into the microampere range.

30 Although the use of the second oscillator at a low clock frequency conflicts with the demand for a precise time lapse or a high time resolution for the calibration interval, the inventive combination of
35 oscillators which operate no more than intermittently in parallel at different frequencies and the inventive calibration achieve the required precision of the timer circuit for the lapse of the programmed time.

According to the invention, it is assumed that the quartz precision external carrier frequency is present for a short time span before, during and after the digital time programming. In one preferred exemplary embodiment, this carrier frequency may also be a carrier of energy in order to supply power to the entire circuit during and after the buffer-storage of the transmitted energy e.g. in capacitors, even after the programming has concluded. In the short time span during the programming and the calibration of the timer circuit, the invention provides sufficient energy for clocking the processor at a high clock frequency by virtue of the inductive coupling to the programming appliance. Accordingly, the circuit requires only the stored energy for the longest lasting phase of the time lapse while the fourth period number of the second oscillator is being counted off, and has a very modest mean power consumption.

In particular, for the much longer phase of the lapse of the programmed time, the invention provides an external RC oscillator or LC oscillator as the second oscillator, said oscillator operating at a very low clock frequency, preferably between approximately 1 kHz and approximately 10 kHz, for example 6 kHz, and undertaking the clocking of the processor during the majority of the lapse of the programmed time. This oscillator (subsequently called NFO) has a very low current draw, starts when the initialization phase starts and remains switch on during all the operating phases of the circuit according to the invention.

By contrast, the faster processor-internal oscillator (subsequently called RCO) is switched on only during the calibration and the transmission of the programmed time and also up to the start of the time lapse and for a short time beyond that and also at the end of the lapse of the programmed time. In this case, the RCO serves as a reference oscillator and clock oscillator

for the microprocessor and has a frequency of preferably between approximately 1 MHz and approximately 5 MHz. For the majority of the time the programmed time is lapsing, the processor-internal
5 oscillator RCO is switched off.

In a preferred method according to the invention for calibration, first of all a first period number for the first oscillator RCO is counted up to a counter
10 reading, which is prescribed by the carrier frequency and which corresponds to a prescribed time, and this is used to determine the ratio and therefore the present period duration of the first oscillator, then, starting at a starting edge of the second oscillator NFO, the
15 periods of the first oscillator RCO are counted, with the second oscillator NFO continuing to operate in parallel, until the first period number is reached by the first instant, and then a next ending edge, occurring after the first instant, of the second
20 oscillator NFO is detected, the direction of which can be determined in comparison with the starting edge, wherein a second period number for the first oscillator RCO is counted off in the period of time starting with the first instant and up to the ending edge being
25 reached, wherein the ratio between the first period number and the second period number and also the periods of the second oscillator which are counted between the starting and ending edges is obtained.

30 This calibration method is a particularly simple method which ensures that the programmed time lapses comparatively precisely and also that the second oscillator NFO can be used as a clock generator for a large proportion of the time during the lapse of the
35 programmed time.

Simple calculation, outlined in the exemplary embodiments, of the period ratio is made possible if, in one preferred exemplary embodiment, the starting

edge and the ending edge of the second oscillator NFO have the same direction and therefore the ratio is ascertained directly from the periods of the second oscillator NFO which are counted between the starting
5 and ending edges and the sum of the first and second period numbers of the first oscillator RCO.

In one particularly preferred exemplary embodiment of the calibration method, the third period number of the
10 first oscillator RCO and the fourth period number of the second oscillator NFO are calculated using the calculation method explained in more detail below.

In one preferred exemplary embodiment of the method for
15 operating an externally programmable electronic circuit, the third period number and the fourth period number are chosen such that the fourth period number of the periods of the second oscillator NFO is counted during the substantially greatest time component of the
20 programmed time, the first oscillator (RCO) being essentially switched off during the time component.

In a further preferred exemplary embodiment, the fourth
25 period number is ascertained from the number of whole periods of the second oscillator which are contained in the transmitted or programmed time less 1.

A particularly easily implementable lapse of the transmitted time is achieved in that after the start
30 signal first of all, when the first oscillator RCO and the second oscillator NFO are operating in parallel, a first lapse number of lapsed periods of the first oscillator, which number has lapsed after the start signal before an edge of the second oscillator has been
35 reached, is counted off, then the first oscillator RCO is switched off and the fourth period number of periods of the second oscillator NFO before the relevant edge of the second oscillator NFO is reached is counted off, when the just mentioned edge of the second oscillator

NFO has been reached the first oscillator RCO is switched on again, and finally the difference number of periods of the first oscillator RCO between the third period number, ascertained in the calibration, and the
5 first lapse number is counted off.

Further advantages, features and opportunities for application of the present invention can also be found in the description below of an exemplary embodiment and
10 the figures. In this case, all the features described and/or graphically presented form the subject matter of the present invention independently or in any combination, including irrespective of their summary in the claims or the back-references therein.

15

Schematically:

Figure 1 shows an electronic circuit based on the present invention,
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Figure 2 shows an illustration of the chronologically successive steps during calibration, programming and the lapse of the programmed time,
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Figure 3 shows a first step in the inventive calibration of the electronic circuit shown in figure 1,

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Figure 4 shows a second step in the inventive calibration of the electronic circuit shown in figure 1, and

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Figure 5 shows an illustration of the method according to the invention for operating the electronic circuit shown in figure 1 during the lapse of the programmed time.

Figure 1 shows the electronic circuit according to the invention with a microprocessor 1 which has the inputs A, B, C and D and the output F.

5 In addition, the microprocessor 1 has an input Ub provided on it which is used for supplying power. The microprocessor 1 has an internal clock generator (RC oscillator, RCO for short) which provides a processor-internal high clock frequency of 2.4 MHz, for example.
10 Furthermore, the microprocessor 1 contains a counting unit (timer) 2 which is connected either to the RCO or to the input D (and hence to the NFO) via a switch 3.

Another part of the electronic circuit according to the
15 invention is a second oscillator (NFO for short) having a clock frequency, which is 6 kHz, for example, which is lower in comparison with the RCO. The NFO is connected not only to the external clock input D of the processor 1 but also in parallel to the port input B of
20 the microprocessor 1, so that this input can also be used for program counter control for calibration to this clock too. The connection to the inputs B and D of the microprocessor 1 is made merely because in many processors the clock input D cannot be used as a port
25 or interrupt input internally.

In a further exemplary embodiment, it is possible to use a microprocessor in which the clock input D can also be used as a port or interrupt input. In this
30 case, the parallel connection of the NFO to a separate port input is not necessary.

During the programming of the circuit according to the invention, the quartz precision external carrier
35 frequency is applied to the input A of the microprocessor 1. In one preferred exemplary embodiment, the carrier frequency may also be an energy carrier in order to supply power to the entire circuit during and after the programming. This case is shown in

figure 1 by the dashed components. The signal for starting the lapse of the programmed time is input at the input C of the microprocessor 1.

- 5 When the programmed time has lapsed, the output F of the microprocessor 1 outputs a predetermined signal which prompts a further action, for example detonation.

The middle row in figure 2 shows the individual steps during initialization, calibration, programming, lapse of the programmed time, and ends with the defined signal being output to the output F of the microprocessor. In the top row, it can be seen which of the oscillators (RCO or NFO) is used as clock generator ('clock') for the microprocessor 1. In this context, in the regions which are denoted by the reference symbol 11, the RCO is the clock generator, whereas the oscillator NFO is the clock generator in the region 12. The bottom row 13 in figure 2 symbolizes by means of its extent or stretch when the external carrier frequency is applied to input A of the microprocessor 1 in the steps above that.

When the carrier frequency f_T , which is 200 kHz, for example, and is initially not yet modulated, has been switched on, the supply of power to the circuit begins and in the first phase 21 the subsystems of the microprocessor 1 are initialized. The direction of the progression of time is denoted by the arrow 10 in figure 2.

In the subsequent phase 22, in which the programming appliance initially continues to send an unmodulated carrier frequency f_T , a first calibration step - which is shown in more detail in figure 3 - is performed.

In this step 22, the processor 1 counts in a first counting operation up to a prescribed known number of oscillations i of the quartz precise carrier frequency

f_T at its input A, said oscillations corresponding to a time of $t_k = k \text{ ms}$ (see row K in figure 3). In one exemplary embodiment, $t_k = 8 \text{ ms}$. At the same time as the first counting operation starts, a second counting operation is initiated by the integrator timer 2 in the microprocessor 1 (cf. arrow 31 in figure 3). The second counting operation involves the clock cycles of the RCO being counted until the predefined number of i carrier oscillations has been reached after the time t_k (arrow 32). The RCO clock cycles counted during the time t_k , which have a period duration T_0 over the time t_k , are shown in row L in figure 3. The counter reading X on the timer 2 which is reached at the end of the second counting operation is stored in a memory - not shown - in the microprocessor 1 for further use. The counter reading X corresponds to the time t_k , measured in RCO clock cycles, and the current period duration T_0 of the first oscillator RCO can be ascertained from the ratio t_k/X .

After this first calibration step 22, the run time t_p is programmed in a step 23 as a digital word by modulating the carrier frequency f_T applied to input A of the microprocessor 1. In this case, the information for the run time t_p is transmitted as a digital value and is likewise stored in the memory - not shown - in the microprocessor 1.

In a further exemplary embodiment, the programming step 23 can also take place before the first calibration step 22.

In accordance with the invention, the programming step 23 is followed by a second calibration step 24, which is not shown in more detail in figure 4. On account of the performance of the preceding first calibration step 22, the external carrier frequency is no longer required for this step. It is therefore switched off in the course of step 24 (cf. end of row 13 in figure 2).

In the second calibration step 24, the microprocessor 1, which continues to be clocked at the RCO frequency, first of all awaits a first counting edge of the NFO clock, which is shown in row M in figure 4. When this appears (see arrow 33), two counting operations (third and fourth counting operations) in turn start. In a third counting operation, a program loop counts the NFO clock cycles supplied to port B, while the timer 2 counts the RCO clock cycles generated inside the processor. In this case, the NFO clock cycles are shown in row M in figure 4 and the RCO clock cycles are shown in row N in figure 4. When the timer 2 now in turn reaches the counter reading X after the time t_k , a flag is set in the program (symbolized in figure 4 by the arrows 34 and 35) and prompts the next counting edge of the NFO clock to arise after the flag to be used after n NFO clock cycles as a stop or takeover criterion for the continued counting of the RCO clock cycles (see arrow 36). After the step 24, an integer count n for the number of NFO clock cycles and the count reading X+Y, to which the timer 2 counted the RCO clock cycles during the n NFO clock cycles, are therefore available. These can be used to ascertain the ratio $V = n/(X+Y)$.

The available counter readings and values can now be used in step 25 by the microprocessor 1, which continues to be clocked at the RCO frequency, to calculate the parameters M and q for the lapse of the programmed time t_p , which is shown in figure 5.

For this, the programmed time t_p , which is intended to lapse before the predefined signal is output at the output F of the microprocessor 1 and which is available as an integer, for example, in milliseconds, is initially expressed by the calibration interval t_k :

$$t_p = at_k + bt_k/k \text{ where } a = t_p \text{ DIV } k \text{ and } b = t_p \text{ MOD } k. \quad (1)$$

In this case, t_p and k are assumed to be integers, for which reason a and b also become integers and b/k is always less than 1.

- 5 If the calibration interval t_k is now expressed by the NFO clock period T in equation (1), the following is obtained with $t_k = n(X/(X+Y))T$:

$$t_p = (a+b/k)n(X/(X+Y))T = MT + FT \quad (2)$$

10

$$\begin{aligned} \text{where } M &= \text{INT}((anX + bnX/k)(X+Y)) &= \text{INT}(nX/(X+Y)(a+b/k)) \\ & &= \text{INT}(Vt_k/To(a+b/k)) \end{aligned}$$

$$\text{and } F = \text{FRAC}((anX + bnX/k)(X+Y)) = \text{FRAC}(Vt_k/To(a+b/k)).$$

15

Since F is the fractional component of an NFO clock period T , higher run time precision T is attained for the second summand in (2) using the relationship $To = nT/(X+Y)$ by writing the NFO period T in integer values of the RCO clock period To :

20

$$\begin{aligned} t_p &= MT + FT = (M-1)T + (F+1)T = (M-1)T + qTo \quad \text{where } q = (F+1)(X+Y)/n \\ &\text{and } q = (F+1)/V. \end{aligned} \quad (3)$$

- 25 Since the time qTo is always longer than one clock period T but shorter than two clock periods T , there has been a breakdown into $M-1$ and $F+1$ clock periods T in equation (3). The effect achieved by this is that the time from the start signal, which appears
- 30 asynchronously with the period T , to the start of an NFO clock cycle and also the end of the lapse phase shown in figure 3 can always be filled in integer fashion with $q = p + (q-p)$ fast RCO clock cycles. This achieves a precise lapse for the programmed time t_p . In
- 35 the average time period - which is of predominant length - of the time lapse, precisely $(M-1)$ NFO clock cycles are counted in power-saving fashion.

After a pause 26 and when triggered by a start signal applied to input C of the microprocessor 1 (symbolized by arrow 27 in figure 2), the programmed run time t_p - which is shown in figure 2 by step 28 - now lapses.

5 When the programmed time t_p has lapsed, a predefined signal is output at the output F of the microprocessor 1 and prompts a prescribed action. The output of the signal is shown in figure 2 by the arrow 29.

10 The lapse of the programmed time t_p is illustrated in detail in figure 5. The start 27 generally occurs out of sync with the NFO clock, which means that up until the occurrence of the first counting edge of the NFO clock (see arrow 41 in figure 5) the internal timer
15 initially counts RCO clock cycles (cf. row Q in figure 5). The counter reading p attained with the first counting edge of the NFO clock - which counter reading must still be smaller than q in this case for the reason cited above $qT_0 > T$ - is stored in the
20 memory of the microprocessor 1 and then the RCO clock is switched off. The state of the RCO is shown in row 42 in figure 5, where "RCO on" means that the RCO is switched on and "RCO off" means that the RCO is switched off.

25 The internal timer 2 which is then connected to the NFO clock now counts precisely $(M-1)$ NFO clock periods T (see row P in figure 5), and then a timer interrupt (symbolized by arrow 43) switches on the RCO again. The
30 latter now undertakes the timer clocking again by appropriately changing over the switch 3 for the remaining $(q-p)$ RCO clock cycles up to the end of the programmed run time t_p . Row 44 in figure 5 once again shows in which periods of time which period or clock
35 frequency governs the microprocessor, where T_0 is the period of the RCO and T is the period of the NFO.

Since in the predominant time component $(M-1)T$, in which only the low-frequency NFO is switched on, the

power consumption of the circuit according to the invention is very low, the power consumption of the whole arrangement can be kept very low during the entire lapse of the programmed time t_p .

5

The frequency tolerance of the oscillators NFO and RCO is of no significance for obtaining a high level of run time precision. Only sufficient short-term stability of the output frequency from these oscillators is
10 necessary, so that the frequencies match during calibration and the run time phase. In addition, RC oscillators require the temperature and the supply of power to be kept constant. This can generally be achieved with simple means, however.

15

List of Reference Symbols

1	Microprocessor
2	Counter unit (timer)
3	Switch
11	Time span in which the RCO is the clock generator
12	Time span in which the NFO is the clock generator
13	Time span in which the external carrier frequency is applied
21	Initialization phase
22	First calibration step
23	Programming step
24	Second calibration step
25	Step for parameter calculation
26	Pause
27	Start signal
28	Lapse of the programmed time
29	Output of the output signal by the microprocessor 1
42	Row
44	Row

10,31,32,33,34,35,36,41,43 Arrow

A,B,C,D,Ub	Inputs of the microprocessor 1
F	Output of the microprocessor 1
K	Signal profile of the unmodulated carrier frequency
L,N,Q	Profile of the RCO signal
M,P	Profile of the NFO signal

i	Prescribed counter reading
n	Number of NFO oscillations
T	Period duration of the NFO
To	Period duration of the RCO
t _p	Programmed time
X,Y	Period number of RCO periods
M	Period number of NFO periods (or M-1)
q,p	Period number of RCO periods
V	Ratio

Patent Claims

1. A method for calibrating an externally programmable electronic circuit having a first oscillator (RCO) and at least one second oscillator (NFO), wherein the second frequency ($1/T$) of the second oscillator (NFO) is lower than the first frequency ($1/T_0$) of the first oscillator (RCO), wherein the circuit, after a programmable time (t_p) has lapsed, outputs an appropriate output signal to prompt the execution of a prescribed action, wherein the programming is effected by modulating a carrier frequency (f_T), wherein the known carrier frequency (f_T) is used to ascertain the present period duration (T_0) of the first oscillator (RCO) and a ratio (V) which corresponds to the ratio between the period duration (T_0) of the first oscillator (RCO) and the period duration (T) of the second oscillator (NFO).
2. The method as claimed in claim 1, characterized in that first of all a first period number (X) for the first oscillator (RCO) is counted up to a counter reading (i), which is prescribed by the carrier frequency (f_T) and which corresponds to a prescribed time (t_k), and this is used to determine the ratio (t_k/X) and therefore the present period duration (T_0) of the first oscillator (RCO), then, starting at a starting edge of the second oscillator (NFO), the periods (T_0) of the first oscillator (RCO) are counted, with the second oscillator (NFO) continuing to operate in parallel, until the first period number (X) is reached by the first instant, and then a next ending edge, occurring after the first instant, of the second oscillator (NFO) is detected, the direction of which can be determined in comparison with the starting edge, wherein a second period

number (Y) for the first oscillator (RCO) is counted off in the period of time starting with the first instant and up to the ending edge being reached, wherein the ratio between the first
5 period number (X) and the second period number (Y) and also the periods (n) of the second oscillator (NFO) which are counted between the starting and ending edges is obtained.

10 3. The method as claimed in claim 2, characterized in that the starting edge and the ending edge of the second oscillator (NFO) have the same direction and therefore the ratio (V) is ascertained from
15 $n/(X+Y)$.

4. The method as claimed in one of the preceding claims, characterized in that
20 the first frequency $(1/T_0)$ is between approximately 1 and approximately 5 MHz and the second frequency $(1/T)$ is between approximately 1 and approximately 10 kHz.

25 5. The method as claimed in one of claims 3 or 4, characterized in that in order to control the lapse of the programmed time (t_p) a third period number (q) for the first oscillator (RCO) is ascertained from

30
$$q = \{[\text{FRAC}(P)] + 1\} / V$$

and a fourth period number (M-1) for the second oscillator is obtained from

35
$$M-1 = [\text{INT}(P)] - 1,$$

wherein $P = V t_k / T_0 (a + b/k)$ and a, b, k are integers.

6. A method for operating an externally programmable electronic circuit which, after a programmed time (t_p) has lapsed, outputs an appropriate output signal to prompt the execution of a prescribed action, wherein the programming is effected by modulating a high precision carrier frequency, wherein the circuit has a first oscillator (RCO) and at least one second oscillator (NFO), wherein the second frequency ($1/T$) of the second oscillator (NFO) is lower than the frequency ($1/T_o$) of the first oscillator (RCO), wherein after or during the calibration of the circuit the time (t_p) is programmed using the carrier frequency, wherein after termination of the calibration and a start signal the transmitted time (t_p) lapses by virtue of an appropriate fourth period number ($M-1$) for the second oscillator (NFO) and an appropriate third period number (q) for the first oscillator (RCO), which operates no more than intermittently in parallel, being counted off.
7. The method as claimed in claim 6, characterized in that the third period number (q) and the fourth period number ($M-1$) are chosen such that the periods (T) of the second oscillator (NFO) are counted over the substantially greatest time component of the transmitted time (t_p), wherein while the time component is lapsing the first oscillator (RCO) is switched off.
8. The method as claimed in one of claims 6 to 7, characterized in that the fourth period number ($M-1$) corresponds to the number (M) of whole periods (T) of the second oscillator (NFO) which are contained in the programmed time (t_p) less 1.

9. The method as claimed in one of claims 6 to 8, characterized in that
the transmitted time (t_p) lapses after the start
5 signal such that first of all, when the first oscillator (RCO) and the second oscillator (NFO) are operating in parallel, a first lapse number (p) of the lapsed periods (T_o) of the first oscillator (RCO), which number has lapsed after
10 the start signal before an edge of the second oscillator (NFO) has been reached, is counted off, then the first oscillator (RCO) is switched off and the fourth period number of periods (T) of the second oscillator (NFO) before the relevant edge
15 of the second oscillator (NFO) is reached is counted off, when the edge just mentioned has been reached the first oscillator (RCO) is switched on again, and finally the difference number ($q-p$) of periods (T_o) of the first oscillator (RCO) between
20 the third period number (q), ascertained in the calibration, and the first lapse number (p) is counted off.
10. An externally programmable electronic circuit
25 having a first oscillator (RCO) and a second oscillator (NFO), wherein the second frequency ($1/T$) of the second oscillator is lower than the first frequency ($1/T_o$) of the first oscillator, wherein the circuit is set up such that when a
30 programmable time (t_p) has lapsed the output of an appropriate output signal prompts the execution of a prescribed action, wherein the programming is effected by modulating a carrier frequency to which the circuit is at least intermittently
35 connected during the programming, wherein a counting unit, which can be connected either to the first oscillator (RCO) or to the second oscillator (NFO), and also means for performing one of the methods specified in claims 1 to 5 and

means for performing one of the methods specified in claims 6 to 9 are provided.

11. The electronic circuit as claimed in claim 10,
5 characterized in that
the first frequency ($1/T_0$) is between
approximately 1 MHz and approximately 5 MHz and
the second frequency ($1/T$) is between
approximately 1 kHz and approximately 10 kHz.