

REPLACED SHEETS		SG
☒	Description : paged 1 to paged 9	
☒	Claim(s) : paged 10 to paged 11	
☒	Drawing(s) : paged 1/2 to paged 3/3	
☒	Abstract : paged 12 to paged	
DATE OF RECEIPT		

1

Picture Reproduction system1P055
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The invention relates to a picture reproduction system.

Picture reproduction systems are known which simultaneously reproduce a picture of a first source, in particular of a first receiving frequency, referred to in the following as main picture, and a picture of a second source, in particular of a second receiving frequency, referred to in the following as reduced picture, where on the screen the reduced picture describes a part of the screen described by the main picture. To achieve this division of the screen it is known to use a picture memory for the reduced picture. A separate picture memory is used for the main picture. Input into and read-out from the two memories takes place synchronously. A controller controls the output from the memories of the picture data which are fed to the screen. Known dynamic or static memories can be used as memories.

Furthermore, circuits are known with the aid of which a relatively higher picture frequency can be generated and thus the picture can be reproduced with an increased picture reproduction frequency. For this purpose two picture memories are used, where a first picture to be reproduced is stored in the first picture memory, while at the same time the picture stored in the other picture memory is read out twice therefrom. In this way two pictures are reproduced while one picture is stored.

For a picture reproduction system with two simultaneously represented pictures of different receiving frequencies, for example one picture memory can be used to store the reduced picture while the other memory stores the combination of the main picture and the reduced picture for the picture reproduction at an increased frequency. When two picture memories are used, however, two controllers are also

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required, which additionally increase the cost of such a circuit arrangement.

To increase the picture reproduction frequency it is known to store a picture in only one picture memory. When commercially available memories are used, one write cycle then alternates with two read cycles, so that on average two pictures are read out while one is written in. When a picture memory with two interfaces is used as memory, where one interface is responsible for the input and the second interface for the output, the data can be written into and read out from the memory simultaneously.

The aim of the invention is to provide a simplified circuit arrangement for storing a reduced picture in a main picture and to permit picture reproduction duplication.

This aim is fulfilled by the features described in Claim 1. Advantageous further developments of the invention are described in the dependent claims.

In accordance with the invention, the data of the main picture and of the reduced picture occurring in digital form are stored in only one single picture memory. A picture memory with two interfaces is used as memory, so that input into and read-out from the memory can take place simultaneously. To enable both the main picture and the reduced picture to be input using one picture memory, each line of the main picture is divided into two parts. The parts of the line of the main picture carrying information are used to write the lines of the main picture into the picture memory, the parts of the line which contain no information due to the line blanking interval are used for the input of the data of the reduced picture into the picture memory. Although the time of the line blanking interval is substantially shorter than the time during which



the line contains information, this input procedure is possible since the quantity of data required for the reduced picture is very much smaller than the quantity of data of the main picture. As a reduced picture describes a smaller screen area than the main picture but is to represent a complete picture, prior to the storage a reduction in the horizontal and vertical directions must be carried out. The quantity of data of the reduced picture is then dependent upon the underscanning rate and ranges between $1/9$ and $1/32$ of the main picture.

In the following an exemplary embodiment will be explained with reference to the drawing in which:

- Fig. 1 illustrates a picture memory;
- Fig. 2 illustrates scan values;
- Fig. 3 illustrates the input process of the reduced picture;
- Fig. 4 illustrates the input process of the reduced picture with delay of the main picture;
- Fig. 5 illustrates a circuit for storage with a delayed main picture.

Fig. 1 illustrates a picture memory employed in accordance with the invention. The picture data to be processed are fed to an input interface 1 which is connected via data lines to a picture memory interface 3. The picture memory interface 3 is connected by data lines both to a picture memory 4 and to an output interface 2. The processed picture data data out can be tapped from data outputs of the output interface 2. The addressing of the picture memory 4 takes place by means of three counters 5, 6, 7 for the horizontal addressing and three counters 9, 10, 11 for the vertical addressing. A controller 8 undertakes the control of the addressing. The counters 5, 9 are responsible for the addresses of the main picture which is to be input. The counters 6, 10 are responsible for the addresses of the



reduced picture which is to be input, and the counters 7, 11 are responsible for the correctly addressed read-out of the entire memory 4.

The input- and output interfaces 1, 2 are clocked with the video scanning frequency. The input interface 1 is supplied with a continuous input data flow data in. The output interface 2 is likewise supplied with a continuous output data flow data out. The data flow rate of the two interfaces 1, 2 can be the same when the pictures are reproduced for example with a picture reproduction frequency of 50 Hz. However, they can also be different if the pictures are reproduced for example with a picture change frequency of 100 Hz.

Fig. 2 illustrates the scan values for the main picture for the reduced picture. If for example the clock frequency of the main picture amounts to 13.5 MHz, 864 picture elements SPS can be reproduced in each line. However, of these 864 picture elements SPS only 725 picture elements SPS are present in an active line. If for example the size of the reduced picture is to amount to one quarter of the main picture in the horizontal and vertical directions, only 180 picture elements SPS need be stored for each line of the reduced picture. In the vertical direction the reduced picture then has only one line while the main picture has four lines. On average it is necessary to input 180 picture elements SPS of the reduced picture in four segments of in each case 144 elements of the line blanking intervals of the main picture.

In order to store 180 scan values SB of the reduced picture in the picture memory 4 during the time of the line blanking interval of the main picture, two approaches are possible:



- A) Half of one line of a reduced picture is input during the time of two time intervals of adjacent lines of the main picture, and this indeed during the time of the line blanking interval. Fig. 3a.
- B) One complete line of the reduced picture is input during time of the line period of the main picture and the active part of a line of the main picture is delayed. Fig. 3b.

Fig. 3 illustrates the principle of the input process of the data of a reduced picture into the main memory 4. During the line blanking interval of the main picture, half of a line (Fig. 3a) consisting of ninety picture elements SPS of the reduced picture can be input into the main memory 4. A time of 144 picture elements SPS is available for this purpose. The counters 6, 10 together with the controller 8 are responsible for the correct addressing. In accordance with Fig. 3b, the complete line of the reduced picture of 180 picture elements SPS can be input into the main memory. Then however the following line of the main picture must be delayed by at least 36 picture elements. This can be effected by means of a line memory or buffer with a small storage capacity. As can be seen from Fig. 3b, a further delay of the following line of the main picture is no longer necessary as it is compensated by the 144 picture elements of the line blanking interval of the second line of the main picture.

Fig. 4 illustrates the input process of a line of the reduced picture with delay of the input of the line of the main picture. Fig. 4a illustrates the time requirement of one line of the main picture of 720 picture elements SPS. During the time of 144 picture elements, thus during the line blanking interval, no picture data of the main picture is to be stored. Fig. 4b illustrates the storage of a line both of the reduced picture and of the main picture. All



180 picture elements of the reduced picture are stored. For this purpose the line of the main picture must be delayed for the time of 36 up to a maximum of 144 picture elements. Following the completion of the input process of this line, one complete line of the main picture is immediately stored so that the delay is compensated again.

Fig. 5 illustrates the circuit for storage with a delayed main picture MP. The main picture MP is fed to a signal processing circuit 12 in which for example the picture elements are digitalized and a data reduction can be effected. The output data lines of the signal processing circuit 12 lead to inputs of a flip-flop 21 on the one hand via a delay circuit 13 and also directly. The picture RP which is to be reduced is fed to a signal processing circuit 14 in which underscanning with the clock signal C takes place. The output signal of the signal processing circuit 14 is fed to a buffer 15 which intermediately stores the data. The buffer 15 is addressed by a counter 16. The buffer 15 and the counter are clocked by the same clock signal T. Furthermore the counter 16 has a reset input R which resets the counter 16 to a predetermined value when the input process into the buffer 15 is completed. The clock signal T fed to the counter 16 and to the buffer 15 is switched over by an output M3 of the controller 8, depending upon whether input into or read-out from the buffer 15 is taking place. If input into the buffer 15 is to take place, a switch 24 is switched over to the write clock signal 27 whereas if the buffer 15 is to be read out, it is switched over to the read clock signal 28. The output data lines of the buffer 15 lead to a flip-flop 18. The data output lines of the flip-flop 21 lead to a further input of the flip-flop 18. The flip-flop 18 is connected via a data line M2 to the controller 8. The output data lines of the flip-flop 18 are connected to a D-flip-flop 19. This D-flip-flop 19 is connected to the read clock signal 28 of the buffer 15 and



of the counter 16. The output data lines of the D-flip-flop 19 lead via a D-flip-flop 20 to the input interface 1 of the picture memory 4. Via the picture memory interface 3 the data are input into the picture memory 4. Via further control lines the controller 8 is connected to address counters 22, 23. The output signal M4 of the controller 8 controls change-over switches 25, 26 which switch over the address counters 22, 23 for the addressing of the picture memory 4. The address counters 22, 23 correspond to the counters 5, 6, 7 and 9, 10, 11. The output interface 2 is clocked by means of a clock pulse CK. The change-over switch 24 is controlled by an output signal M3 of the controller 8, while the change-over switches 25, 26 are controlled by the signal M4 of the controller 8.

The circuit shown in Fig. 5 is divided into two parts. The signal processing of the reduced picture and of the main picture is carried out in the first part 29. In the second part 30 the signals of the reduced picture RP and of the main picture MP are stored in the picture memory 4 and read out line-sequentially for a picture reproduction. The selection between the signals of the reduced picture and of the main picture in the first part is made by the multiplexer 18.

The signal processing for the main picture takes place as follows:

The signal of the main picture MP can be fed to the multiplexer 18 via two paths:

Via the signal processing circuit 12 the data of the main picture are fed directly to the multiplexer 18. This path is used when no reduced picture is to be input into the memory 4 during the line blanking interval. If, however, data of the reduced picture are to be input into the memory 4, the data of the main picture are fed via a delay circuit



13 to the multiplexer 18. The delay circuit 13 effects a delay of $n \times T$. This delay is necessary to enable one complete line of the reduced picture, commencing with the line blanking interval, to be input into the memory 4 and for this input process to continue through the start of the active part of the next line of the main picture.

The smallest value of the time delay T is $n = 36$ ($180 - 144 = 36$), and the largest value is $n = 144$. This is the case when the lines m and $m+1$ of the main picture must be input with no free space between them.

The main picture is input into the main memory 4 within the addressing of the address counters 22.

The signal processing for the reduced picture is carried out as follows.

The output of the signal processing circuit 15 supplies one signal of the reduced picture every four lines. Each line consists of 180 scan values. This data is input into the buffer 15. The write clock rate could amount for example to 3.375 MHz, thus to one quarter of the clock rate of the main picture. The first address, into which the data of the reduced picture must be written, is supplied by the address counter 16 reset by the reset function.

When one complete line of the reduced picture has been input into the buffer 15, the controller 8 awaits the start of the next line blanking interval of a line of the main picture.

At the start of this line blanking interval the system is pre-programmed to input the reduced picture into the main memory 4 in the correct sequence.

This means that the multiplexer 21 is switched so that the original picture is delayed by $n \times T$. The multiplexer 18 is



switched to the position for the reduced picture. The main memory 4 is supplied with the signal of the reduced picture. The change-over switch 24 is switched to the read clock signal 28 by the controller 8. The switching signal M4 of the controller 8 has switched the change-over switches 25, 26 to the address counters 23. These address counters 23 also show those addresses of the memory 4 into which the reduced picture is to be input.

When, after 180 clock cycles, the reduced picture has been input into the memory 4; the multiplexer 18 and the change-over switches 24, 25 and 26 are switched back to the position for the main picture processing. The address counters 22 again assume the addressing of the memory 4. The multiplexer 21 remains in the position for delay of the main picture during the complete following line of the main picture. It is not switched back by the signal M1 of the controller until the start of the next line blanking interval of the main picture MP.

Shift registers, memories or first-in first-out shift registers can be used for example as buffer 15.

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Deutsche Thomson-Brandt GmbH
7730 Villingen-Schwenningen

Hannover, 21.08.89
PTL-WÖ/gn

Claims

1. Picture reproduction system with storage of data-reproducing picture, characterised in that there are stored in a picture memory (4) a picture of a first source, e.g. a first reception frequency, and at least one picture of a second source, e.g. a second reception frequency, the picture of the first and/or the second source representing a picture reduced in its spatial dimensions and for the purpose of picture reproduction there are read out in time sequential manner the data of the picture memory.
2. A picture reproduction system according to Claim 1, characterised in that the data of the pictures of the second source are written sequentially using the line blanking intervals of the pitch of the first source in the picture memory (4).
3. A picture reproduction system according to Claim 1, characterised in that the picture store (4) contains an input- and an output- interface (1, 2).
4. A picture reproduction system according to Claim 2, characterised in that the picture store (4) additionally contains two address pair inputs (5,9; 6,10; 22,23), which control the different addresses of the picture memory (4) for the data to be written in.
5. A picture reproduction system according to one or more of the preceding claims, characterised in that a complete





line of the picture of the second source is written into the picture memory (4), beginning with the begin of the line blanking interval of the picture of the first source and ending with the begin of the first active part of the next line of the picture of the first source.

6. A picture reproduction system according to one or more of the preceding claims, characterised in that there is used a buffer (15) which stores one line of the picture of the second source, before it is written into the picture memory (4).

7. A picture reproduction system according to Claim 5, characterised in that a delay circuit (21) delays the data of one line of the picture of the first source.

8. A picture reproduction system according to Claim 7, characterised in that the data of one line of the picture of the second source from the buffer (15) is completely written into the picture memory (4).

9. A picture reproduction system according to Claim 5, characterised in that a first part of the data of the lines of the picture of the second source are written into the memory (4) during the line blanking interval of one line of the picture of the first source, and another part of the data of the lines of the picture of the second source are written into the memory (4) in the period of the subsequent line blanking interval of the picture of the first source.

