

METHOD FOR DECREASING THE INITIATION TIME IN AN ELECTROLESS BATH

5 Field of the Invention

The present application is generally related to the field of metallizing substances, and more particularly to a process for decreasing the initiation time of an electroless bath plating solution.

10

Background of the Invention

A process for selectively metallizing a circuit board is described in U.S. patent no. 5,162,144, (assigned to the same assignee as the present application) and hereby incorporated by reference. This process is used in conjunction with a dielectric layered, sequentially processed circuit board, as described in U.S. patent no. 5,260,170 (assigned to the same assignee as the present application). This circuit board process requires the sequential deposition and photo-definition of openings in two resins. The first resin, called resin A, is filled with a material referred to herein as a filler, which when activated, will promote electroless plating with a metal, the second resin, called resin B, does not contain such a filler. When each resin, in turn, is photochemically patterned, resin B over resin A, openings produced in resin B define areas called "channels"; superimposed openings produced in resin A and resin B define deeper areas called "wells" which open to a metal layer below. When this structure is subjected to processes which modify or activate particles contained in or at the surface of resin A, the channels and wells may be coated with an electroless plated metal to form metallic features, such as pads, vias and conductors.

30

In today's manufacturing environment reducing process throughput time is critical. After the particles are activated on the circuit

board the electroless plating occurs. Electroless plating is normally characterized by an initiation time, defined as the time it takes the board to start plating once placed in the electroless bath. High activity electroless baths have a fast initiation time but can result in spurious plating. More stable bath chemistries result in longer initiation times. Further, it was found that longer initiation times result in a grainier deposit with less initiation and adhesive sites.

Thus there exists a need for a method to decrease the initiation time of a stable electroless bath. Further, there exists a need for a method which results in a better deposit.

Description of the Preferred Embodiments

In producing a dielectric layered, sequentially processed circuit board, conductors, vias and pads are photochemically defined in the resins. This process exposes the resin A wherever a conductor, via or pad is required. Then the small metal oxide particles on the surface of resin A are exposed. The circuit board is then immersed (or sprayed) in a reducing solution, which produces small catalytic islands around the metal oxide particles. These islands have a thin layer of active metal. For instance in the preferred embodiment the metal oxide particles are Cu_2O . Once exposed to the reducing solution thin island layers of CuH , Cu^0 or CuBH_x form. Next, the board is placed in an electroless bath and solid copper formations appear where ever the catalytic islands occur in sufficient quantity.

The initiation time for a stable electroless bath can be as long as fifteen minutes. To decrease the initiation time a further step of immersing or spraying the circuit board with a noble metal salt solution occurs before electrolessly plating the circuit board. This results in a metal displacement reaction, in which the copper is replaced with the noble metal. This displacement only occurs in a thin layer on the top of the copper.

This layer of the noble metal is catalytic and also protects the copper based catalytic islands from oxidation. Since there are no oxides to remove, the electroless bath can start plating almost immediately. The copper oxides occur even if the board is immediately transferred to the



electroless bath, but increase with any delay. Since the noble metal treatment maintains activity of all the catalytic film produced, control of catalytic film growth is essential for maintaining selective plating. Growth of the catalytic film can be controlled by manipulation of the reduction solution concentrations and the reduction time.

EXAMPLES

1. Samples of a two dielectric layered, sequentially processed circuit board produced according to U.S. patent no. 5,260,170 were prepared. The samples were reduced in a 1.0 molar borohydride and 0.25 molar EDTA solution for five minutes. The samples were then rinsed with deionized water. One sample was then placed in an ionic palladium solution for ten seconds. While, the second sample was dried and set aside. After the palladium dip the first sample was rinsed with deionized water. Both samples were then placed in a Shipley 4500 electroless copper bath for two minutes. The samples were then viewed with a scanning electron microscope.

The second sample showed only isolated plating, while the first sample was continuously plated.

2. A second sample of a two dielectric layered, sequentially processed circuit board produced according to U.S. patent no. 5,260,170 was prepared. The sample was exposed to the ionic palladium solution for ten seconds. Then the sample was rinsed in deionized water and placed in a Shipley 4500 electroless copper bath for two minutes. The sample was then viewed under a scanning electron microscope. The sample showed no plating had occurred. Enhanced plating is not due to adsorption of ionic palladium on the resin of the sample.

In summary, the present invention provides a method for decreasing the initiation time, increasing the density of adhesive sites and decreasing the particle size of the plated copper of conductors, pads and via on a circuit board.



Claims



What is claimed is:

5

1. A method of decreasing the initiation time of copper-based catalytic film grown on a dielectric layered circuit board placed in an electroless bath, the method comprising the consecutive steps of:

10

producing copper-based catalytic islands from discrete copper oxide locations on or in a surface of a dielectric layer of the circuit board;

rinsing the surface with deionized water;

15

treating the surface with an ionic noble metal solution; and

rinsing unreacted noble metal solution off the surface before placing the circuit board in the electroless bath.

20

2. The method of claim 1, wherein the step of treating the surface with an ionic noble metal solution includes the sub-step of selectively depositing a thin layer of noble metal onto areas covered by the copper-based catalytic islands via an electrochemical displacement of reduced copper on the surface of the catalytic islands.

25

3. The method of claim 1, wherein the step of treating the surface with an ionic noble metal solution includes the sub-step of immersing the surface in the ionic noble metal solution.

30

4. The method of claim 1, wherein the step of treating the surface with an ionic noble metal solution includes the sub-step of immersing the surface in the ionic noble metal solution for preferably two minutes.



5 5. The method of claim 1, wherein the step of treating the surface with an ionic noble metal solution includes the sub-step of spraying the surface with the ionic noble metal solution.

 6. The method of claim 1 wherein the step of producing copper-based catalytic islands includes the sub-steps of:

10 exposing the discrete copper oxide locations on the surface; and

 treating the surface with a reduction solution, thereby producing an active metal layer.

15 7. A circuit board with selectively deposited electroless copper produced in accordance with any one of the methods as defined in claims 1 through 6.