A B S T R A C T

FAULT TOLERANT MEMORY SYSTEMS

In a memory system comprising a plurality of memory units (10) each of which possesses unit-level error correction capabilities (20) and each of which are tied to a system level error correction function (30), memory reliability is enhanced by providing means for fixing the output of one of the memory units at a fixed value in response to the occurrence of an uncorrectable error in one of the memory units. This counter-intuitive approach to the generation of forced hard errors nonetheless enhances overall memory system reliability since it enables the employment of the complement/recomplement algorithm which depends upon the presence of reproducible errors for proper operation. Thus, chip level error correction systems, which are increasingly desirable at high packaging densities, are employed in a way which does not interfere with system level error correction methods.

This Sheet Has Been Replaced

