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FIG. 1A

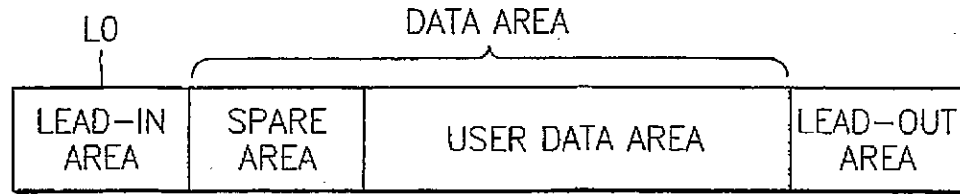


FIG. 1B

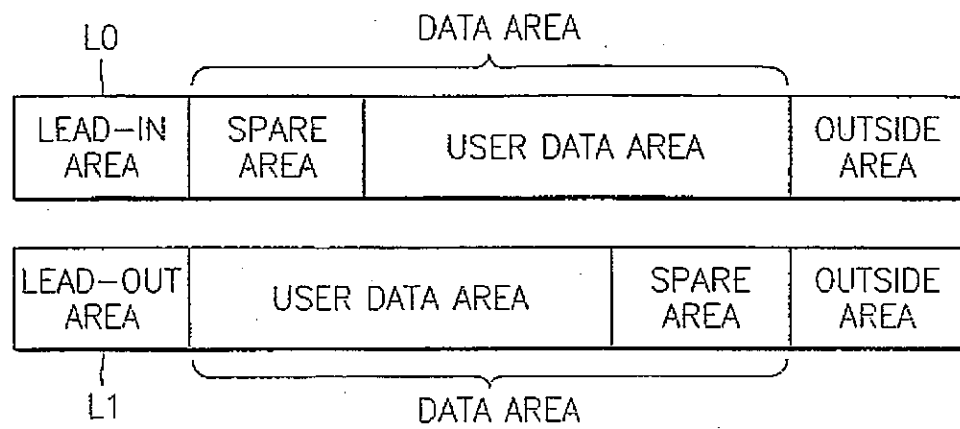


FIG. 2

SBM #0	finalization flag = 0
	update counter = 0
	Bit Map #0
SBM #1	finalization flag = 0
	update counter = 1
	Bit Map #1
...	...
SBM #n	finalization flag = 0
	update counter = n
	Bit Map #n
...	...

FIG. 3

SBM #0	finalization flag = 0
	update counter = 0
	Bit Map #0
SBM #1	finalization flag = 0
	update counter = 1
	Bit Map #1
...	...
SBM #n	finalization flag = 0
	update counter = n
	Bit Map #n
SBM #n	finalization flag = 1
	update counter = n
	Bit Map #n
RECORDING PREVENTION AREA	ffh
...	...

FIG. 4

LEAD-IN AREA	...
	DEFECT MANAGEMENT AREA (DMA2)
	RECORDING CONDITION TEST AREA
	TEMPORARY DISC DEFECT STRUCTURE (TDDS) AREA
	TEMPORARY DEFECT LIST (TDFL) AREA
	SPACE BIT MAP (SBM) AREA
	DISC AND DRIVE INFORMATION AREA
	DEFECT MANAGEMENT AREA (DMA1)
	...
DATA AREA	SPARE AREA 1
	USER DATA AREA
	SPARE AREA 2
LEAD-OUT AREA	...
	DEFECT MANAGEMENT AREA (DMA4)
	...
	DEFECT MANAGEMENT AREA (DMA3)
	...

FIG. 5

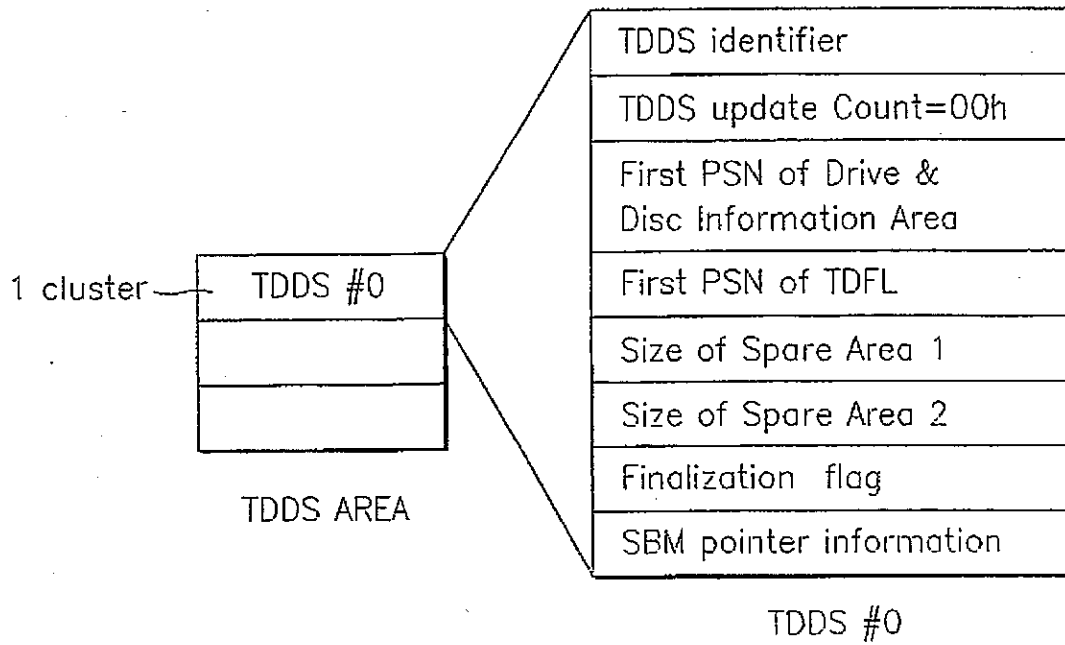


FIG. 6

LEAD-IN AREA	...
	DEFECT MANAGEMENT AREA (DMA2)
	RECORDING CONDITION TEST AREA
	AREA FOR BOTH TDDS AND SBM (TDDS+SBM AREA)
	TDFL AREA
	DISC AND DRIVE INFORMATION AREA
	DEFECT MANAGEMENT AREA (DMA1)
	...
DATA AREA	SPARE AREA 1
	USER DATA AREA
	SPARE AREA 2
LEAD-OUT AREA	...
	DEFECT MANAGEMENT AREA (DMA4)
	...
	DEFECT MANAGEMENT AREA (DMA3)
	...

FIG. 7

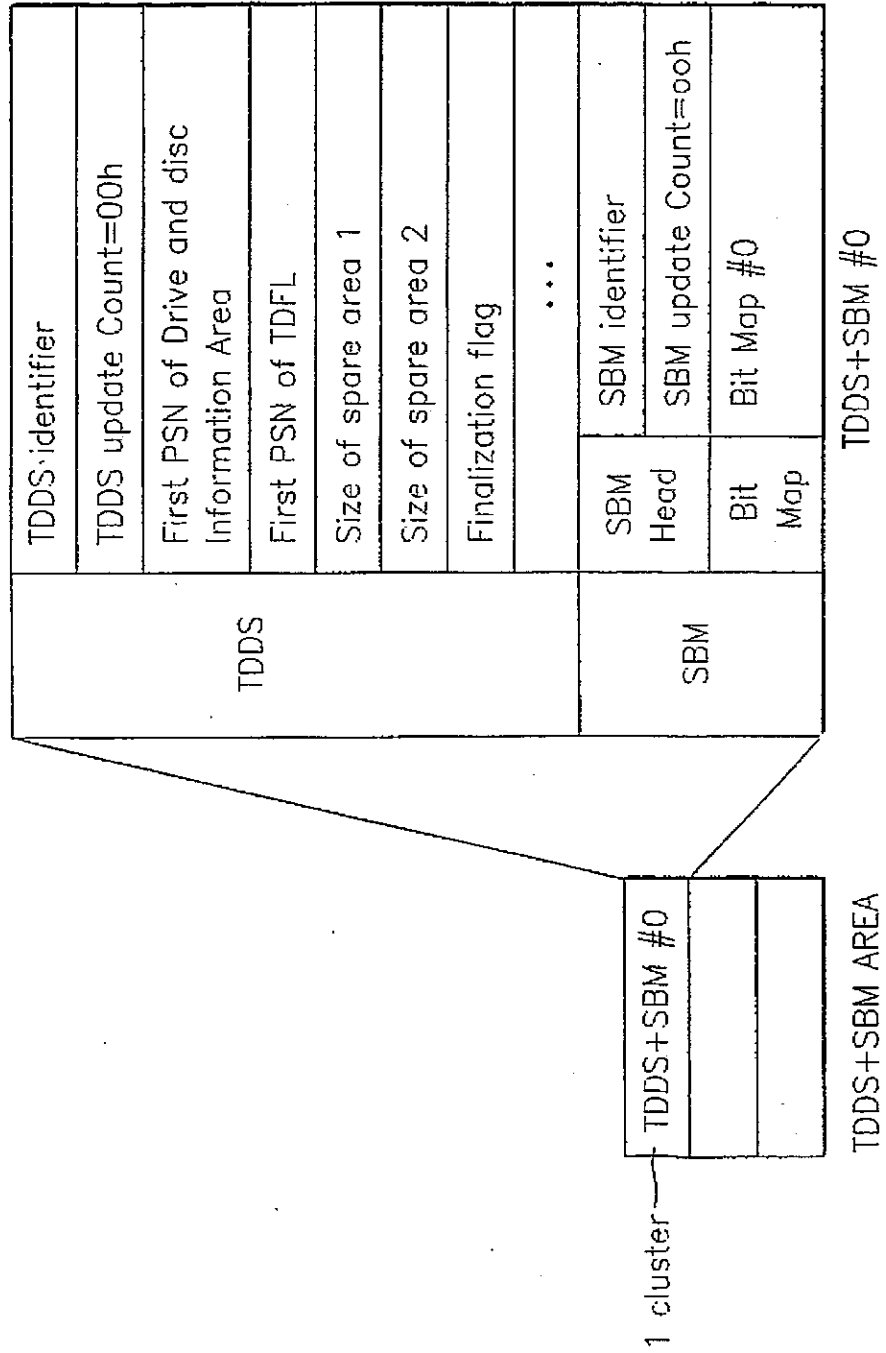


FIG. 8

Lead-in	...
	DMA2
	Recording Condition Test Area
	TDMA
	Drive information Area
	DMA1
	...
Data Area	Spare Area 1
	update counter = n
	Spare Area 2
Lead-out	...
	DMA3
	...
	DMA4
	...

FIG. 9

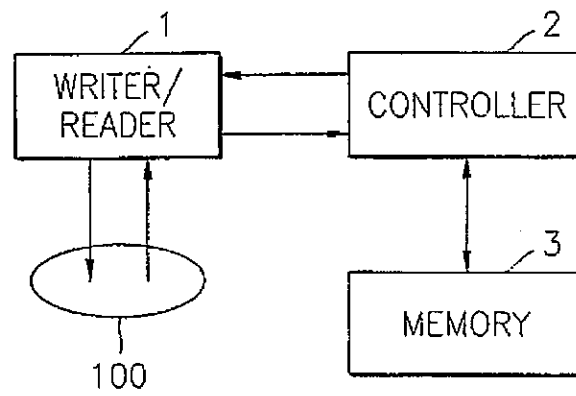


FIG. 10

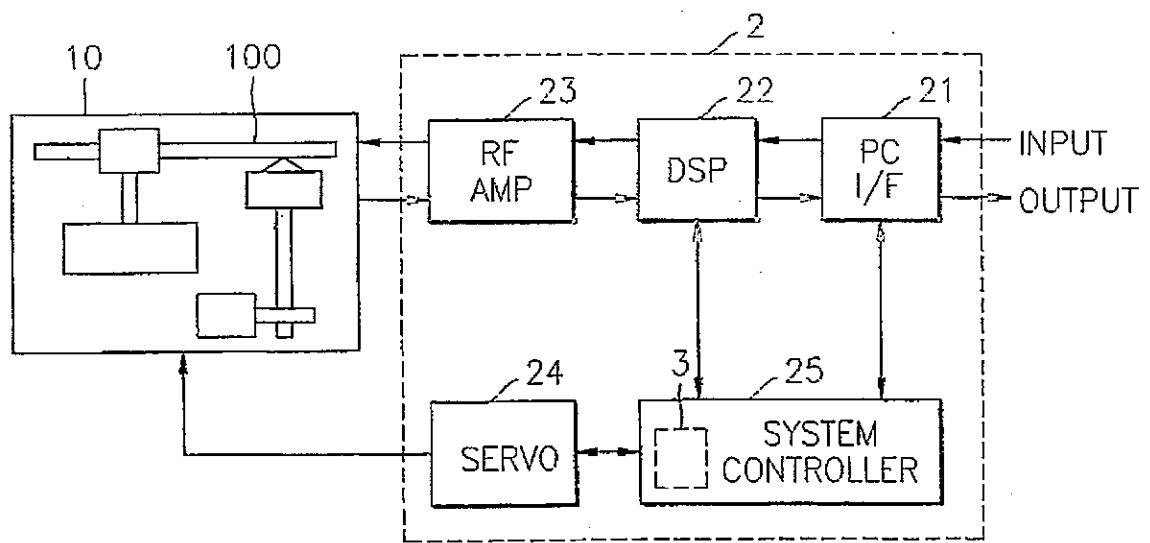


FIG. 11

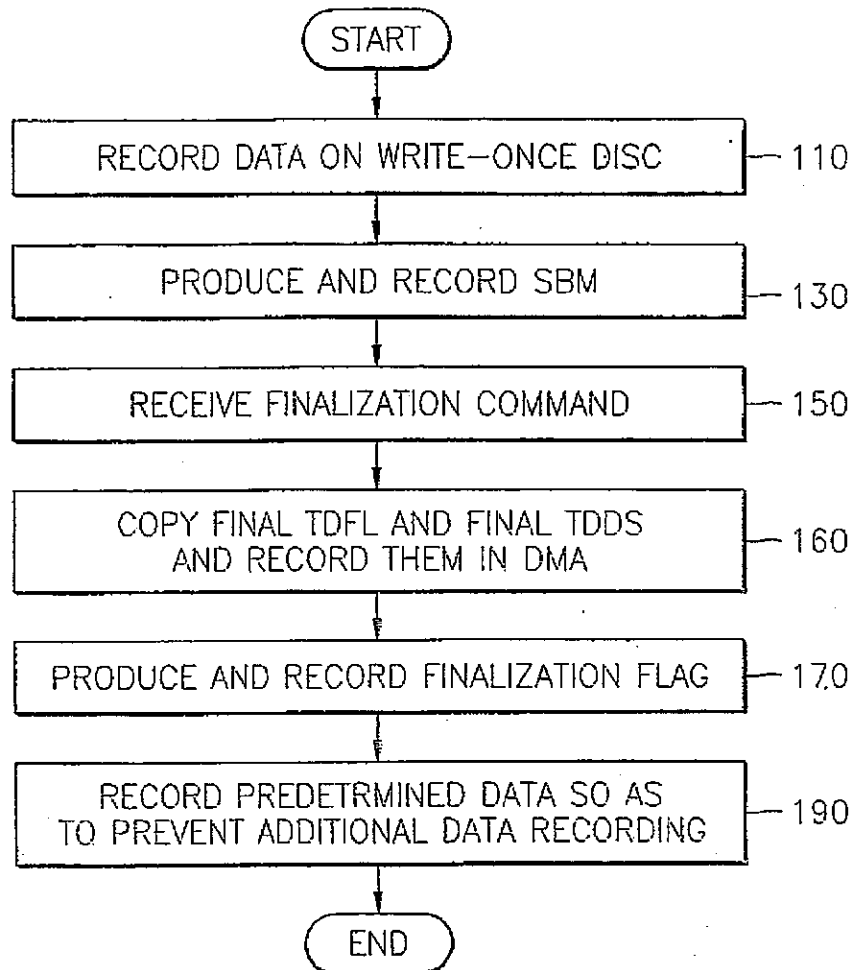


FIG. 12

