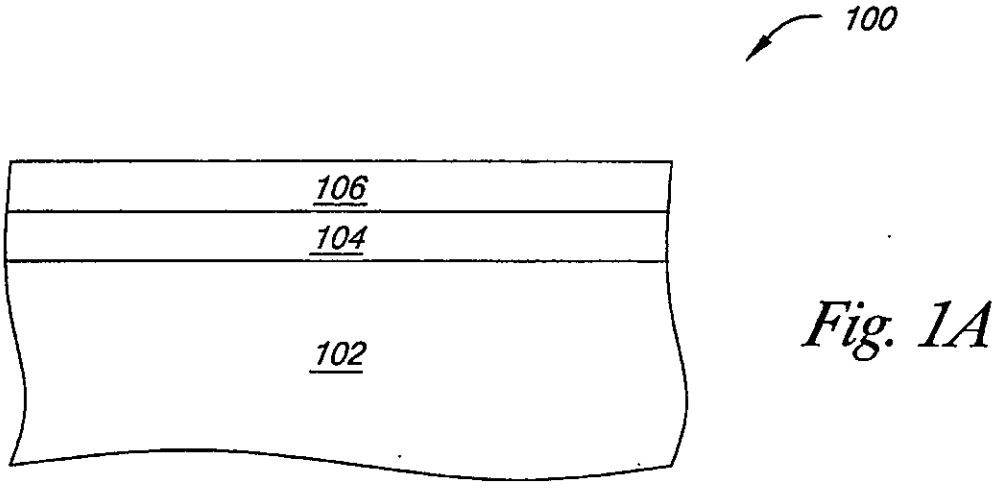


Fig. 1A

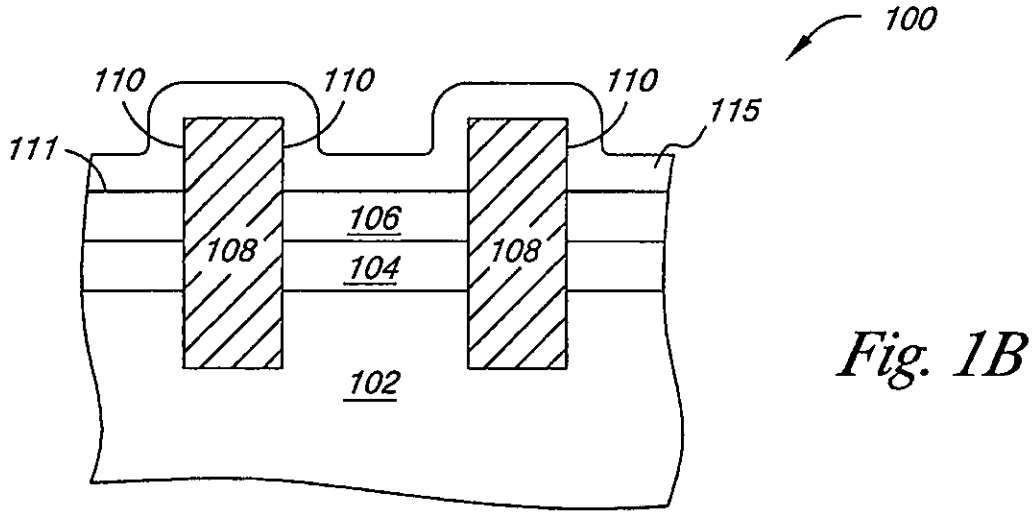


Fig. 1B

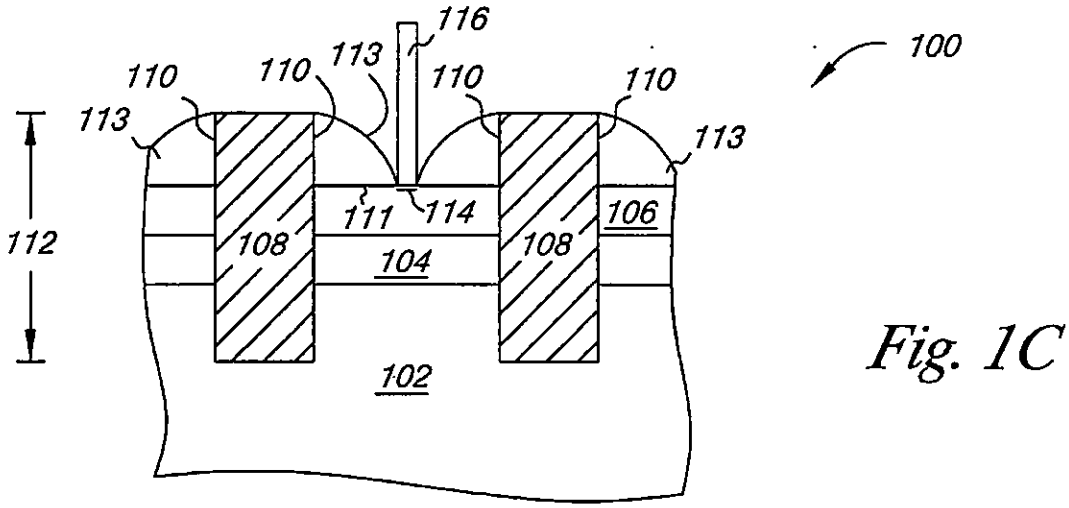


Fig. 1C

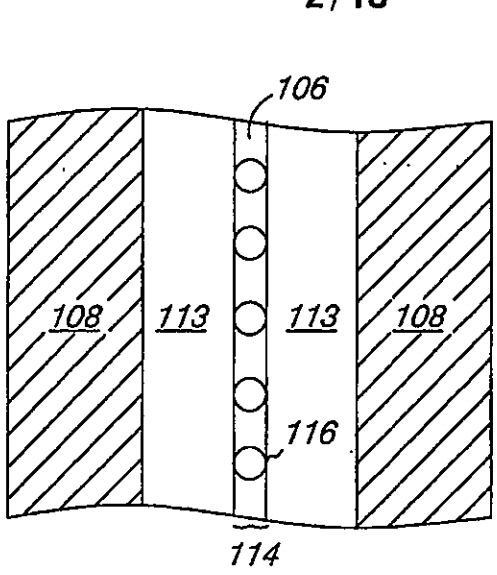


Fig. 1D

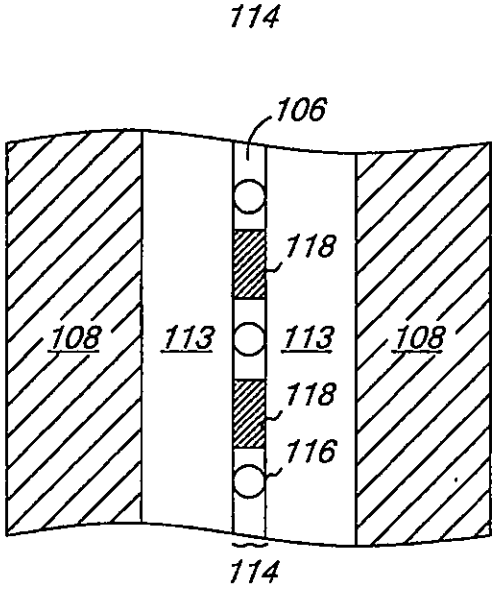


Fig. 1E

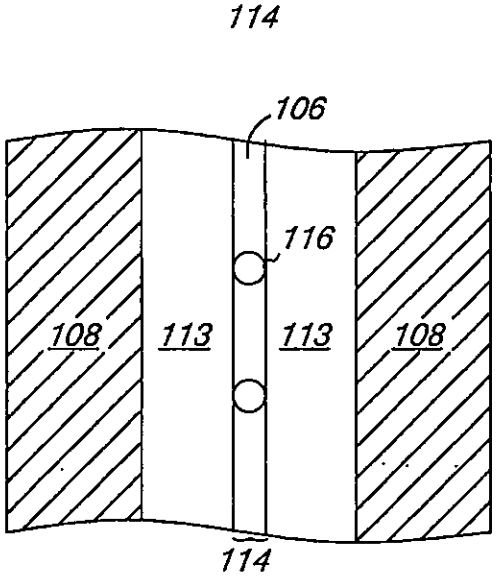


Fig. 1F

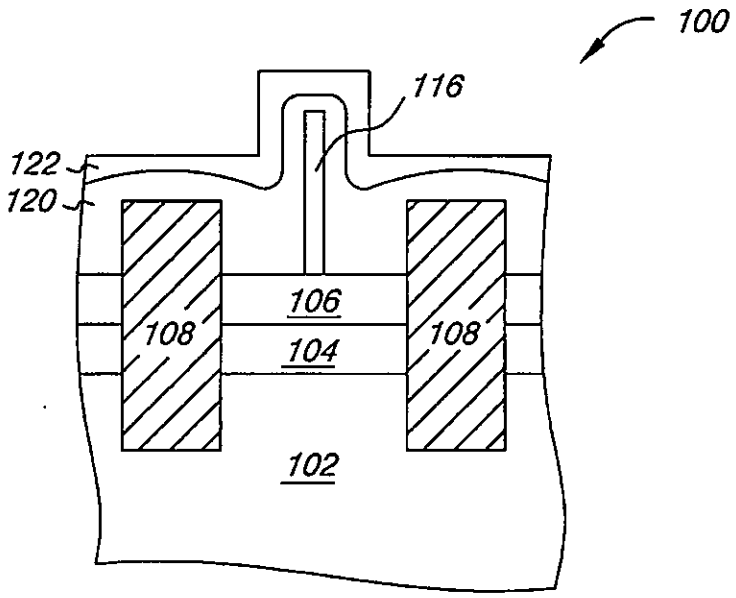


Fig. 1G

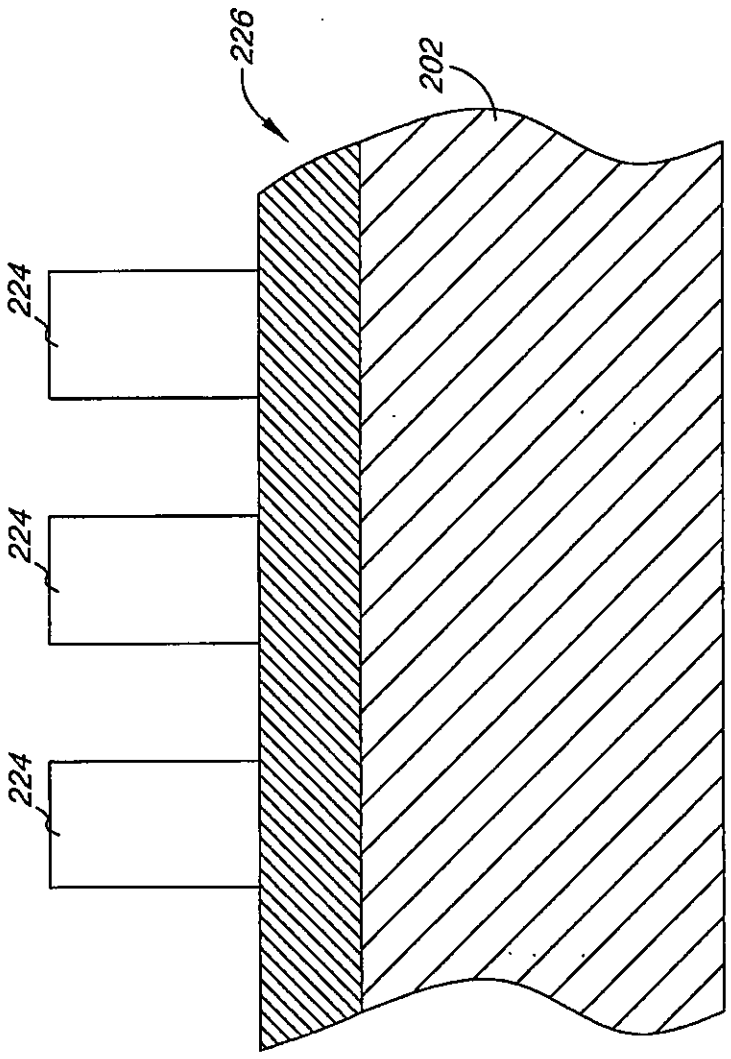


Fig. 2A

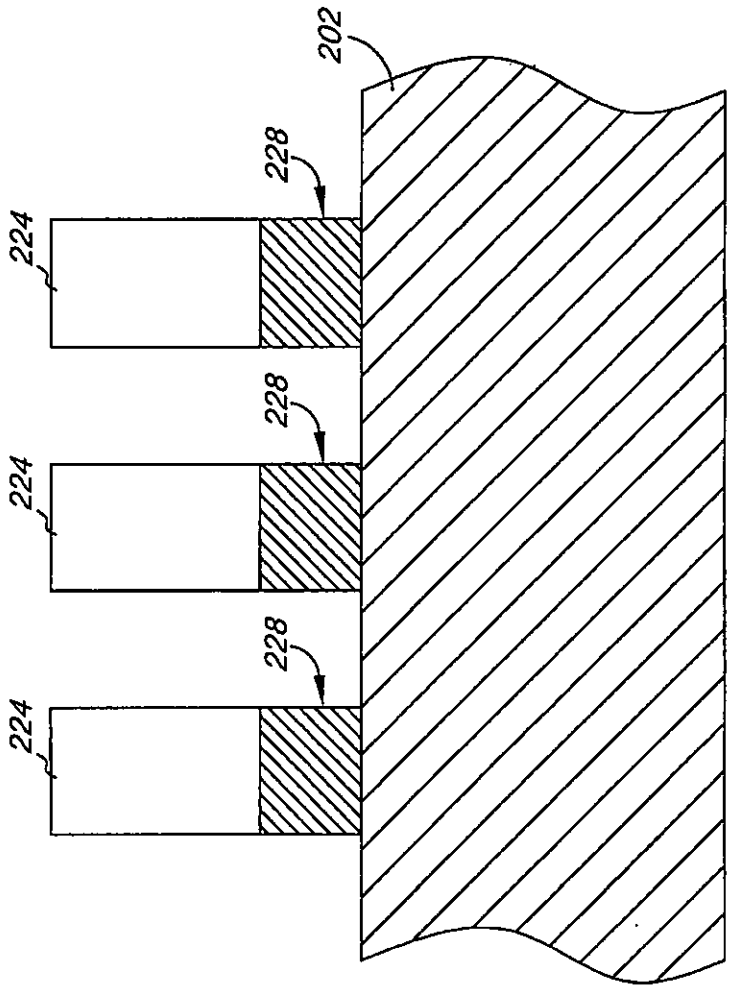


Fig. 2B

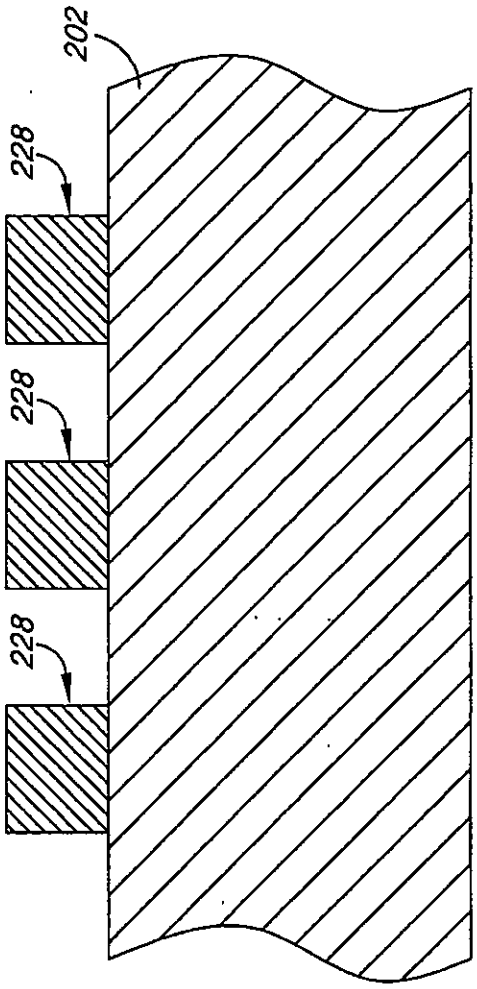


Fig. 2C

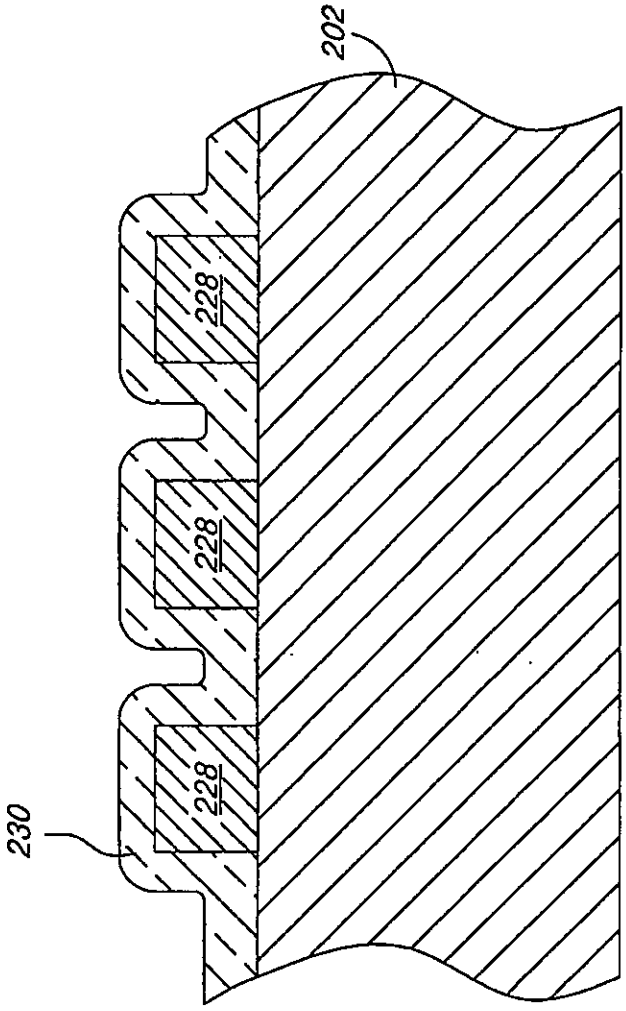


Fig. 2D

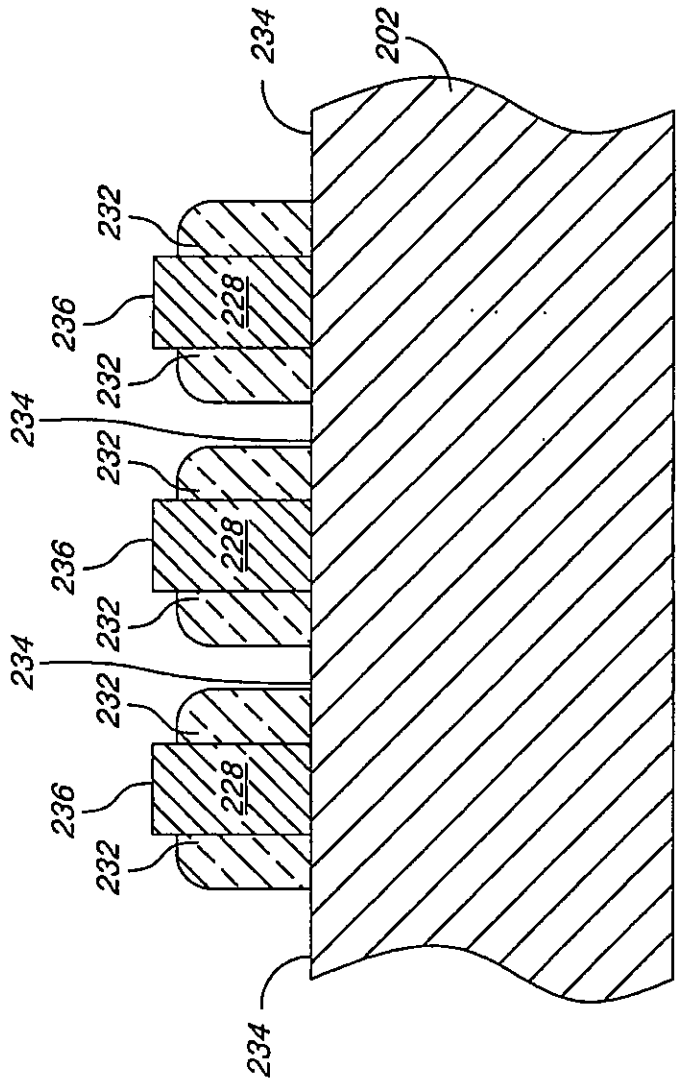

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Fig. 2E

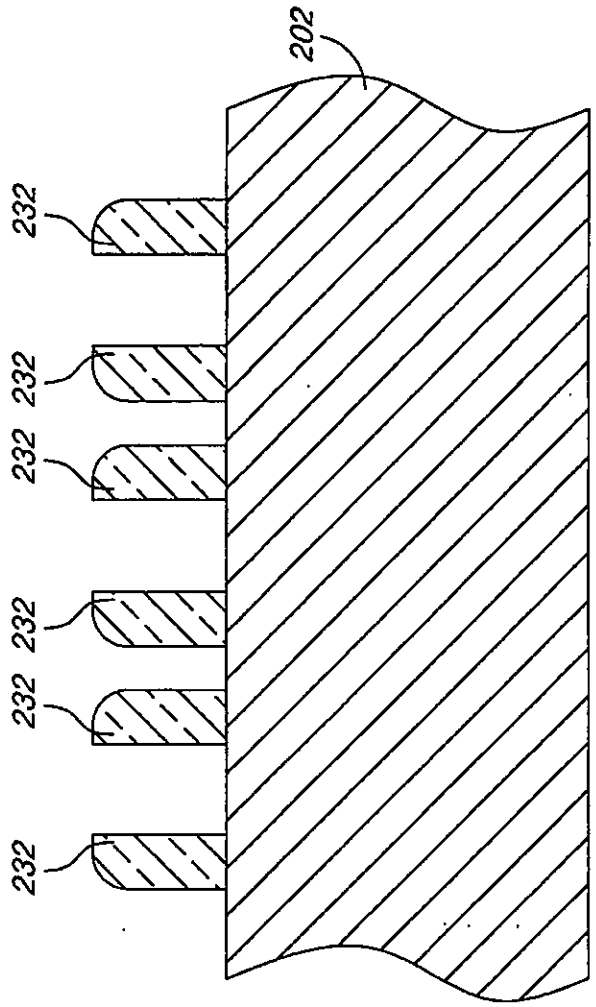


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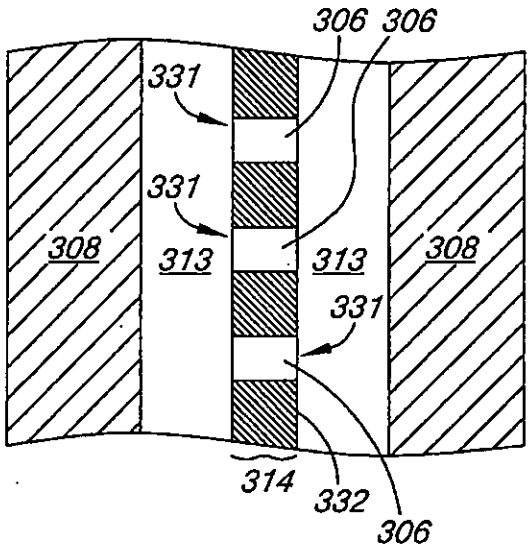


Fig. 3

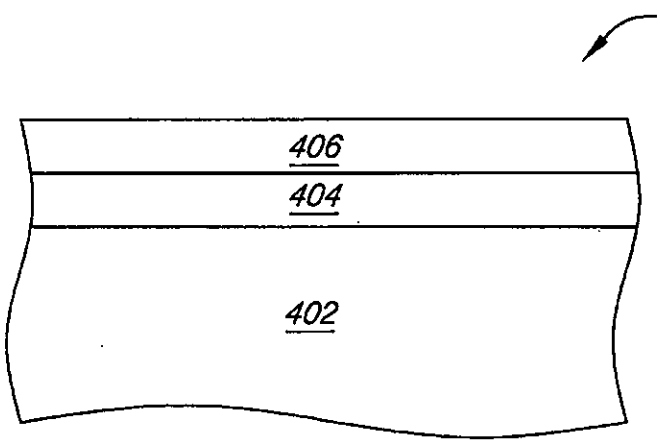


Fig. 4A

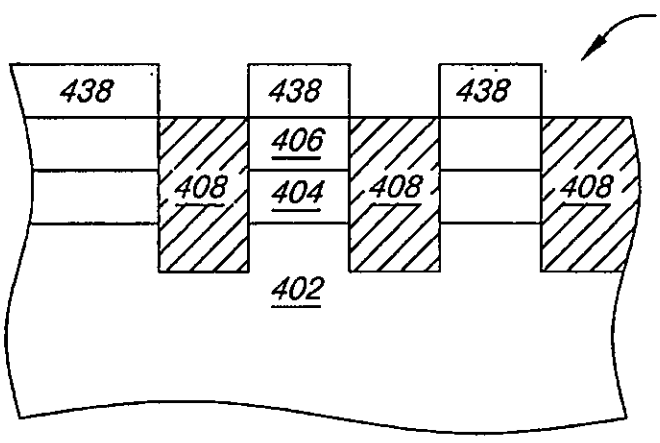


Fig. 4B

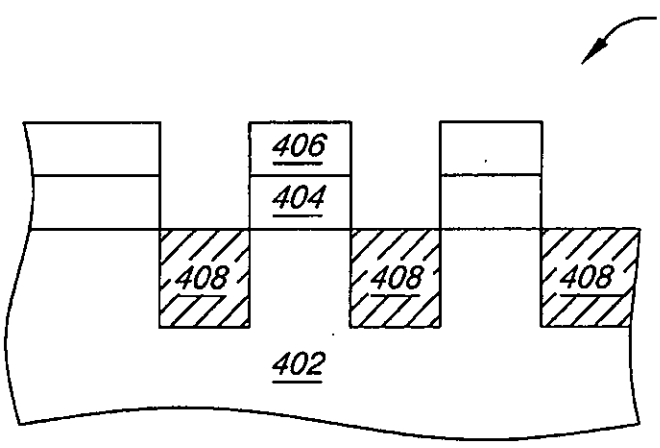


Fig. 4C

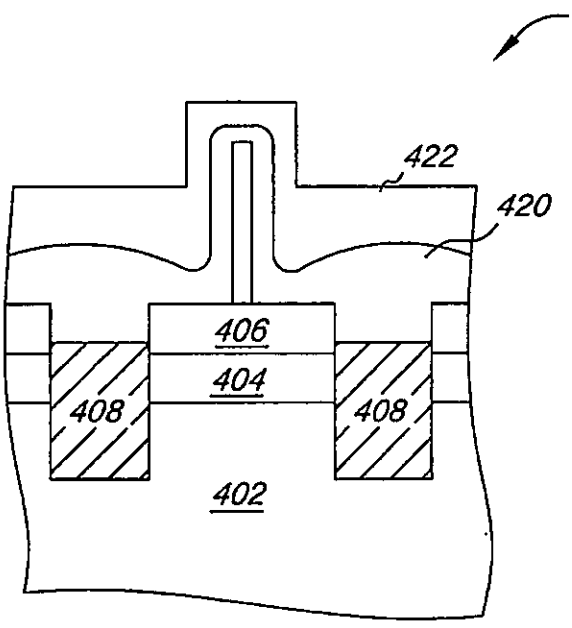


Fig. 4D

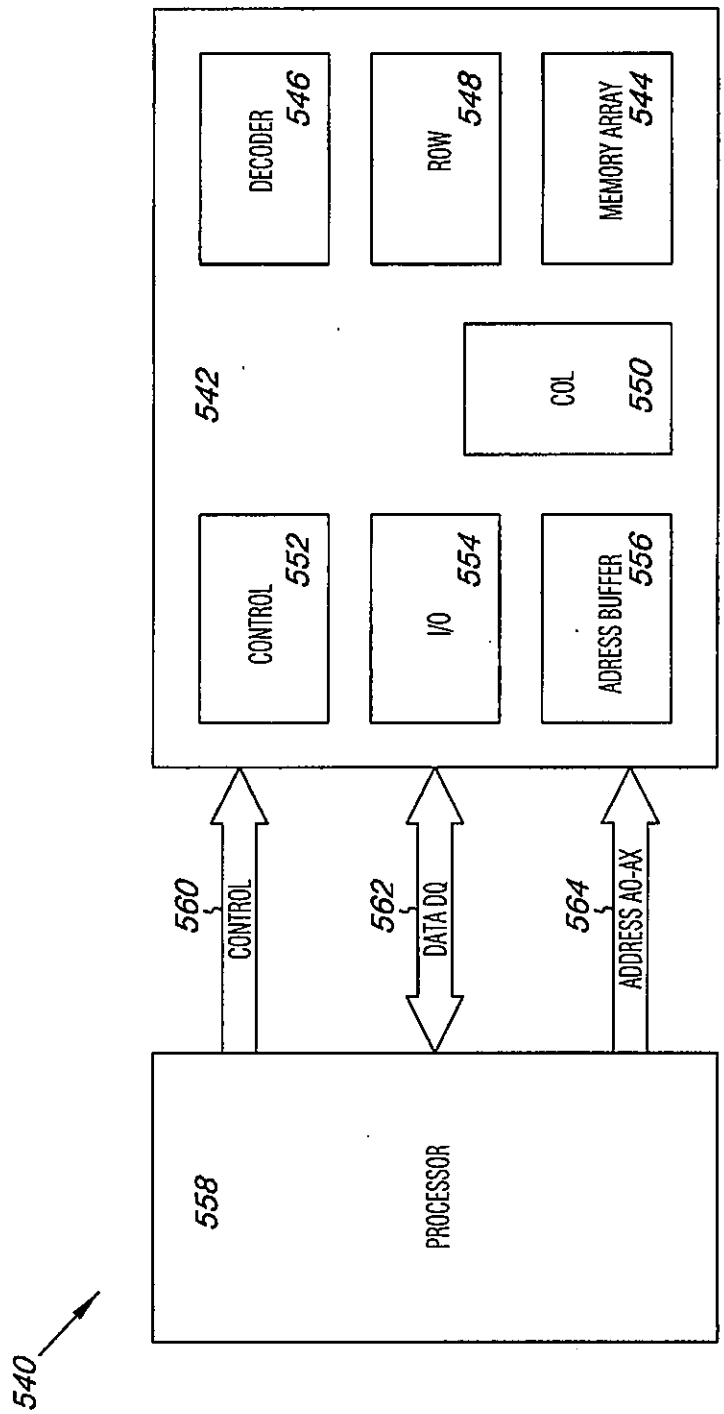

DECODER 546
ROW 548
MEMORY ARRAY 544
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COL 550
CONTROL 552
I/O 554
ADRESS BUFFER 556
560
CONTROL
562
DATA DQ
564
ADDRESS A0-AX
558
PROCESSOR
540

Fig. 5