METHODS OF FORMING ELECTRICAL CONNECTIONS FOR SEMICONDUCTOR CONSTRUCTIONS

ABSTRACT

The invention includes methods for forming electrical connections associated with semiconductor constructions. A semiconductor substrate is provided which has a conductive line thereover, and which has at least two diffusion regions adjacent the conductive line. A patterned etch stop is formed over the diffusion regions. The patterned etch stop has a pair of openings extending through it, with the openings being along a row substantially parallel to an axis of the line. An insulative material is formed over the etch stop. The insulative material is exposed to an etch to form a trench within the insulative material, and to extend the openings from the etch stop to the diffusion regions. At least a portion of the trench is directly over the openings and extends along the axis of the line. An electrically conductive material is formed within the openings and within the trench.

FIGURE 30