FIG. 1

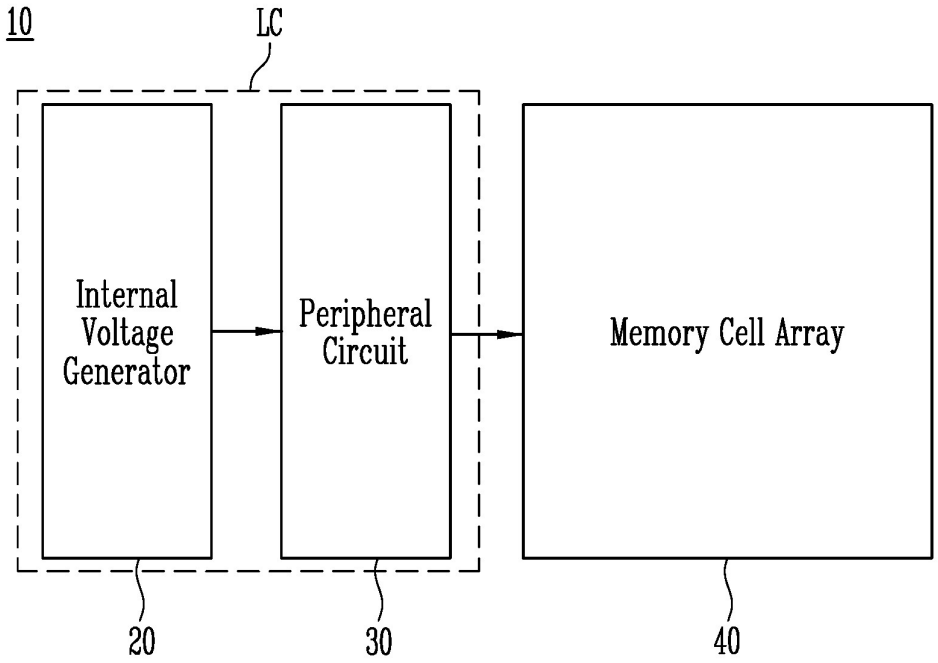

10
LC
Internal Voltage Generator
Peripheral Circuit
Memory Cell Array
20
30
40

FIG. 2

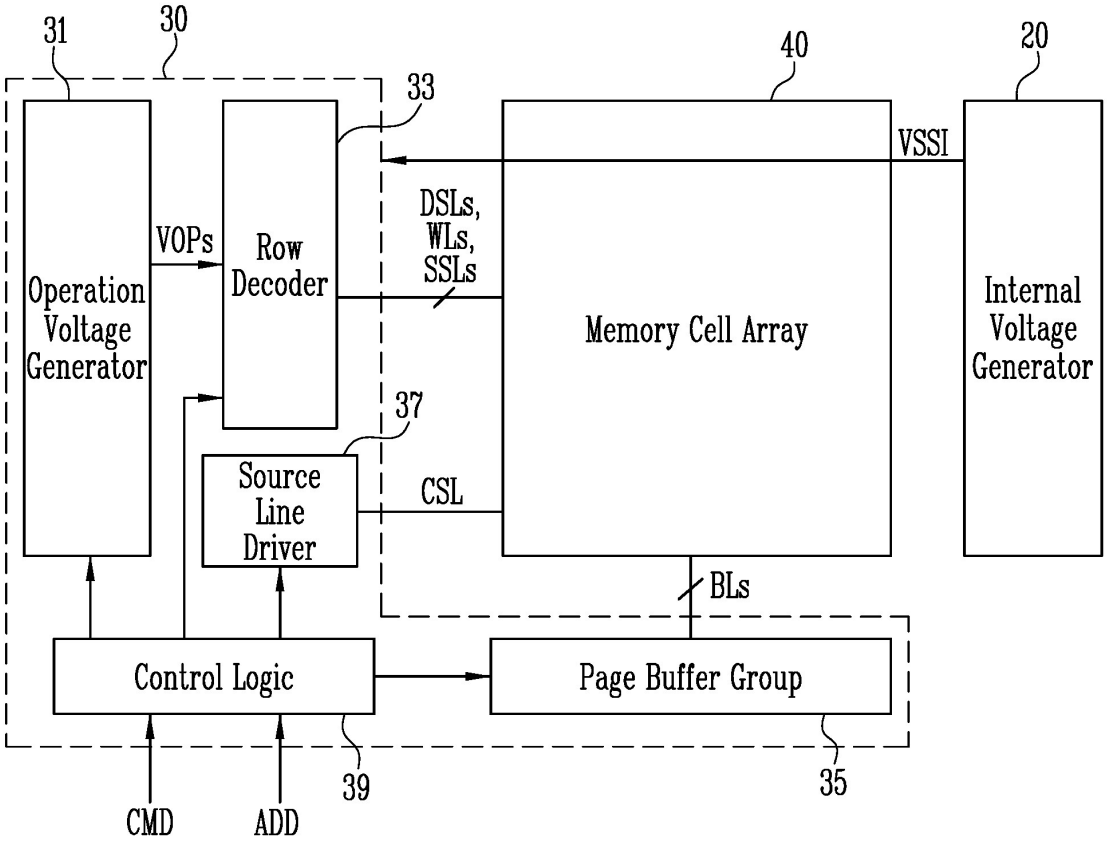

31
30
33
40
20
VSSI
DSLs,
WLs,
SSLs
VOPs
Row
Decoder
Operation
Voltage
Generator
Memory Cell Array
Internal
Voltage
Generator
37
Source
Line
Driver
CSL
BLs
Control Logic
Page Buffer Group
39
35
CMD
ADD

FIG. 3

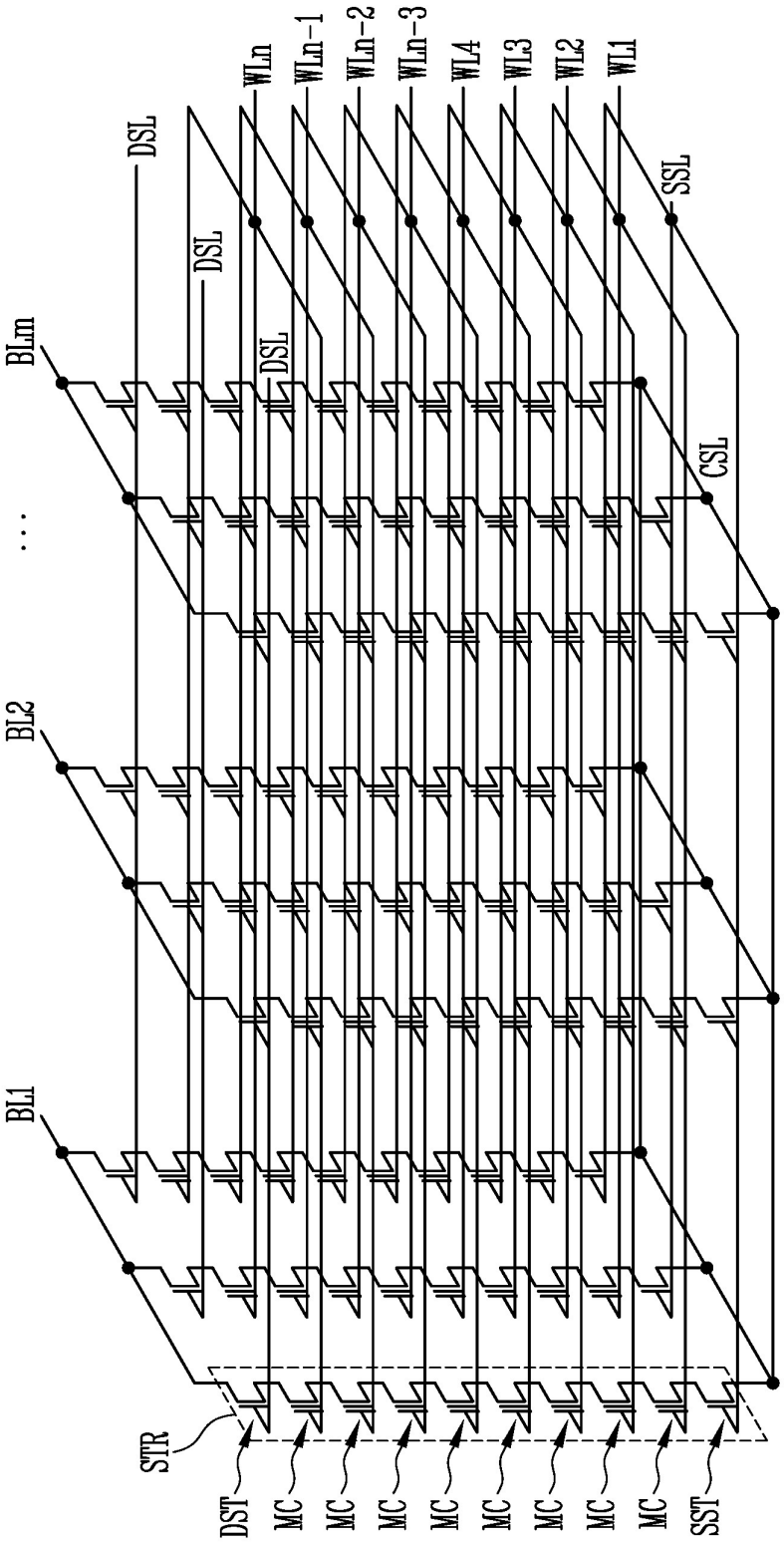

BLm
BL2
BL1
DSL
DSL
DSL
WLn
WLn-1
WLn-2
WLn-3
WL4
WL3
WL2
WL1
SSL
CSL
STR
DST
MC
MC
MC
MC
MC
MC
MC
MC
SST

FIG. 4

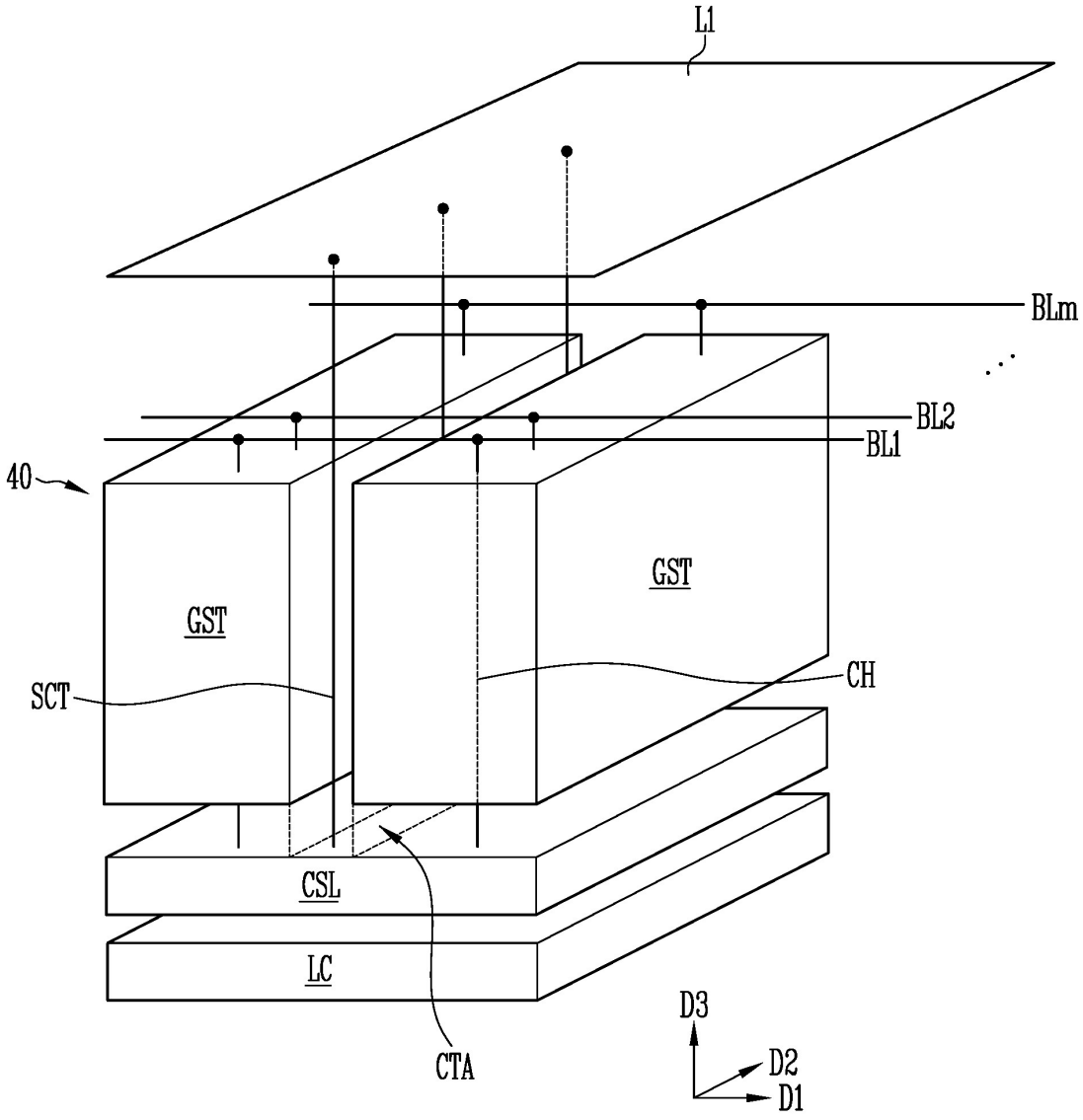


FIG. 5

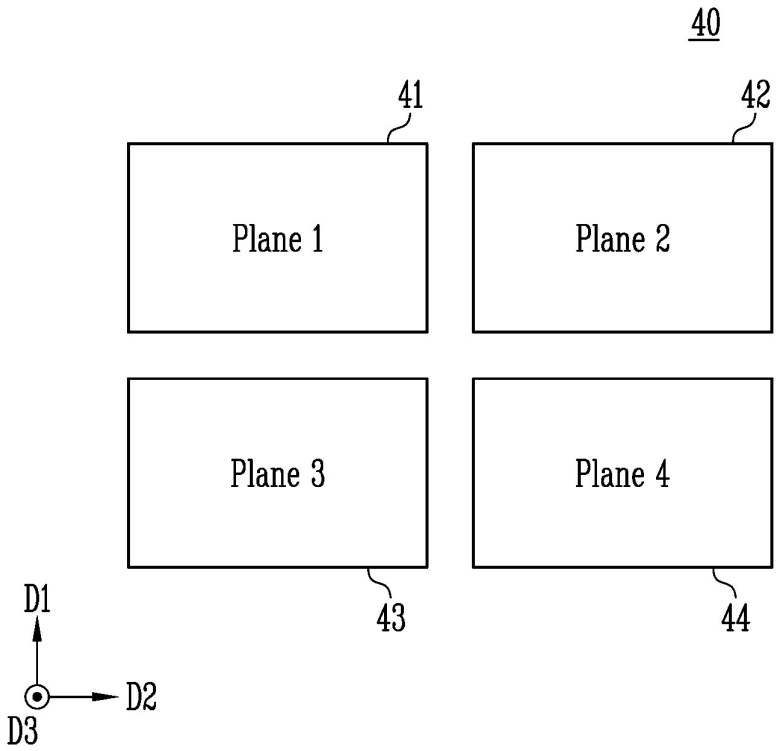


FIG. 6

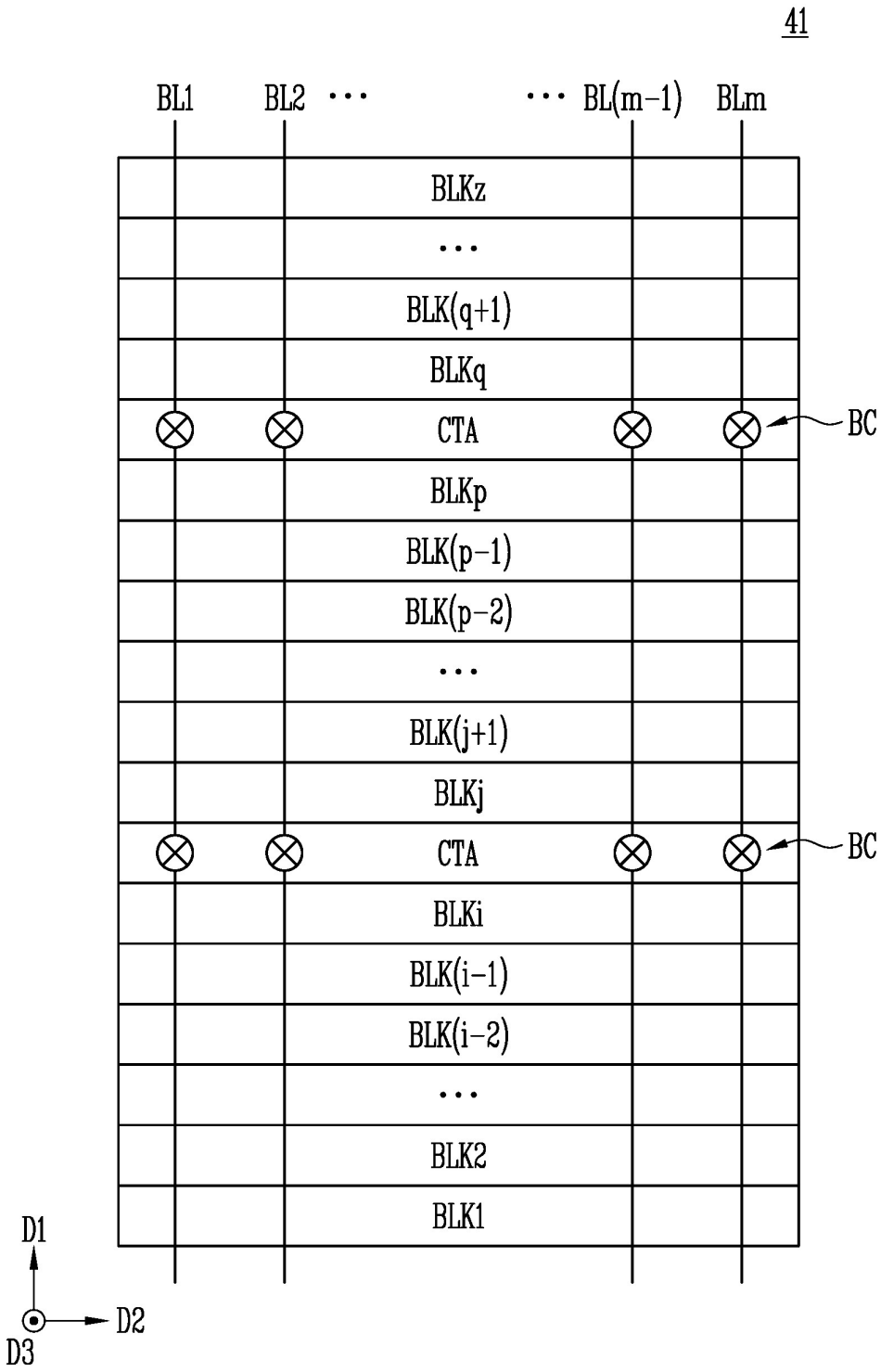

41
BL1
BL2
BL(m-1)
BLm
BLKz
BLK(q+1)
BLKq
CTA
BC
BLKp
BLK(p-1)
BLK(p-2)
BLK(j+1)
BLKj
CTA
BC
BLKi
BLK(i-1)
BLK(i-2)
BLK2
BLK1
D1
D2
D3

FIG. 7

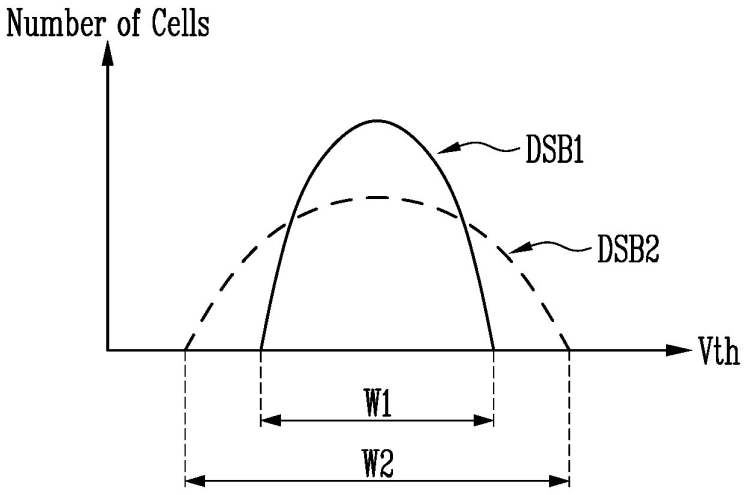

Number of Cells
DSB1
DSB2
Vth
W1
W2

FIG. 8

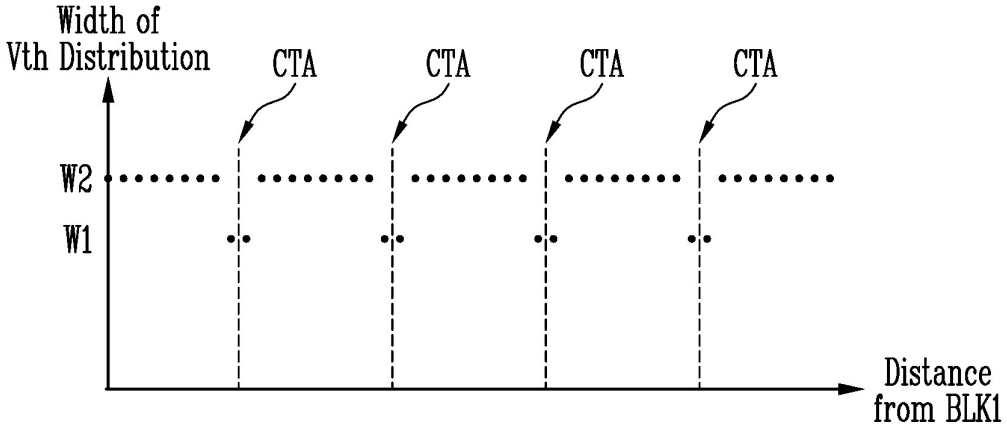

Width of
Vth Distribution
CTA
CTA
CTA
CTA
W2
W1
Distance
from BLK1

FIG. 9

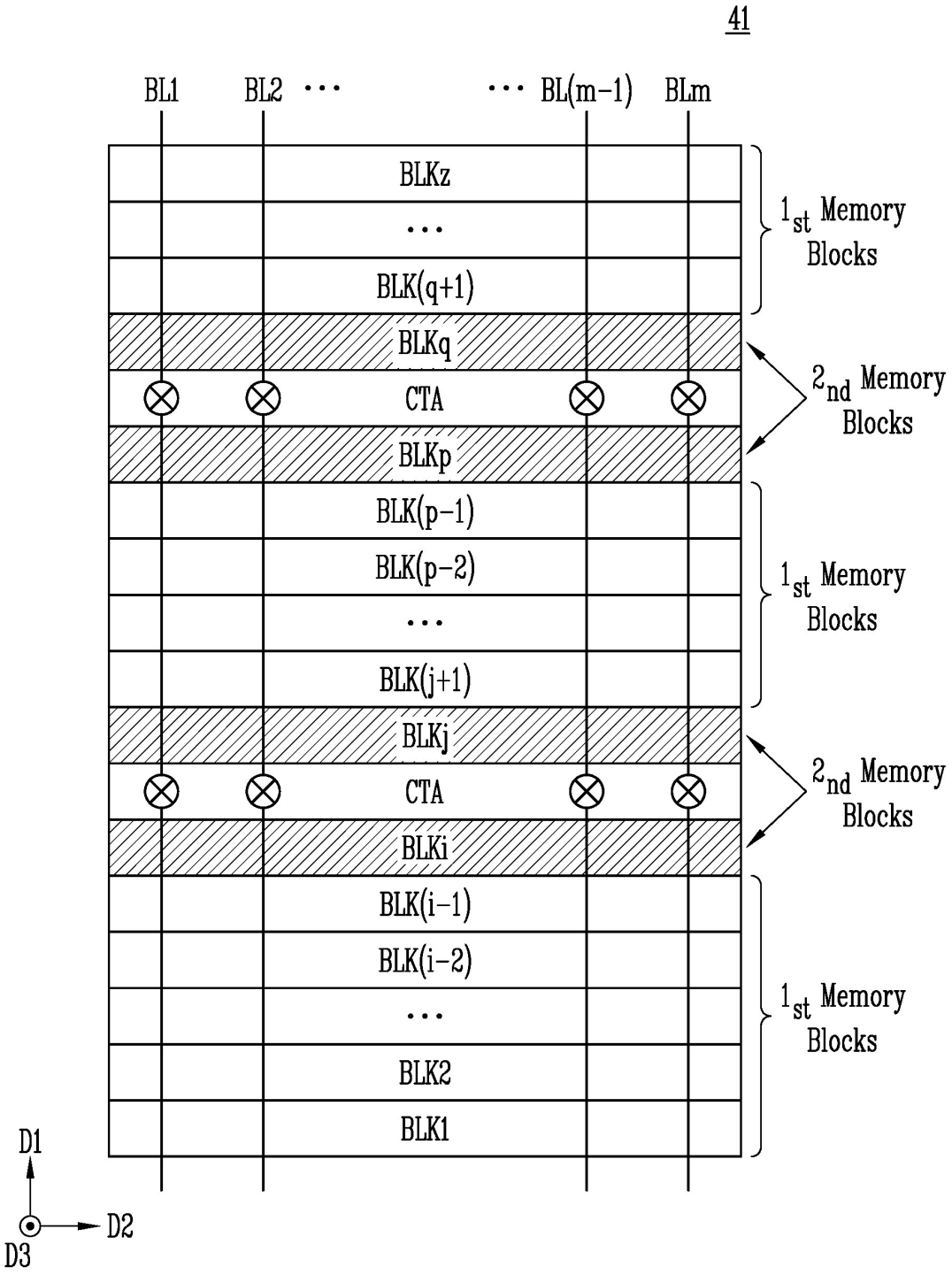

41
BL1
BL2
BL(m-1)
BLm
BLKz
BLK(q+1)
BLKq
CTA
BLKp
BLK(p-1)
BLK(p-2)
BLK(j+1)
BLKj
CTA
BLKi
BLK(i-1)
BLK(i-2)
BLK2
BLK1
1st Memory Blocks
2nd Memory Blocks
1st Memory Blocks
2nd Memory Blocks
1st Memory Blocks
D1
D2
D3

FIG. 10

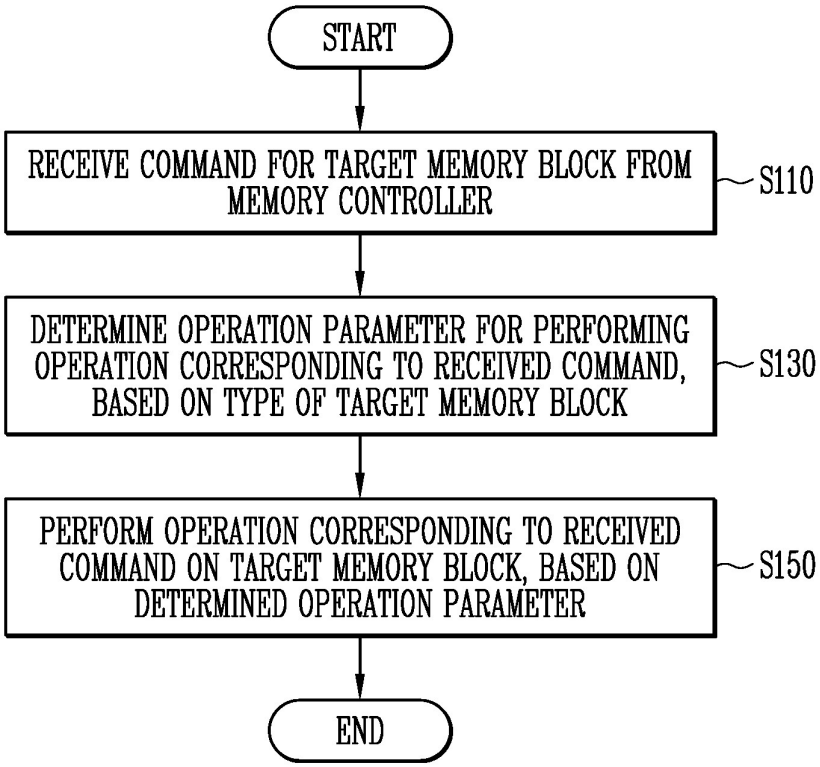

START
RECEIVE COMMAND FOR TARGET MEMORY BLOCK FROM MEMORY CONTROLLER
S110
DETERMINE OPERATION PARAMETER FOR PERFORMING OPERATION CORRESPONDING TO RECEIVED COMMAND, BASED ON TYPE OF TARGET MEMORY BLOCK
S130
PERFORM OPERATION CORRESPONDING TO RECEIVED COMMAND ON TARGET MEMORY BLOCK, BASED ON DETERMINED OPERATION PARAMETER
S150
END

FIG. 11

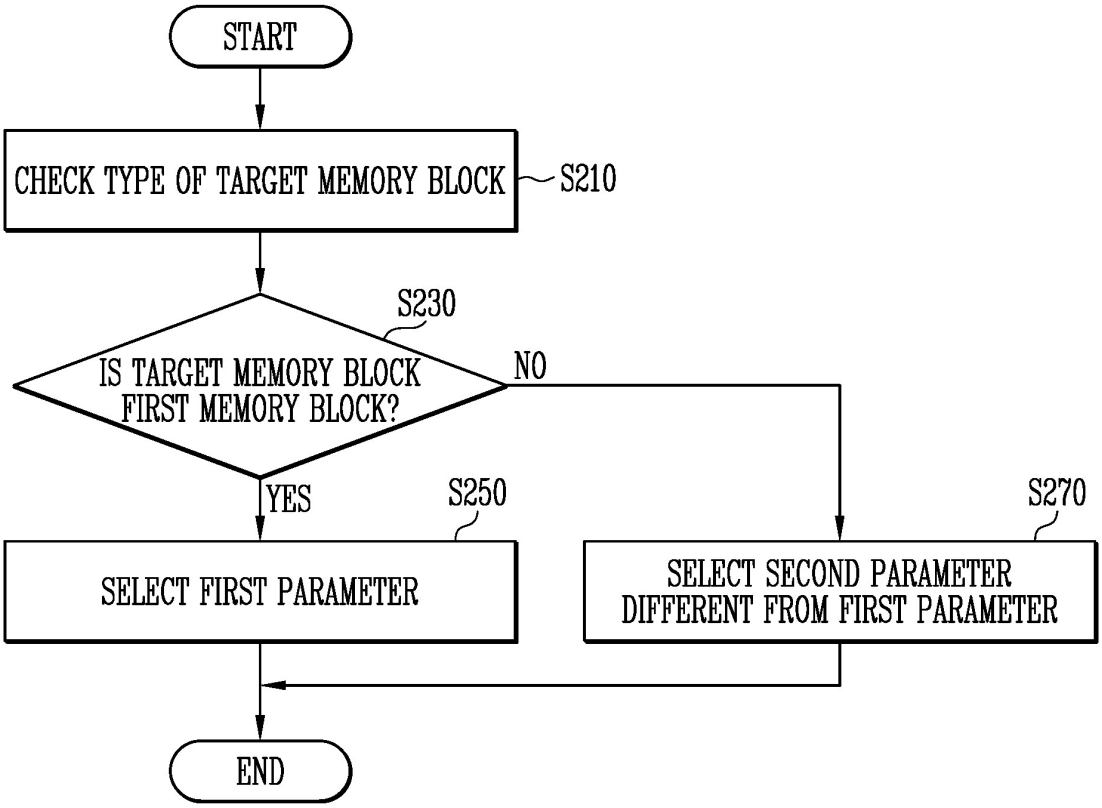

START
CHECK TYPE OF TARGET MEMORY BLOCK
S210
S230
IS TARGET MEMORY BLOCK FIRST MEMORY BLOCK?
NO
YES
S250
SELECT FIRST PARAMETER
S270
SELECT SECOND PARAMETER DIFFERENT FROM FIRST PARAMETER
END

FIG. 12

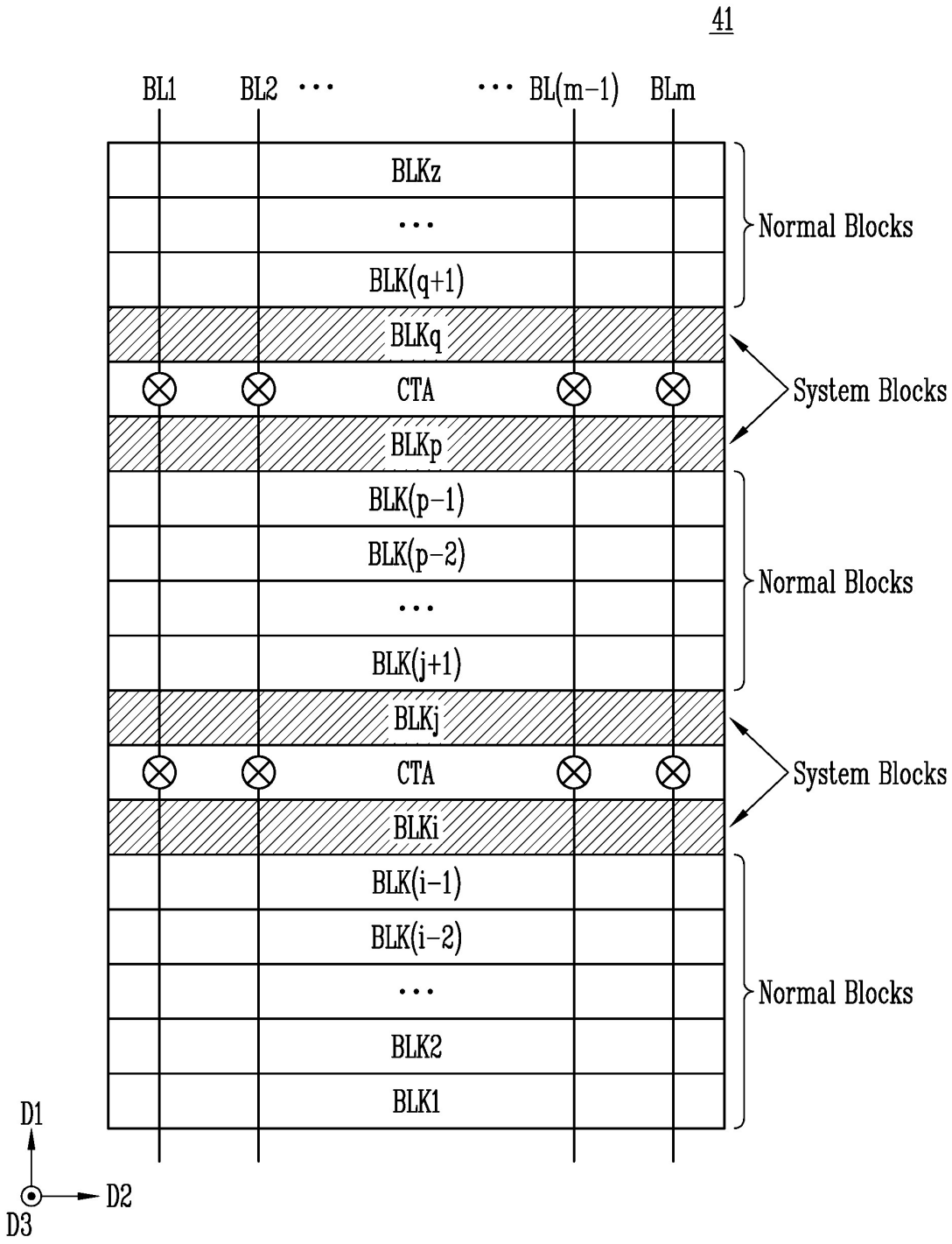

41
BL1
BL2
BL(m-1)
BLm
BLKz
BLK(q+1)
BLKq
CTA
BLKp
BLK(p-1)
BLK(p-2)
BLK(j+1)
BLKj
CTA
BLKi
BLK(i-1)
BLK(i-2)
BLK2
BLK1
Normal Blocks
System Blocks
Normal Blocks
System Blocks
Normal Blocks
D1
D2
D3

FIG. 13

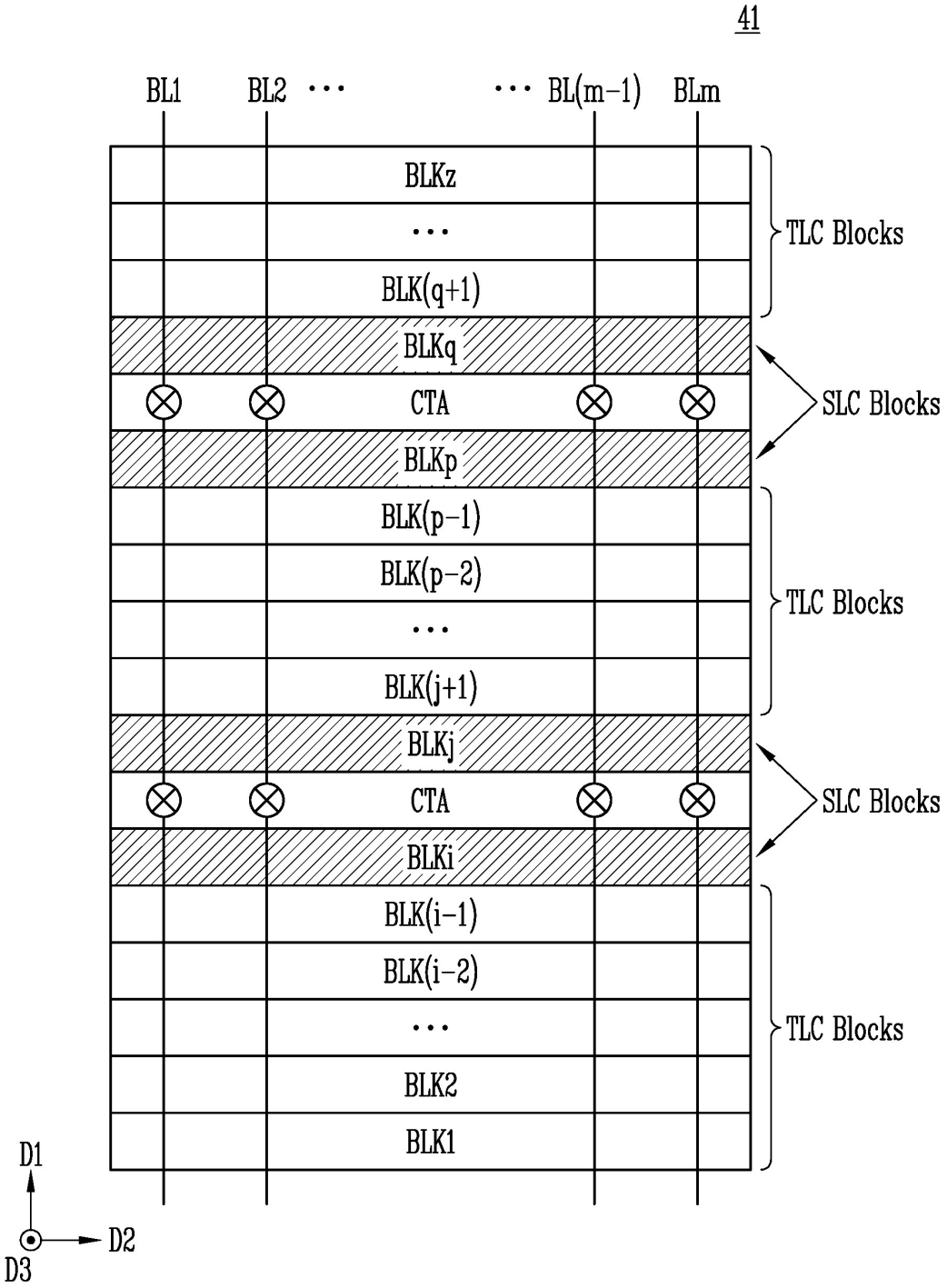

41
BL1
BL2
BL(m-1)
BLm
BLKz
BLK(q+1)
BLKq
CTA
BLKp
BLK(p-1)
BLK(p-2)
BLK(j+1)
BLKj
CTA
BLKi
BLK(i-1)
BLK(i-2)
BLK2
BLK1
TLC Blocks
SLC Blocks
TLC Blocks
SLC Blocks
TLC Blocks
D1
D2
D3

FIG. 14

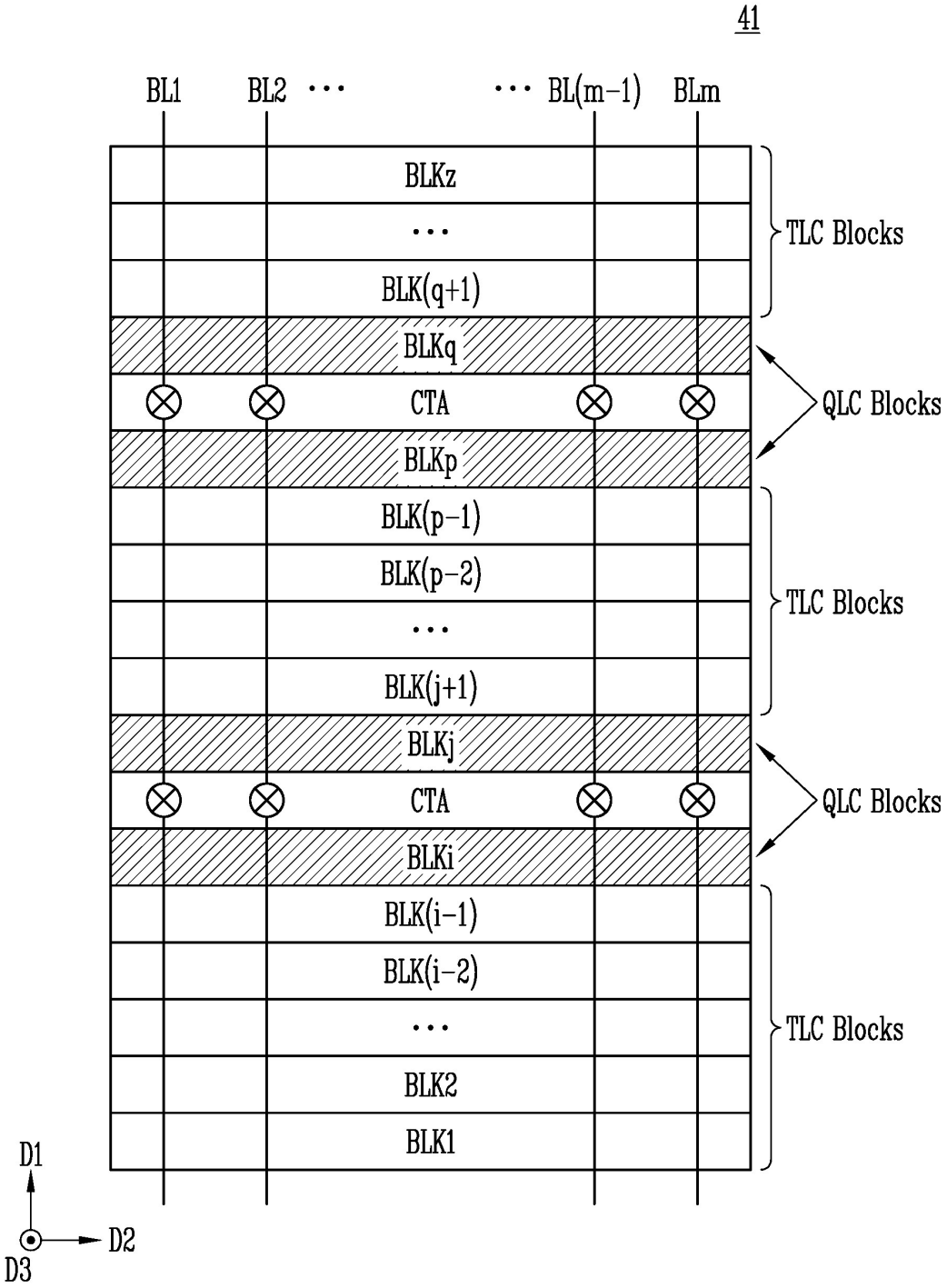

41
BL1
BL2
BL(m-1)
BLm
BLKz
BLK(q+1)
BLKq
CTA
BLKp
BLK(p-1)
BLK(p-2)
BLK(j+1)
BLKj
CTA
BLKi
BLK(i-1)
BLK(i-2)
BLK2
BLK1
TLC Blocks
QLC Blocks
TLC Blocks
QLC Blocks
TLC Blocks
D1
D2
D3

FIG. 15

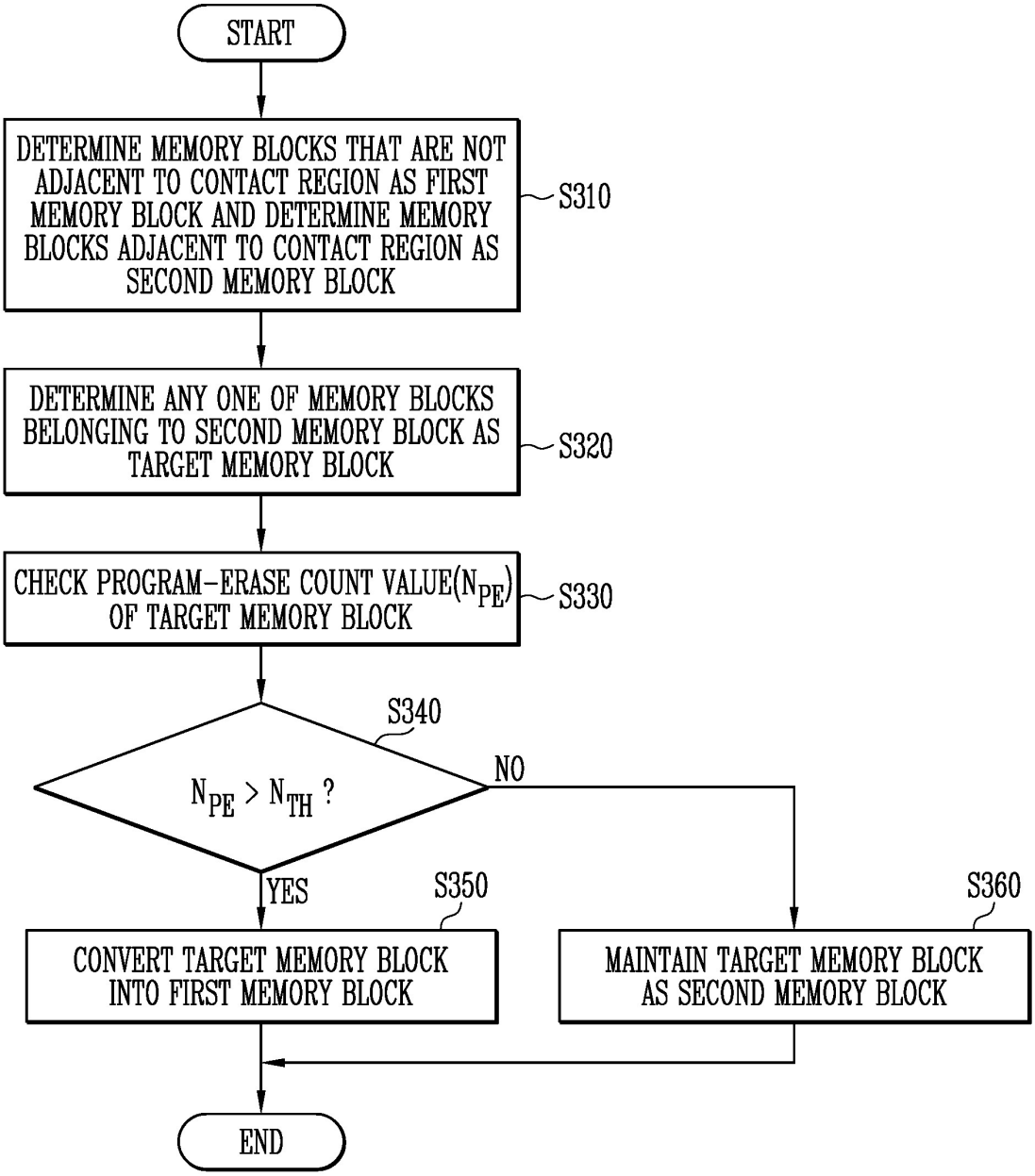

START
DETERMINE MEMORY BLOCKS THAT ARE NOT ADJACENT TO CONTACT REGION AS FIRST MEMORY BLOCK AND DETERMINE MEMORY BLOCKS ADJACENT TO CONTACT REGION AS SECOND MEMORY BLOCK
S310
DETERMINE ANY ONE OF MEMORY BLOCKS BELONGING TO SECOND MEMORY BLOCK AS TARGET MEMORY BLOCK
S320
CHECK PROGRAM-ERASE COUNT VALUE(N_{PE}) OF TARGET MEMORY BLOCK
S330
S340
$N_{PE} > N_{TH}$?
NO
YES
S350
CONVERT TARGET MEMORY BLOCK INTO FIRST MEMORY BLOCK
S360
MAINTAIN TARGET MEMORY BLOCK AS SECOND MEMORY BLOCK
END

FIG. 16

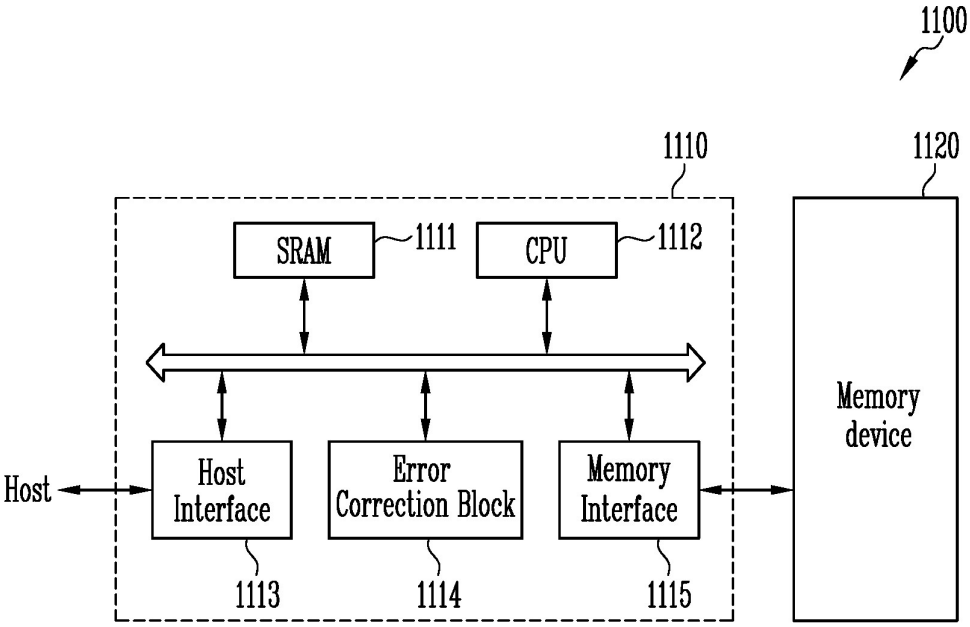
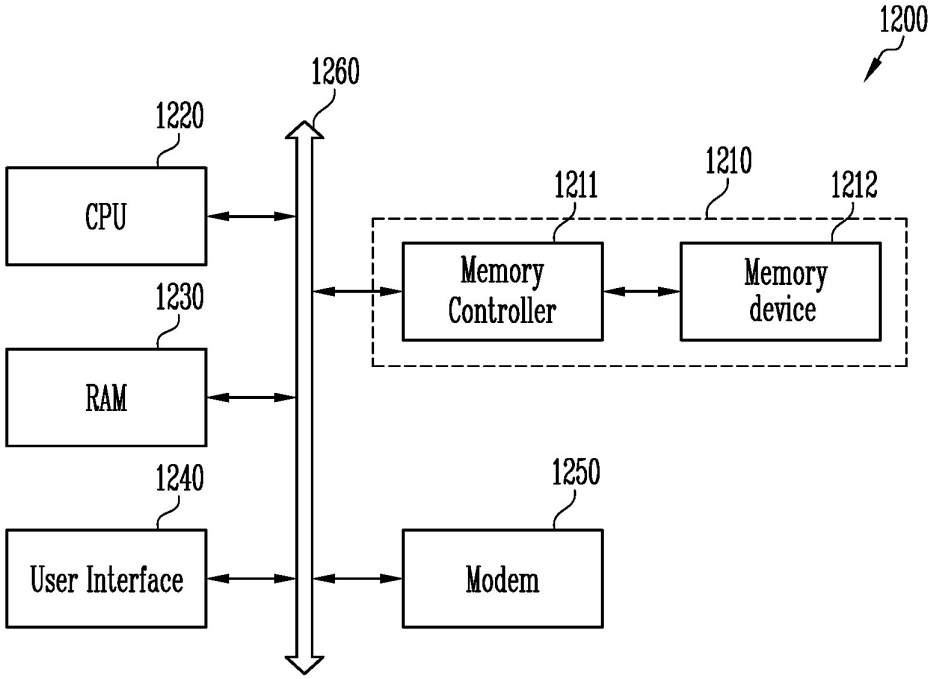

1100
1110
1120
SRAM
1111
CPU
1112
Memory device
Host
Host Interface
Error Correction Block
Memory Interface
1113
1114
1115

FIG. 17


1200
1260
1220
CPU
1211
1210
1212
Memory Controller
Memory device
1230
RAM
1240
1250
User Interface
Modem