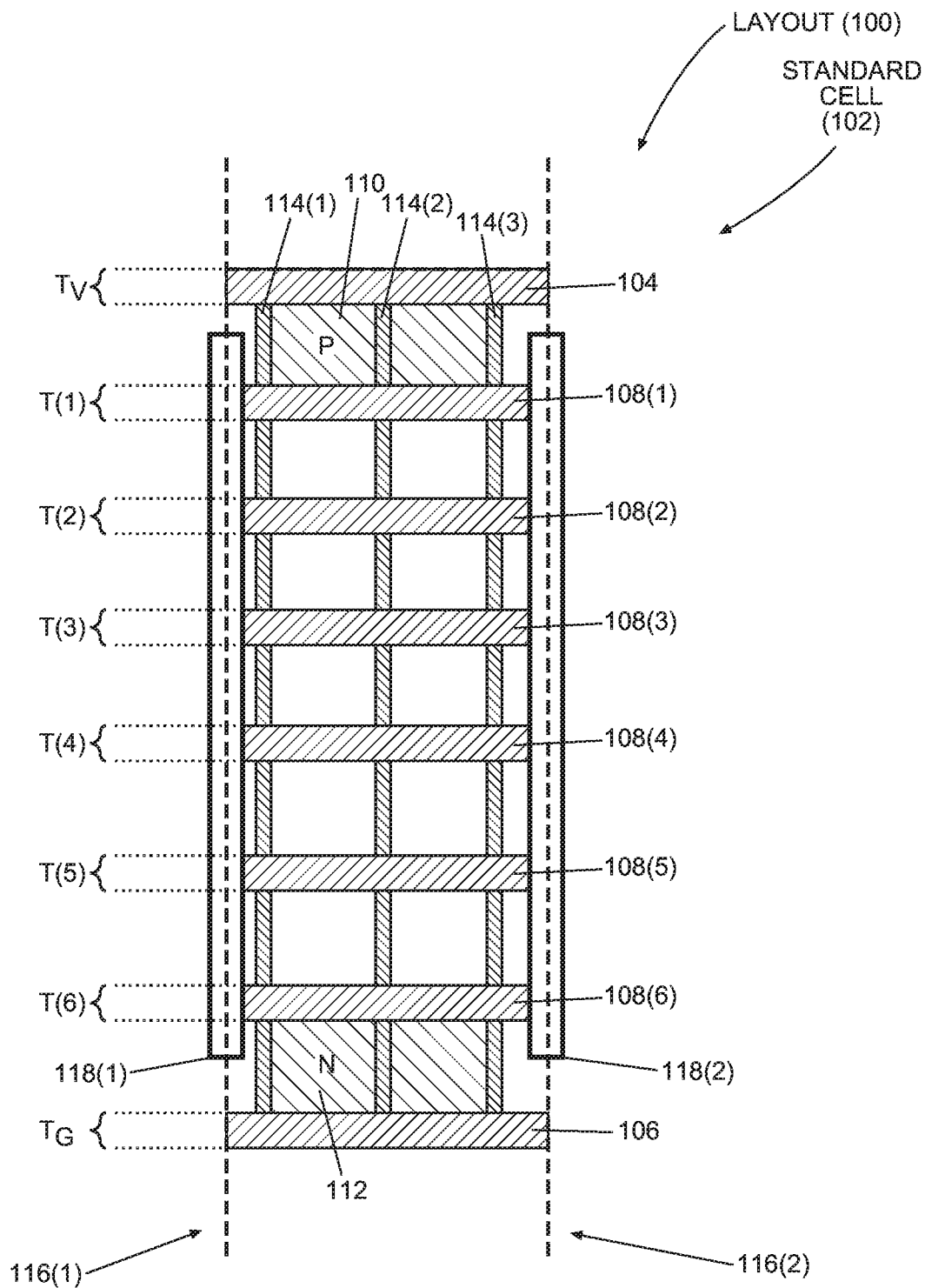


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**FIG. 1**

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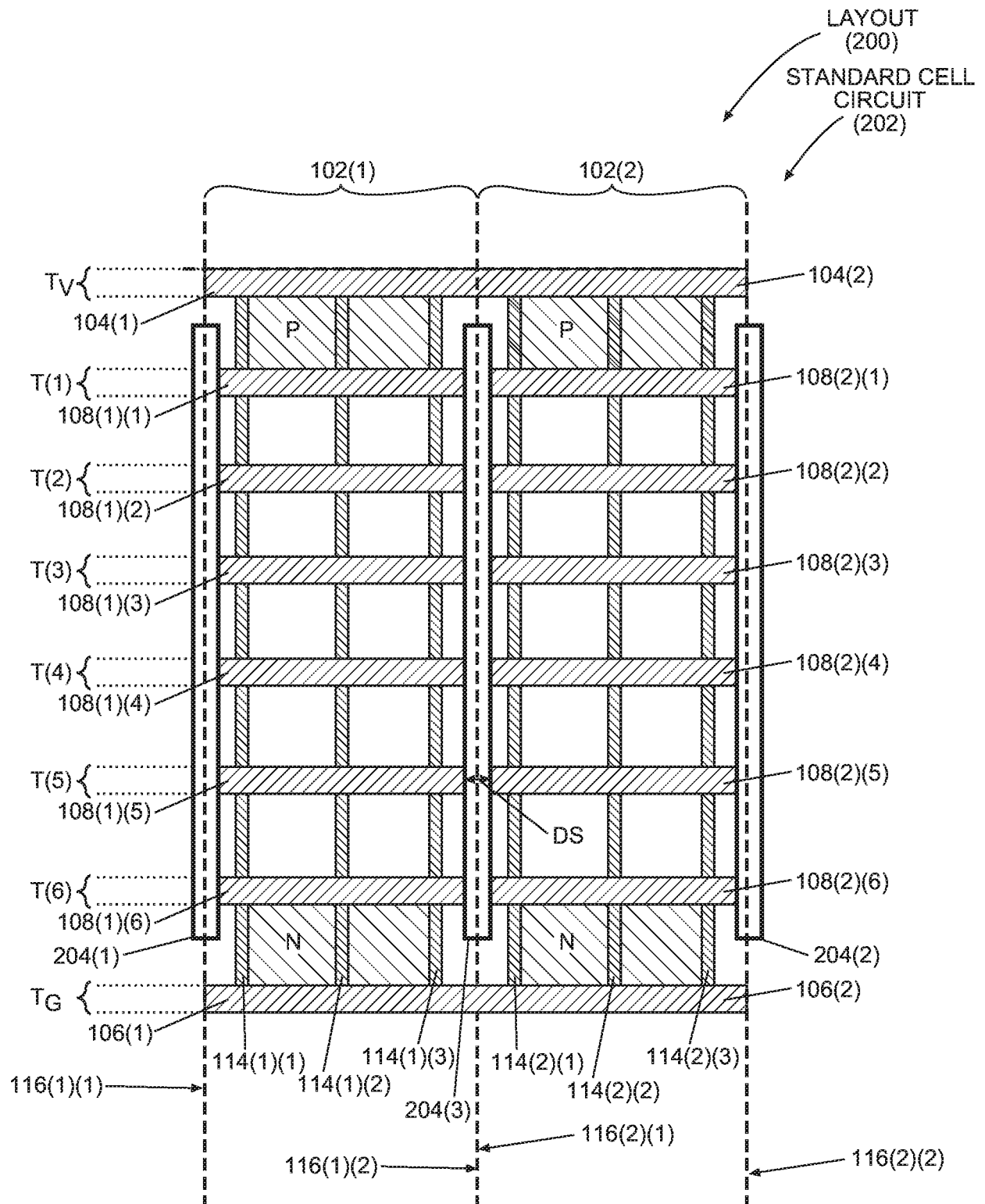
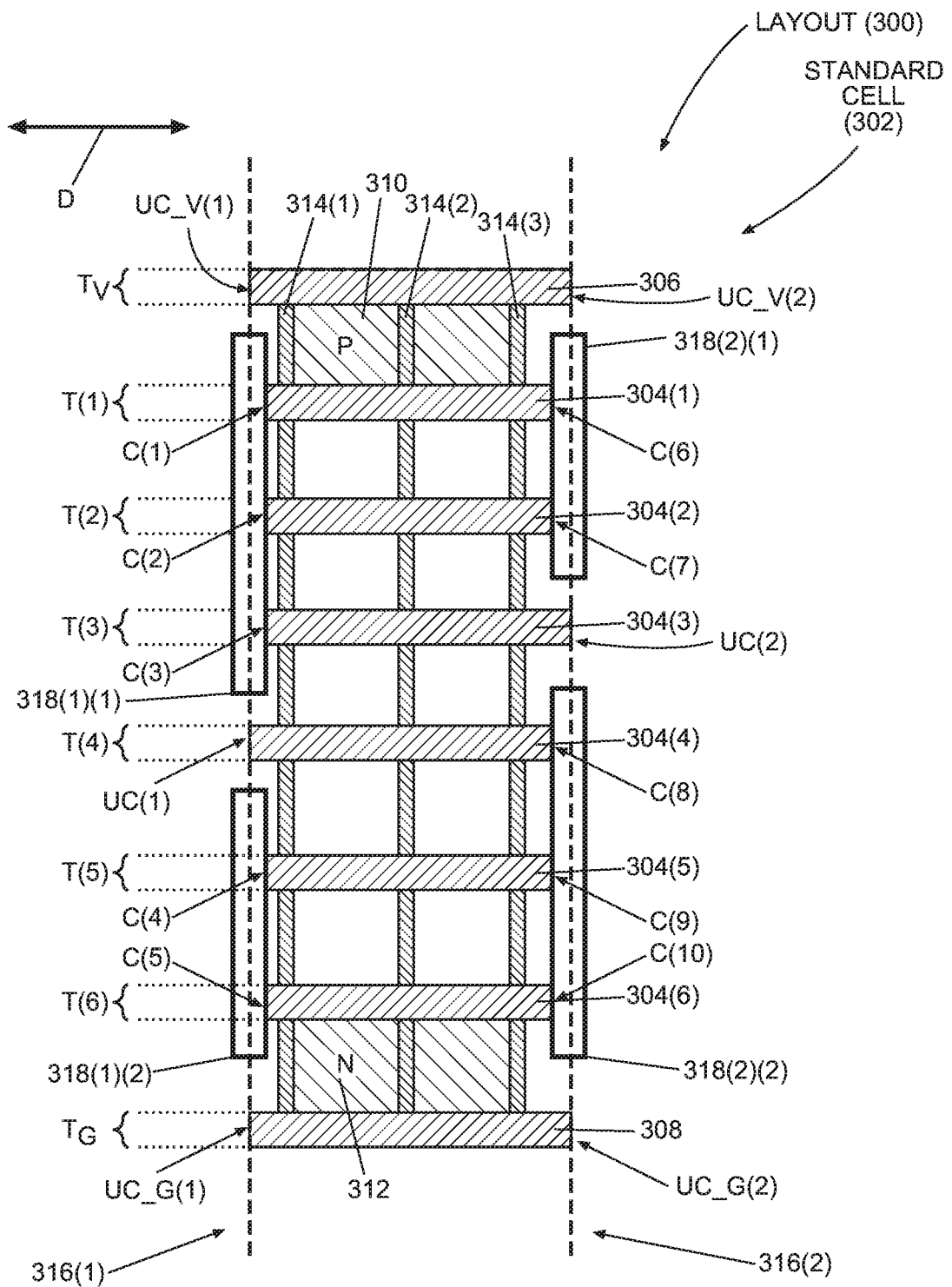


FIG. 2

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**FIG. 3**

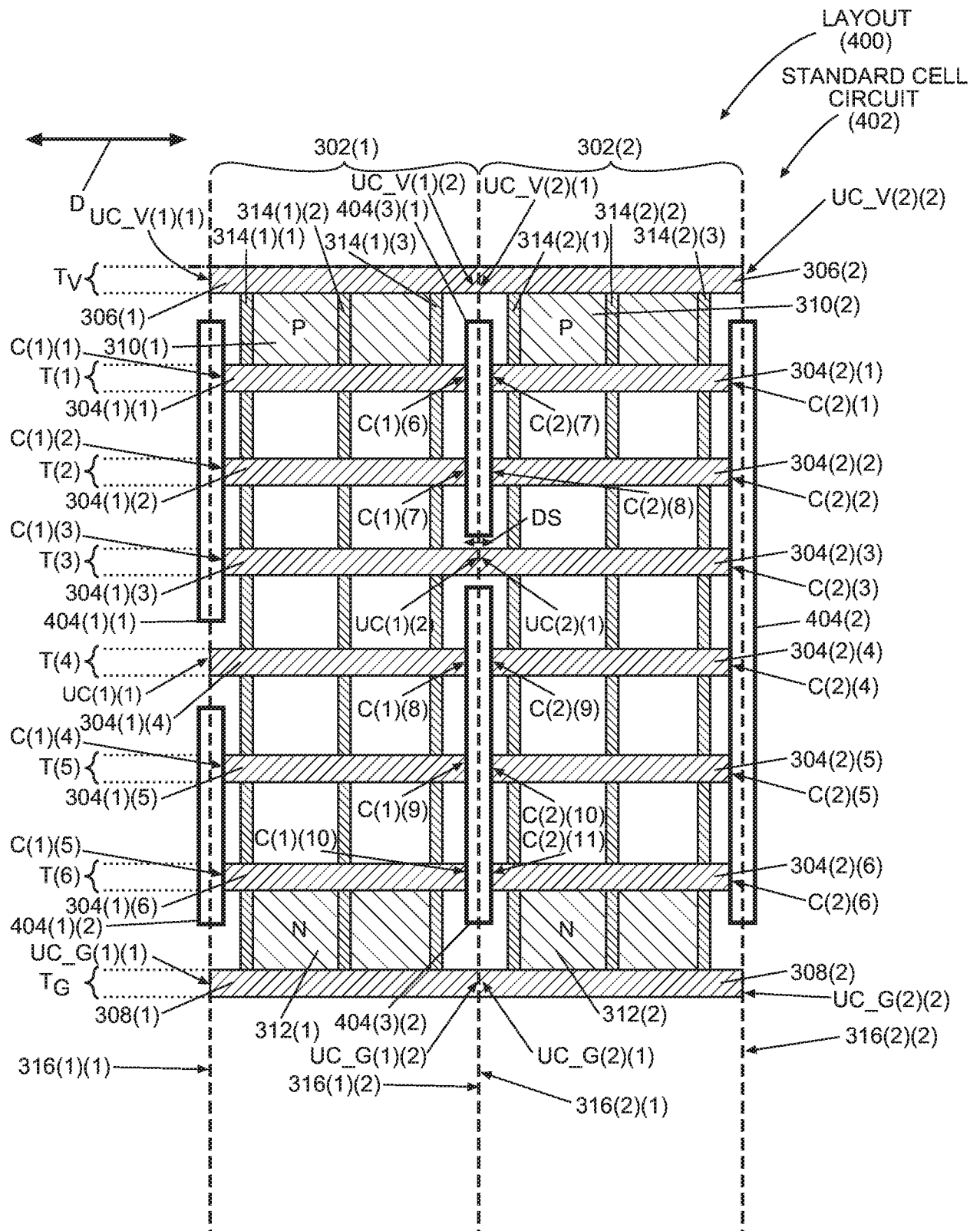


FIG. 4

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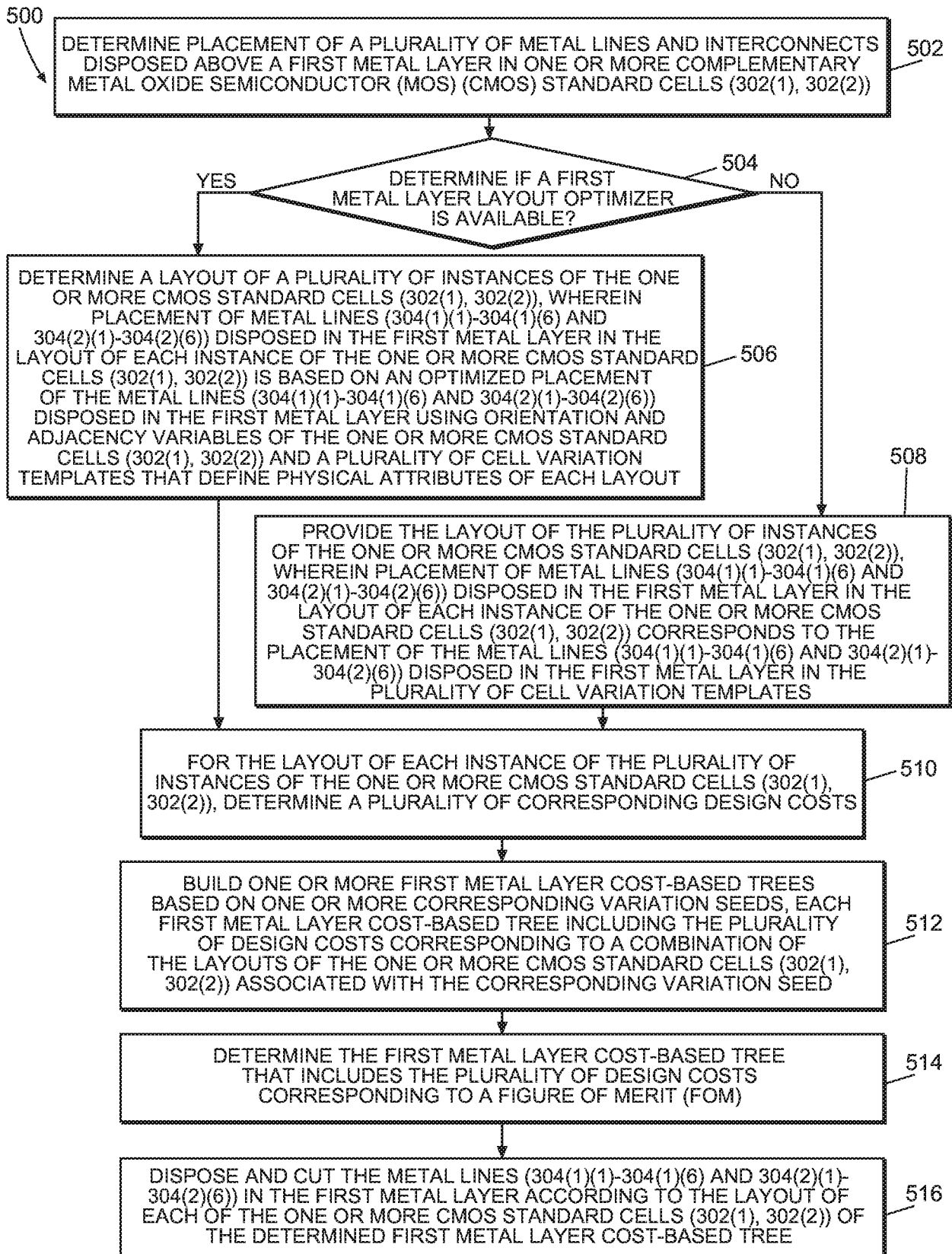


FIG. 5

600

602(1) 602(2)

INVERTER	
INPUT	3 (T(3))
OUTPUT	1, 6 (T(1), T(6))
OPEN	2,4,5 (T(2), T(4), T(5))
BLOCKED	0,7 (T _V , T _G)
BLOCKEDL	
BLOCKEDR	

604(1) 604(2) 604(3) 604(4) 604(5) 604(6)

FIG. 6

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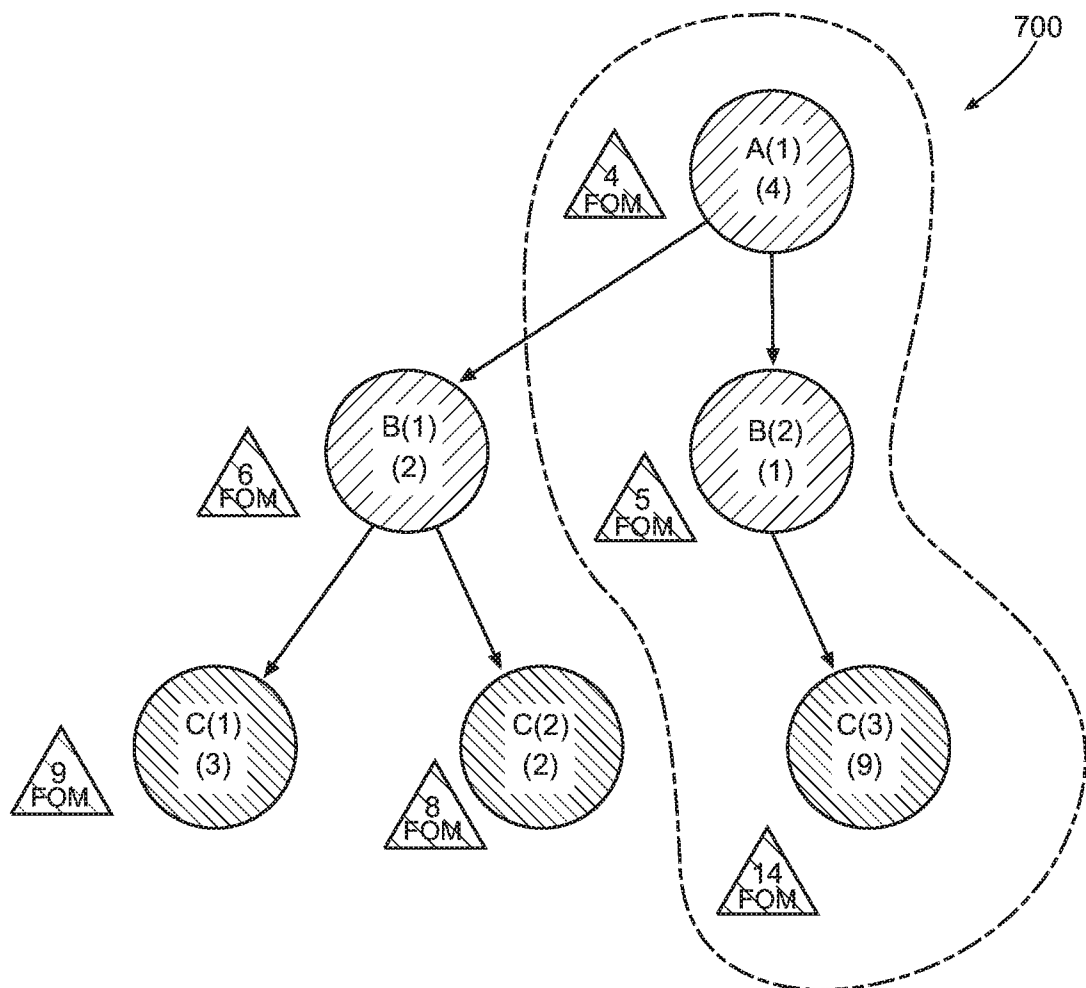


FIG. 7

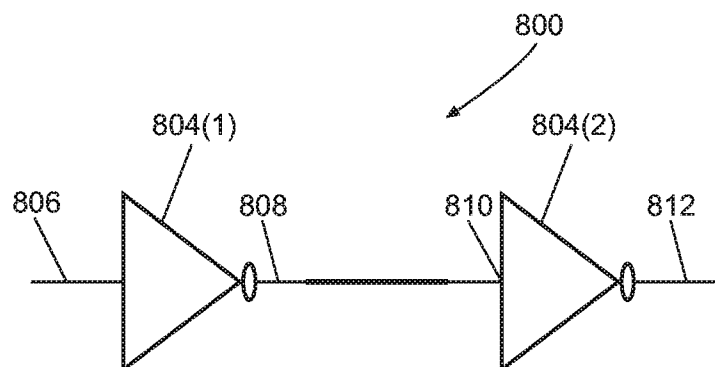


FIG. 8A

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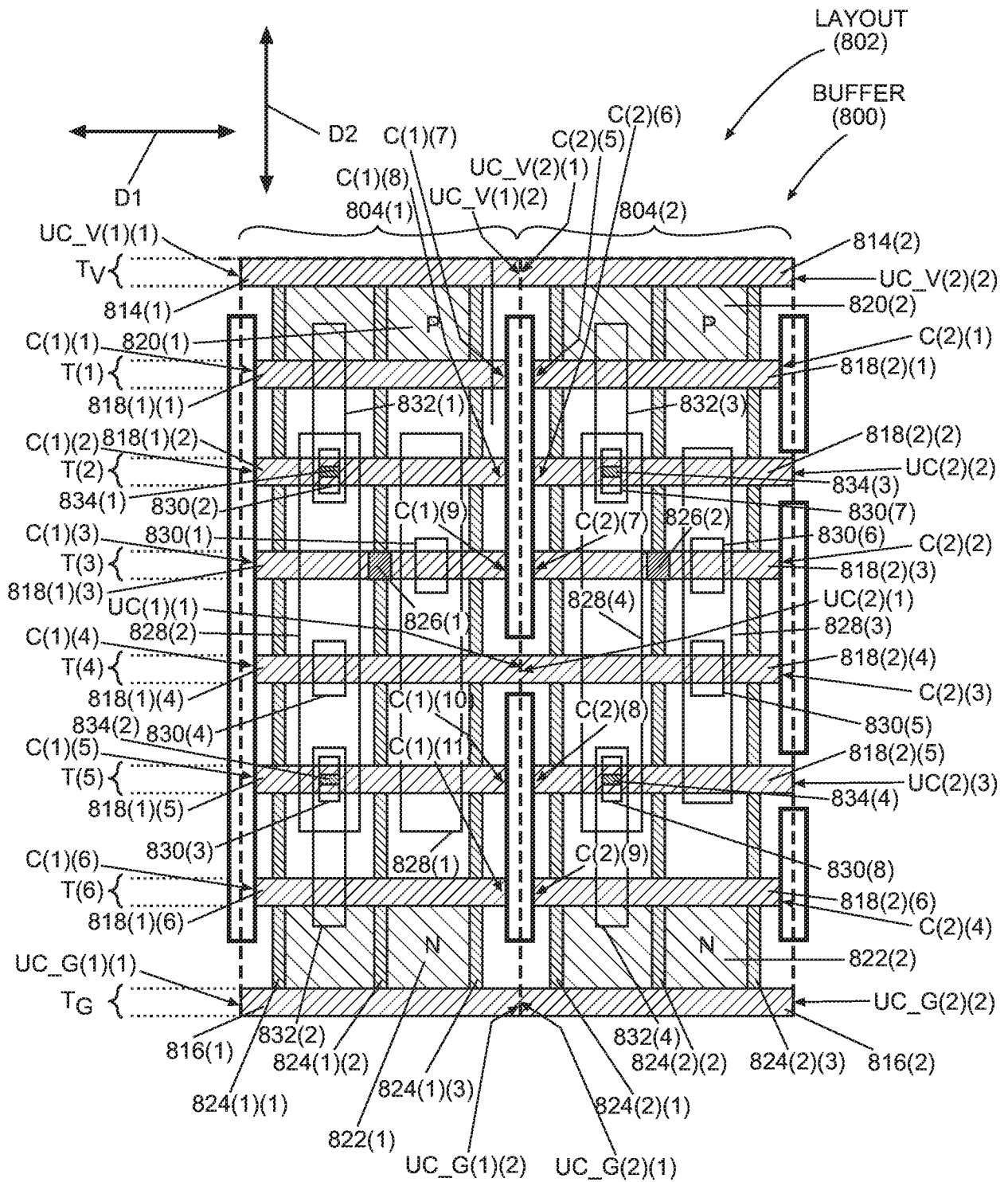


FIG. 8B

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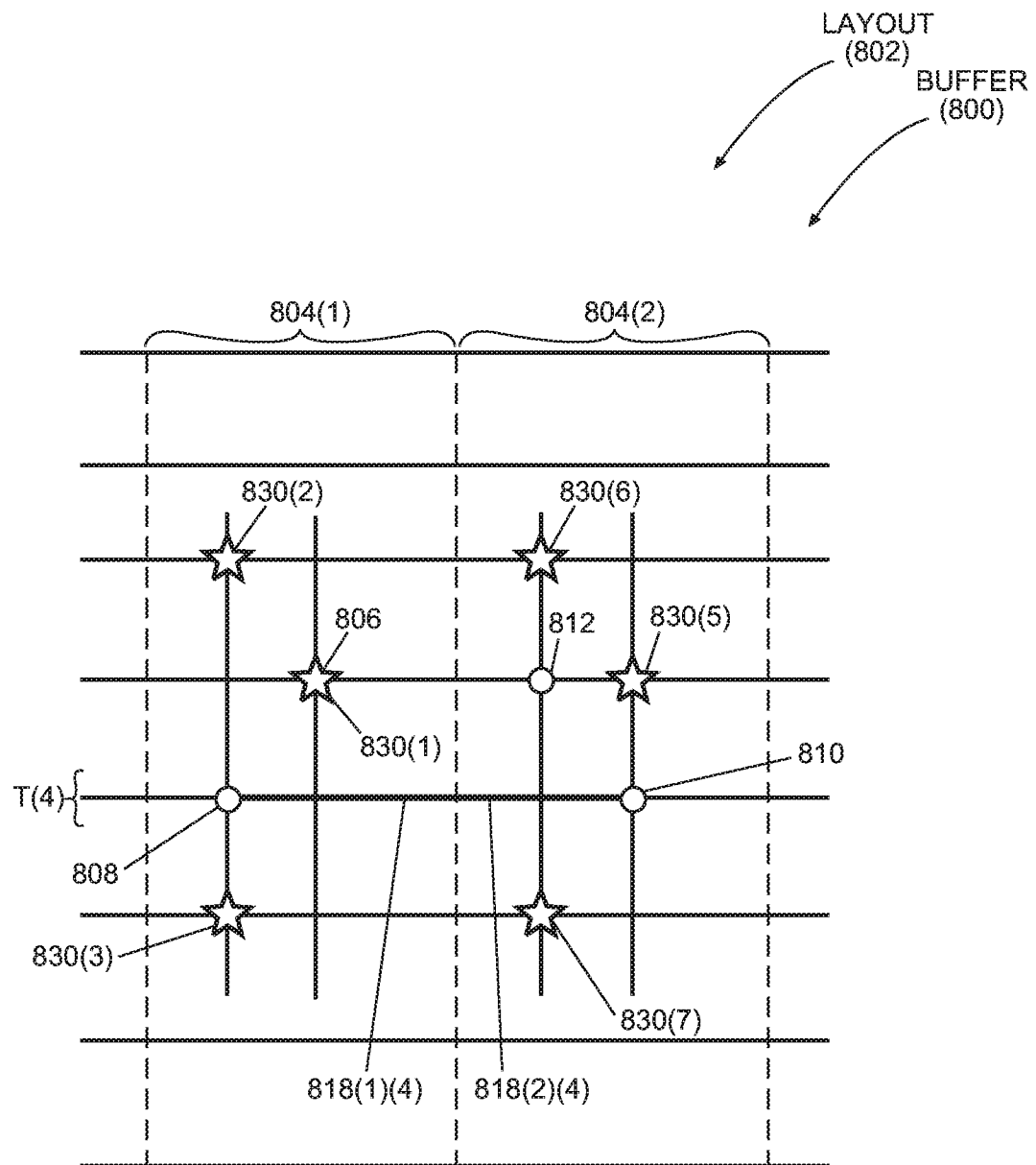


FIG. 8C

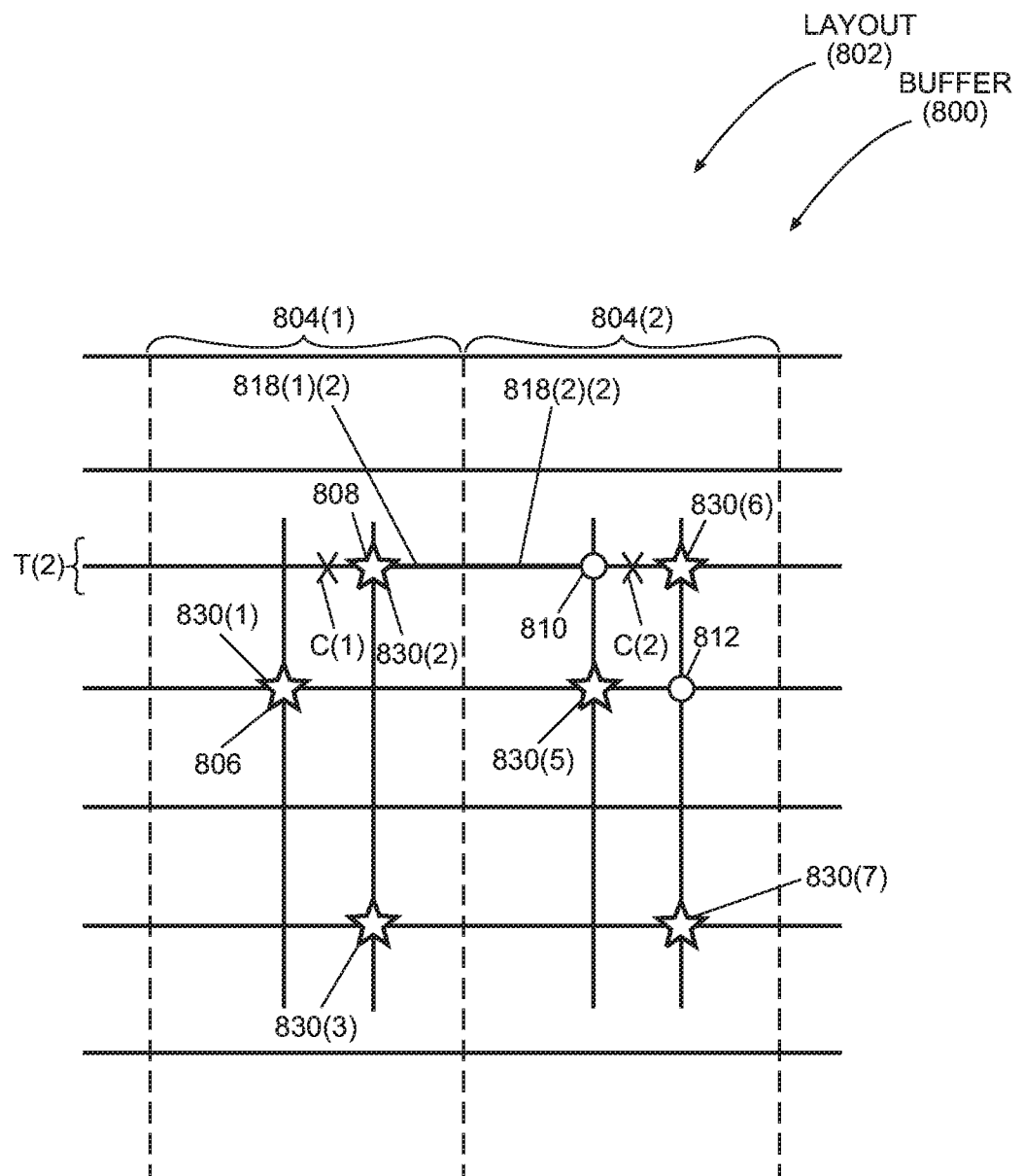


FIG. 8D

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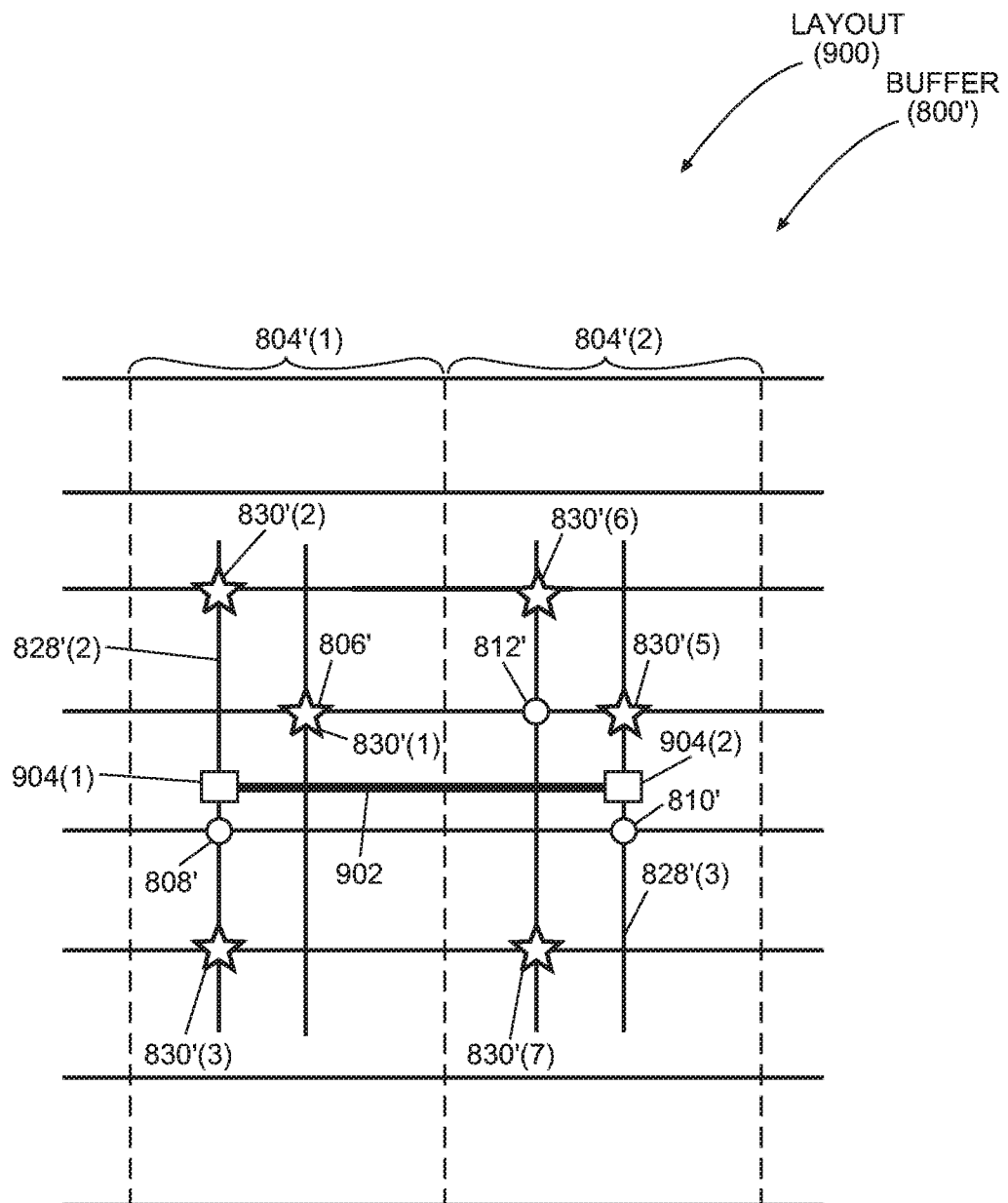


FIG. 9

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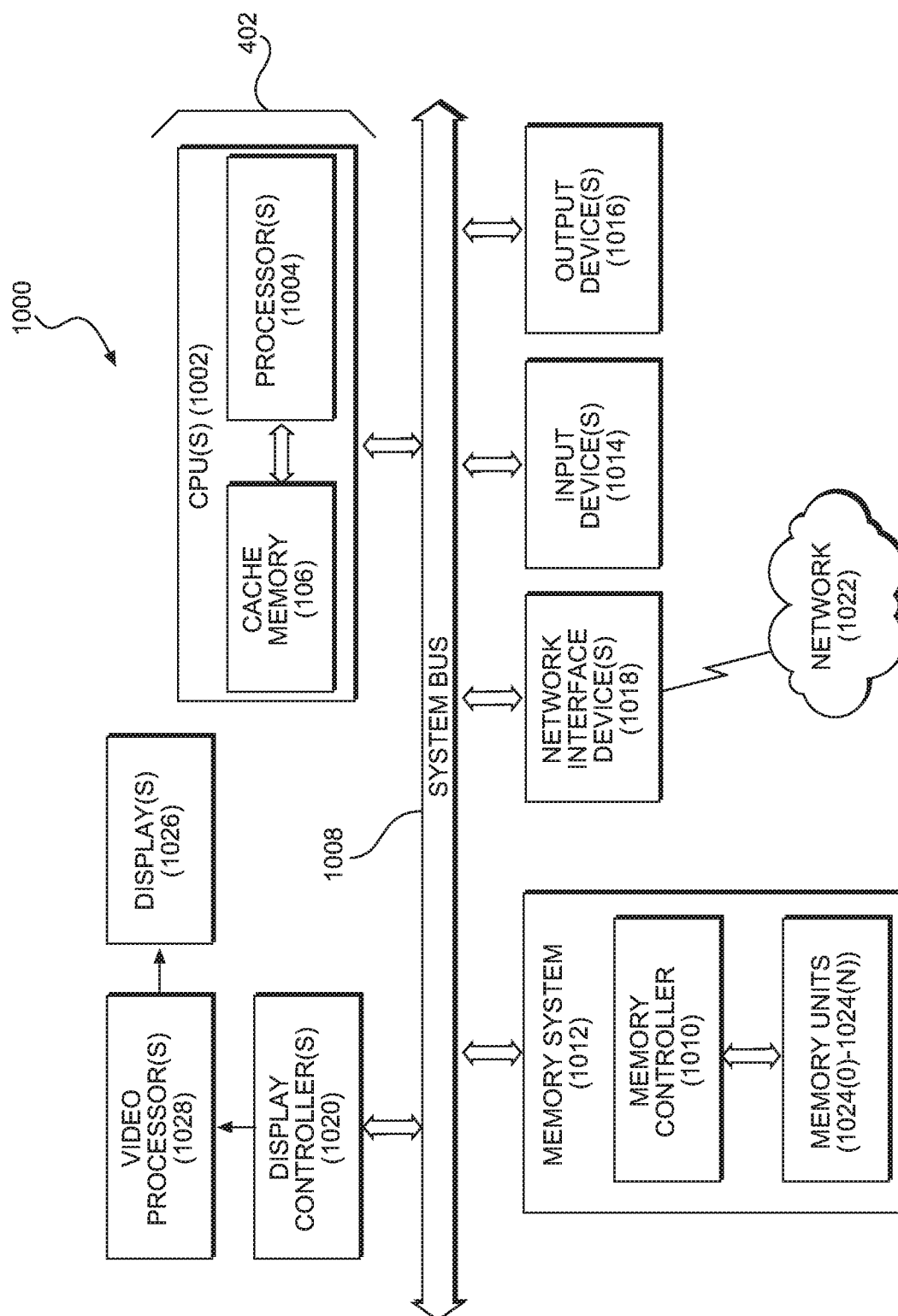


FIG. 10

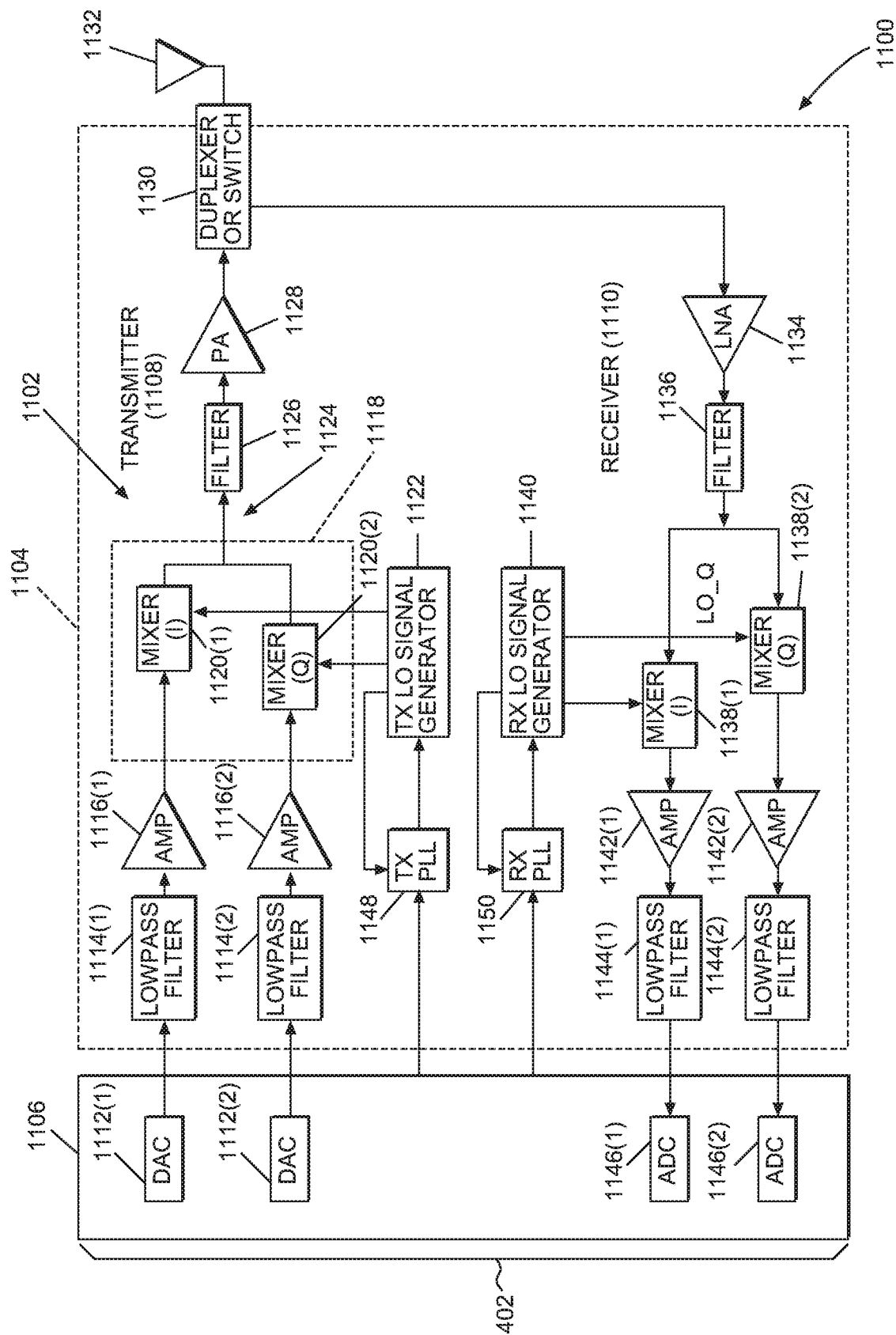


FIG. 11