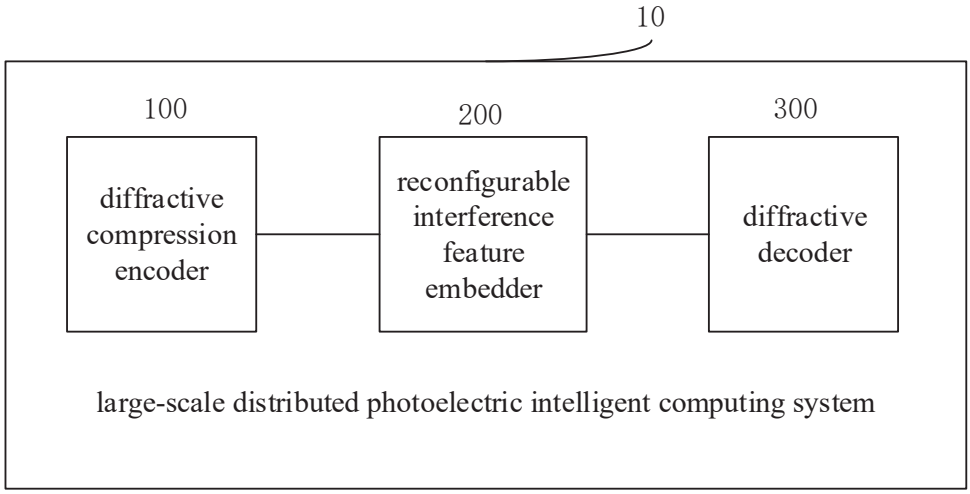

10
100
200
300
diffractive compression encoder
reconfigurable interference feature embedder
diffractive decoder
large-scale distributed photoelectric intelligent computing system

FIG. 1

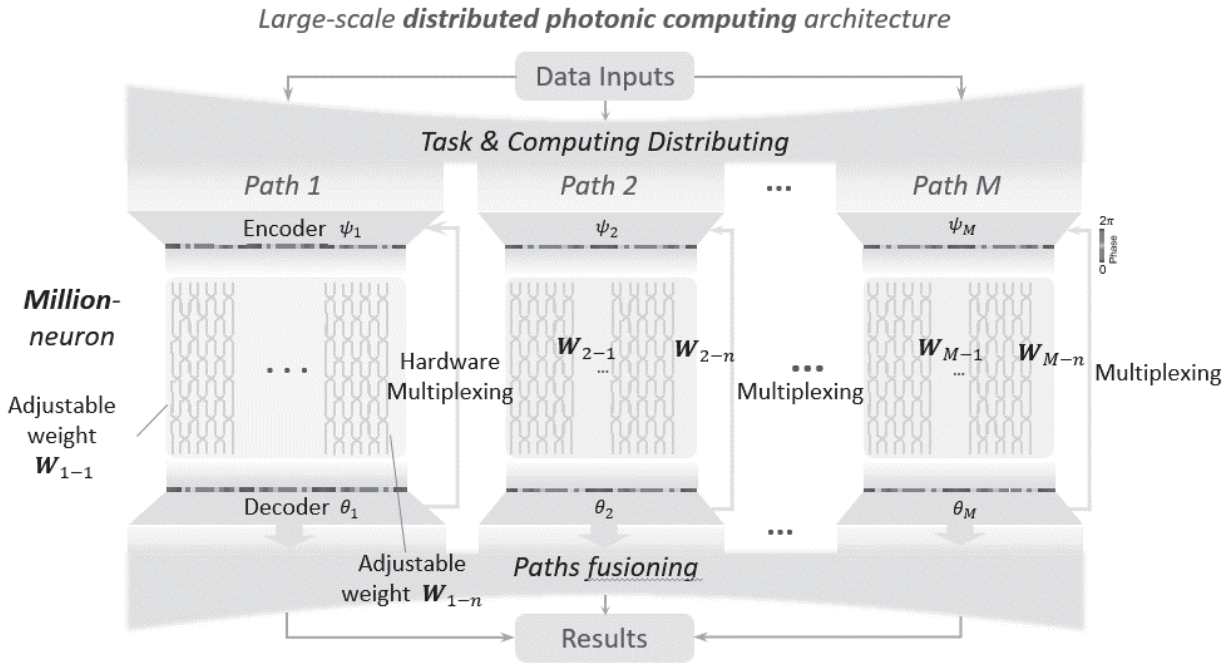

Large-scale distributed photonic computing architecture
Data Inputs
Task & Computing Distributing
Path 1
Path 2
Path M
Encoder ψ_1
ψ_2
ψ_M
Million-neuron
Adjustable weight W_{1-1}
Hardware Multiplexing
W_{2-1}
W_{2-n}
Multiplexing
W_{M-1}
W_{M-n}
Multiplexing
Decoder θ_1
θ_2
θ_M
Adjustable weight W_{1-n}
Paths fusioning
Results

FIG. 2

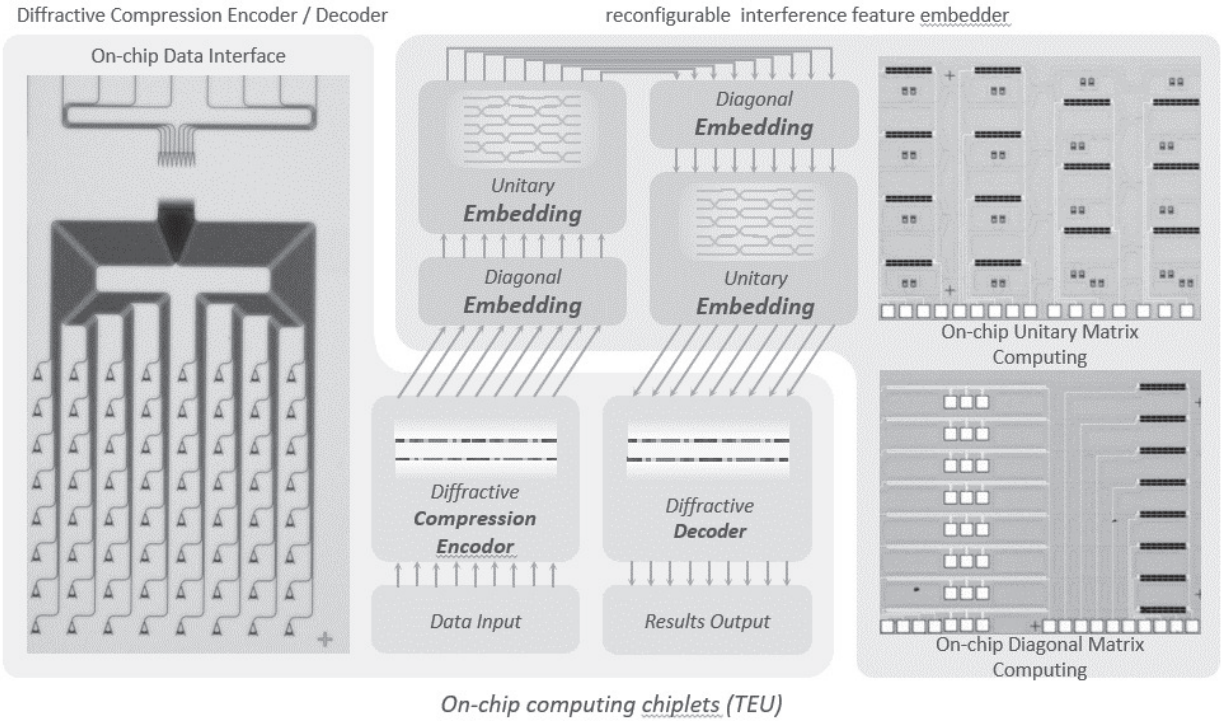

Diffractive Compression Encoder / Decoder
reconfigurable interference feature embedder
On-chip Data Interface
Unitary
Embedding
Diagonal
Embedding
Diagonal
Embedding
Unitary
Embedding
On-chip Unitary Matrix
Computing
Diffractive
Compression
Encodor
Diffractive
Decoder
Data Input
Results Output
On-chip Diagonal Matrix
Computing
On-chip computing chiplets (TEU)

FIG. 3

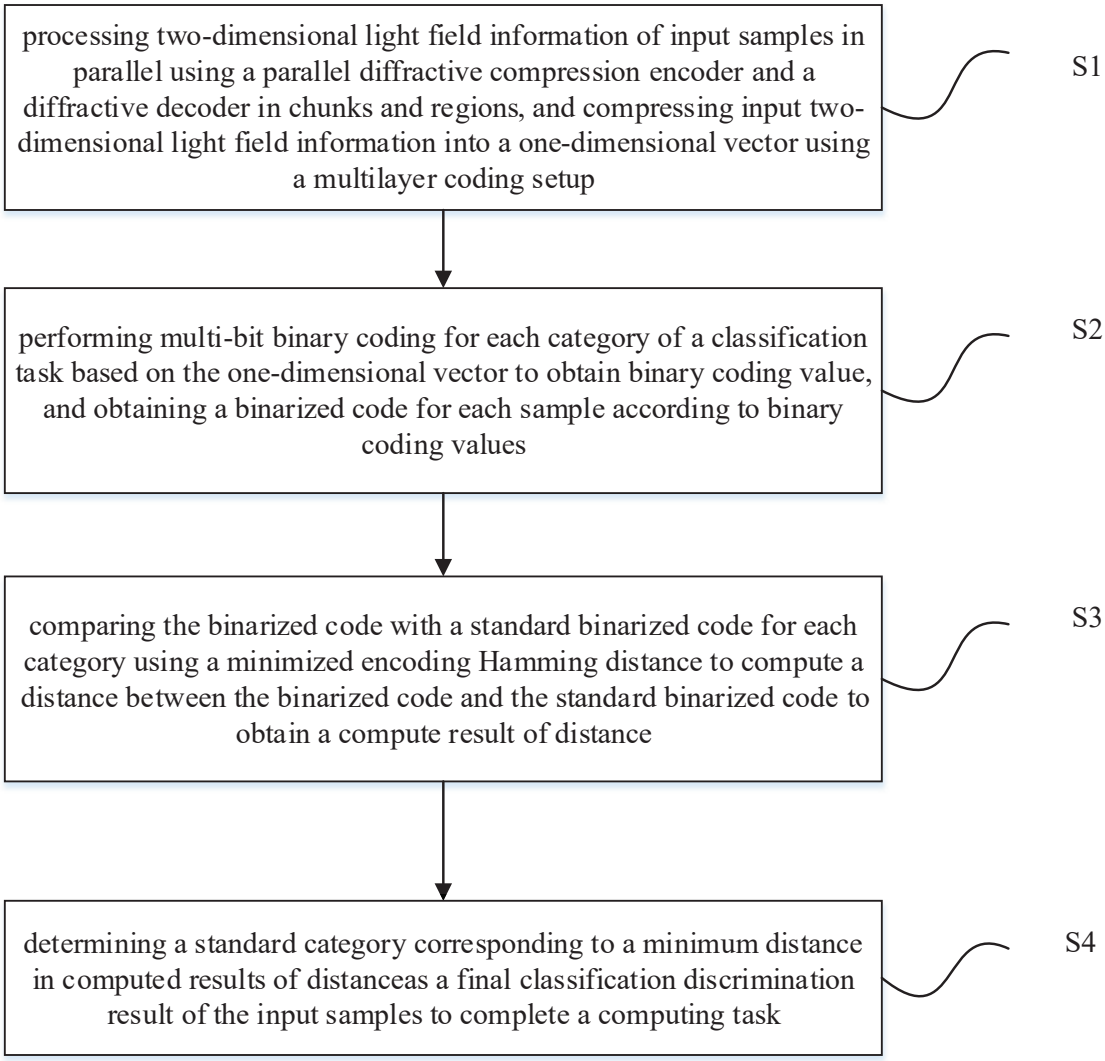

processing two-dimensional light field information of input samples in parallel using a parallel diffractive compression encoder and a diffractive decoder in chunks and regions, and compressing input two-dimensional light field information into a one-dimensional vector using a multilayer coding setup
S1
performing multi-bit binary coding for each category of a classification task based on the one-dimensional vector to obtain binary coding value, and obtaining a binarized code for each sample according to binary coding values
S2
comparing the binarized code with a standard binarized code for each category using a minimized encoding Hamming distance to compute a distance between the binarized code and the standard binarized code to obtain a compute result of distance
S3
determining a standard category corresponding to a minimum distance in computed results of distanceas a final classification discrimination result of the input samples to complete a computing task
S4

FIG. 4

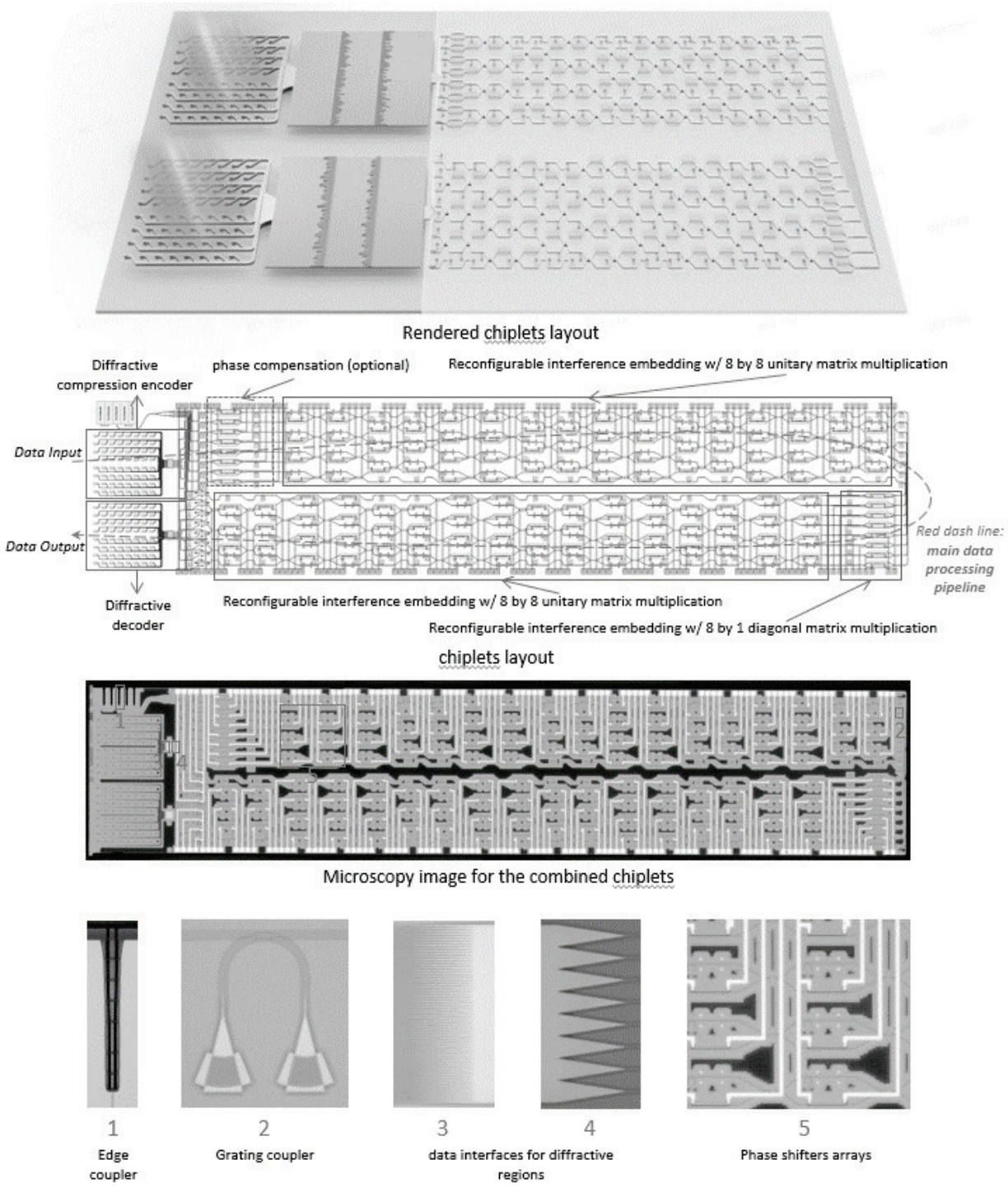

Rendered chiplets layout
Diffractive compression encoder
phase compensation (optional)
Reconfigurable interference embedding w/ 8 by 8 unitary matrix multiplication
Data Input
Data Output
Red dash line: main data processing pipeline
Diffractive decoder
Reconfigurable interference embedding w/ 8 by 8 unitary matrix multiplication
Reconfigurable interference embedding w/ 8 by 1 diagonal matrix multiplication
chiplets layout
Microscopy image for the combined chiplets
1
Edge coupler
2
Grating coupler
3
4
data interfaces for diffractive regions
5
Phase shifters arrays

FIG. 5

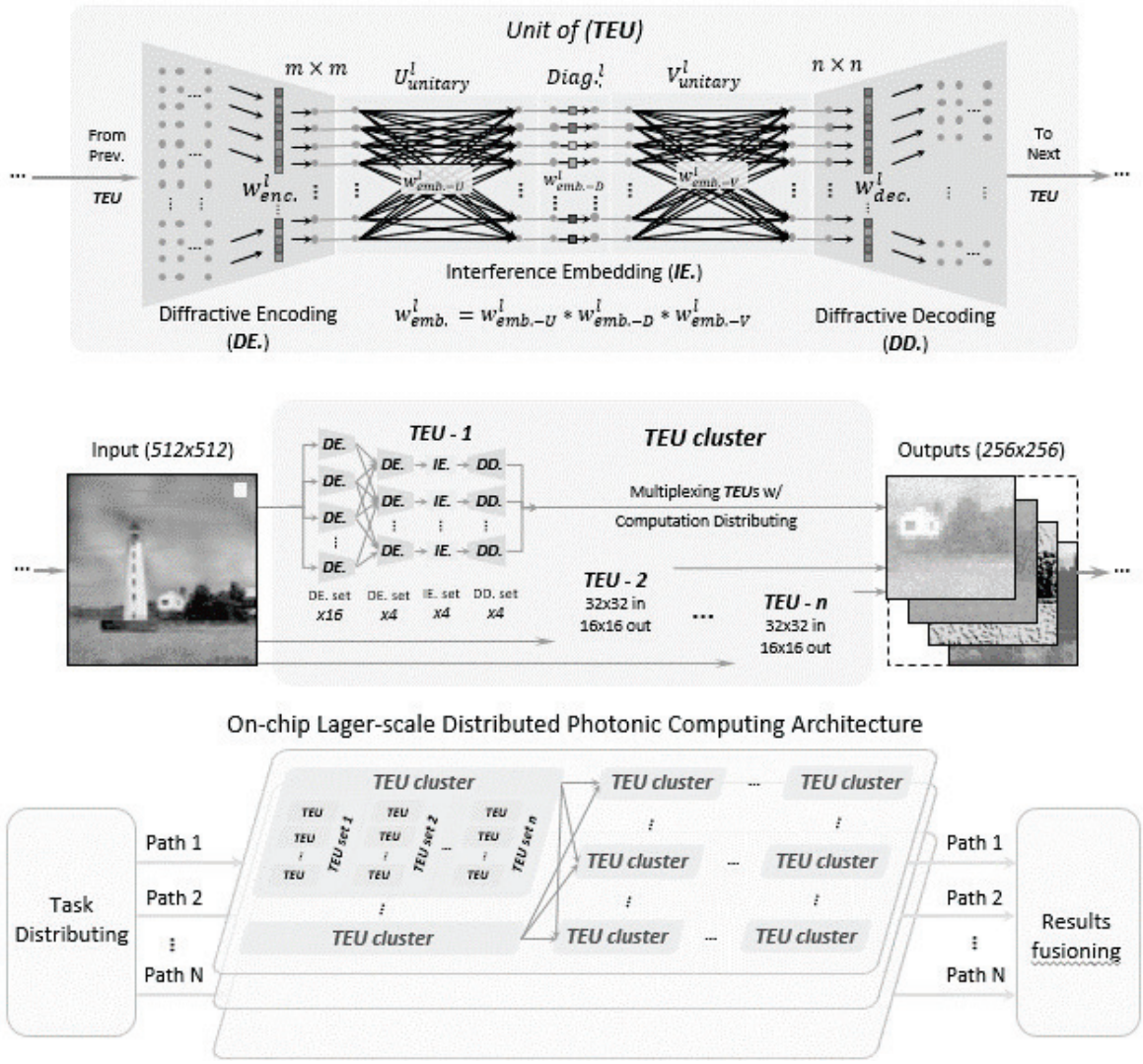

Unit of (TEU)
From Prev. TEU
To Next TEU
Interference Embedding (IE.)
Diffractive Encoding (DE.)
Diffractive Decoding (DD.)
Input (512x512)
TEU - 1
TEU cluster
Outputs (256x256)
Multiplexing TEUs w/
Computation Distributing
TEU - 2
32x32 in
16x16 out
TEU - n
32x32 in
16x16 out
DE. set x16
DE. set x4
IE. set x4
DD. set x4
On-chip Lager-scale Distributed Photonic Computing Architecture
Task Distributing
Path 1
Path 2
Path N
Results fusioning

FIG. 6

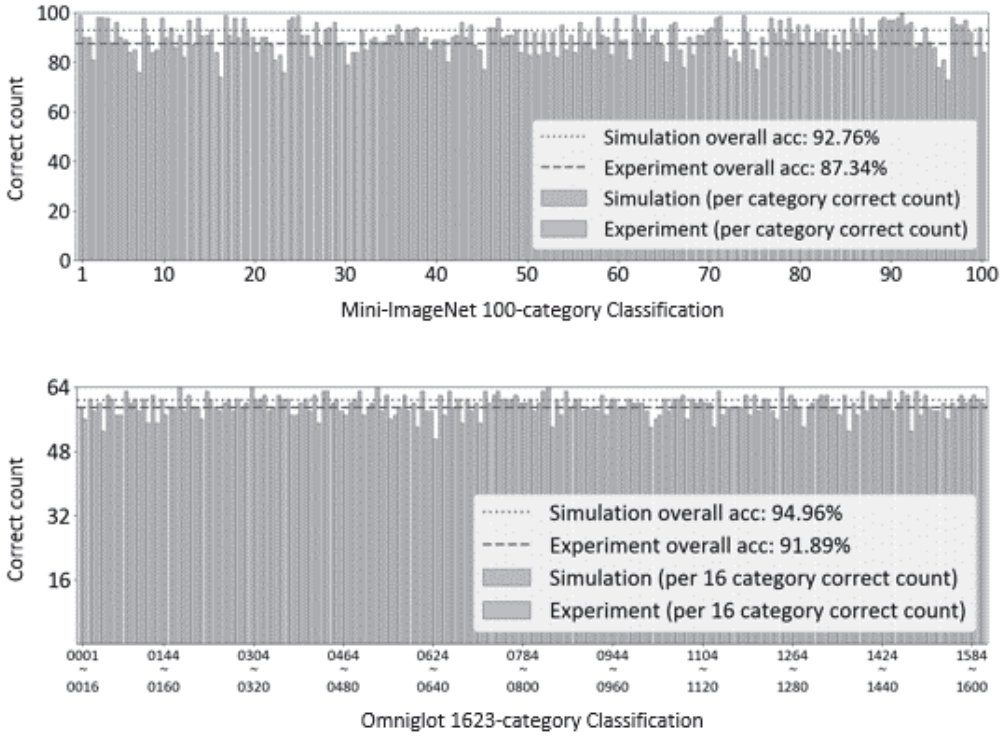

Correct count
100
80
60
40
20
0
1
10
20
30
40
50
60
70
80
90
100
Simulation overall acc: 92.76%
Experiment overall acc: 87.34%
Simulation (per category correct count)
Experiment (per category correct count)
Mini-ImageNet 100-category Classification
Correct count
64
48
32
16
Simulation overall acc: 94.96%
Experiment overall acc: 91.89%
Simulation (per 16 category correct count)
Experiment (per 16 category correct count)
0001 ~ 0016
0144 ~ 0160
0304 ~ 0320
0464 ~ 0480
0624 ~ 0640
0784 ~ 0800
0944 ~ 0960
1104 ~ 1120
1264 ~ 1280
1424 ~ 1440
1584 ~ 1600
Omniglot 1623-category Classification

FIG. 7