

SEMICONDUCTOR PACKAGE

TECHNICAL FIELD

[0001] The inventive concept relates to a semiconductor package. More particularly, the inventive concept relates to a semiconductor package including a stiffener.

BACKGROUND

[0002] Semiconductor packages are implemented from semiconductor chips in a form suitable for use in electronic products. In general, in semiconductor packages, semiconductor chips are mounted on a printed circuit board and electrically connected to the printed circuit board by using bonding wires or bumps. Recently, as semiconductor packages have become more high-performance, semiconductor packages have become large in size. In such large-sized semiconductor packages, a semiconductor package including a stiffener is used to control warpage occurred due to differences in thermal expansion coefficients of individual components constituting the semiconductor package.

SUMMARY

[0003] The inventive concept provides a semiconductor package with improved mechanical stability.

[0004] The technical problems to be solved by the inventive concept are not limited to the problems mentioned above, and other problems not mentioned will be clearly understood by those skilled in the art from the description below.

[0005] According to an aspect of the inventive concept, there is provided a semiconductor package.

[0006] According to another aspect of the inventive concept, there is provided a semiconductor package including a first redistribution structure, a second redistribution structure disposed on the first redistribution structure, a plurality of semiconductor chips disposed on an upper surface of the second redistribution structure, a bridge chip disposed on a lower surface of the second redistribution structure, a passive device spaced apart from the bridge chip in a horizontal direction and disposed on the lower surface of the second redistribution structure, a molding layer disposed between the first redistribution structure and the second redistribution structure and surrounding the bridge chip and the passive device, a plurality of conductive posts spaced apart from the bridge

chip and the passive device in the horizontal direction within the molding layer, a heat sink disposed at a vertical level higher than an upper surface of each of the plurality of semiconductor chips, and a stiffener disposed on the upper surface of the second redistribution structure and including a plurality of openings, wherein the plurality of semiconductor chips are disposed in the plurality of openings of the stiffener.

[0007] The semiconductor package includes a first redistribution structure, a second redistribution structure disposed on the first redistribution structure, a plurality of semiconductor chips disposed on an upper surface of the second redistribution structure, a bridge chip disposed on a lower surface of the second redistribution structure, a molding layer disposed between the first redistribution structure and the second redistribution structure and surrounding the bridge chip, and a stiffener disposed on the upper surface of the second redistribution structure and including a plurality of openings, wherein the plurality of semiconductor chips are disposed in the plurality of openings of the stiffener.

[0008] According to another aspect of the inventive concept, there is provided a semiconductor package including a first redistribution structure including a passivation layer, an under bump metallurgy (UBM) layer covering a part of a lower surface of the passivation layer, and a conductive layer in contact with the UBM layer and exposed to an upper surface of the passivation layer, a second redistribution structure disposed on the first redistribution structure, and including one or more redistribution insulating layers, a plurality of conductive line patterns disposed in the one or more redistribution insulating layers and extending in a horizontal direction, and a plurality of conductive vias disposed in the one or more redistribution insulating layers and extending in a vertical direction perpendicular to the horizontal direction, a plurality of semiconductor chips disposed on an upper surface of the second redistribution structure, a bridge chip disposed on a lower surface of the second redistribution structure and providing an electrical connection path between at least two semiconductor chips among the plurality of semiconductor chips, a passive device spaced apart from the bridge chip in the horizontal direction and disposed on the lower surface of the second redistribution structure, a molding layer disposed between the first redistribution structure and the second redistribution structure and surrounding side surfaces of the bridge chip and the passive device, a plurality of conductive posts spaced apart from the bridge chip and the passive device in the horizontal direction within the molding layer, and a stiffener disposed on the upper surface of the second redistribution structure and including a plurality of

openings, wherein the plurality of semiconductor chips are disposed in the plurality of openings of the stiffener.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0010] FIG. 1A is a horizontal cross-sectional view briefly illustrating the shape of a stiffener according to an embodiment;

[0011] FIGS. 1B and 1C are simplified vertical cross-sectional views taken along line A - A' in FIG. 1A;

[0012] FIG. 2A is a horizontal cross-sectional view briefly illustrating the shape of a stiffener according to an embodiment;

[0013] FIG. 2B is a simplified vertical cross-sectional view taken along line B - B' in FIG. 2A;

[0014] FIG. 3A is a plan view illustrating a semiconductor package according to an embodiment, and FIG. 3B is a cross-sectional view taken along line C - C' of FIG. 3A;

[0015] FIG. 4 is a cross-sectional view illustrating a semiconductor package according to an embodiment;

[0016] FIG. 5 is a cross-sectional view illustrating a semiconductor package according to an embodiment;

[0017] FIG. 6 is a cross-sectional view illustrating a semiconductor package according to an embodiment;

[0018] FIG. 7 is a cross-sectional view illustrating a semiconductor package according to an embodiment;

[0019] FIG. 8 is a cross-sectional view illustrating a semiconductor package according to an embodiment; and

[0020] FIGS. 9A, 9B, 9C, 9D, 9E, 9F, 9G and 9H are cross-sectional views illustrating a method of manufacturing a semiconductor package according to an embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0021] Hereinafter, embodiments of the inventive concept will be described in detail with reference to the attached drawings. The same reference numerals are used for the same components in the drawings, and redundant descriptions thereof are omitted.

[0022] Because embodiments of the inventive concept may be variously modified and changed and may be implemented in various different ways, particular embodiments will be illustrated in the accompanying drawings and described in detail in the following detailed description. However, it is not intended to limit the scope of the inventive concept to the particular embodiments, and all changes, modifications, equivalents, and replacements made without departing from the spirit and scope of the inventive concept should be construed as falling within the scope of the inventive concept. In describing embodiments, when it is determined that specific descriptions of relevant techniques known in the art may make the subject matter of the inventive concept ambiguous, detailed descriptions thereof are omitted.

[0023] FIG. 1A is a horizontal cross-sectional view briefly illustrating the shape of a stiffener 70 according to an embodiment. FIGS. 1B and 1C are simplified vertical cross-sectional views taken along line A - A' in FIG. 1A. FIG. 2A is a horizontal cross-sectional view briefly illustrating the shape of a stiffener 70' according to an embodiment. FIG. 2B is a simplified vertical cross-sectional view taken along line B - B' in FIG. 2A.

[0024] Referring to FIGS. 1A to 1C, the stiffener 70 may have a ring shape including a plurality of openings each having a quadrangular horizontal cross-section. The stiffener 70 may include a mold material. The mold material may include, for example, thermoset, thermoplastic, UV-curable resin, or a combination thereof. The mold material may include, for example, epoxy resin, silicone resin, or a combination thereof. The mold material may include, for example, an epoxy mold compound (EMC). Referring to FIG. 1B, the stiffener 70 may be formed on a first redistribution structure 100 without an adhesive layer. Referring to FIG. 1C, the stiffener 70 may be attached to the first redistribution structure 100 by using an adhesive layer 72.

[0025] Referring to FIGS. 2A to 2B, the stiffener 70' may include a metal material. The stiffener 70' may be pre-manufactured by a method such as die casting, injection, or forging, and then attached to the first redistribution structure 100 by using the adhesive layer 72. As will be described below, one or more semiconductor chips may be disposed in the openings of the stiffeners 70 and 70'.

[0026] FIG. 3A is a plan view illustrating a semiconductor package 1 according to an embodiment, and FIG. 3B is a cross-sectional view taken along line C - C' of FIG. 3A. For convenience of explanation, FIG. 3A shows only a first semiconductor chip 10, a second semiconductor chip 20, a bridge chip 40, the first redistribution structure 100, and the stiffener 70.

[0027] Referring to FIGS. 3A and 3B, the semiconductor package 1 may include the first semiconductor chip 10, the second semiconductor chip 20, a first device 30, the bridge chip 40, the first redistribution structure 100, a molding layer 200, a second redistribution structure 300, and the stiffener 70.

[0028] In the specification, a direction parallel to a main surface of the first redistribution structure 100 may be referred to as a horizontal direction (X direction and/or Y direction), and a direction perpendicular to the horizontal direction (X direction and/or Y direction) may be referred to as a vertical direction (Z direction).

[0029] In addition, among two surfaces spaced apart in the vertical direction (Z direction), the surface further away from an external connection terminal 170 may be referred to as an upper surface of a component, and the surface opposite to the upper surface may be referred to as a lower surface of the component.

[0030] The first redistribution structure 100 may include a passivation layer 110, an under bump metallurgy (UBM) layer 150, and a conductive layer 160. For example, the passivation layer 110 may have a single-layer structure. In another embodiment, the passivation layer 110 may have a multi-layer structure.

[0031] The passivation layer 110 may completely cover lower and side surfaces of the conductive layer 160 and expose an upper surface of the conductive layer 160. In addition, a part of the lower surface of the passivation layer 110 may be covered by the UBM layer 150. The passivation layer 110 may include, for example, silicon oxide, silicon nitride, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), fluorosilicate glass (FSG), or an insulating material including a combination thereof.

[0032] The UBM layer 150 may include a UBM pad disposed on the lower surface of the passivation layer 110 and a UBM via vertically penetrating at least a part of the passivation layer 110 and electrically connecting the UBM pad and the conductive layer 160. The UBM via may have a truncated cone cup shape with a partially empty center space, but, may also have a truncated cone shape with a filled center space according to an embodiment. The UBM pad may have a ring

shape with an empty center space, but may have a coin shape with a filled center space according to an embodiment. The UBM layer 150 may electrically connect different components of the semiconductor package 1, such as the conductive layer 160 and the external connection terminal 170, which will be described below. In addition, the UBM layer 150 may suppress the occurrence of cracks in the external connection terminal 170 due to thermal shock between the external connection terminal 170 and the first redistribution structure 100, thereby improving the reliability of the semiconductor package 1. The UBM layer 150 may include, for example, copper (Cu), aluminum (Al), silver (Ag), gold (Au), tungsten (W), titanium (Ti), or a conductive material including a combination thereof.

[0033] The conductive layer 160 may be disposed within the passivation layer 110, and an upper surface of the conductive layer 160 may be exposed to the upper surface of the passivation layer 110. The conductive layers 160 may be respectively disposed below a plurality of conductive posts 210, and upper surfaces of the conductive layer 160 may be bonded to lower surfaces of the plurality of conductive posts 210. The conductive layers 160 may be conductive patterns spaced apart in the first horizontal direction (X direction) or the second horizontal direction (Y direction). At this time, in FIG. 3B, the conductive layers 160 are patterns disposed at one vertical level, but, may be conductive patterns having a multi-layer structure disposed at different vertical levels within the passivation layer 110 according to an embodiment. The conductive layers 160 may electrically connect different components to each other, such as the plurality of conductive posts 210 and the UBM layers 150. The conductive layer 160 may be, for example, metal such as copper (Cu), aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), indium (In), molybdenum (Mo), manganese (Mn), cobalt (Co), tin (Sn), nickel (Ni), magnesium (Mg), rhenium (Re), beryllium (Be), gallium (Ga), ruthenium (Ru), or an alloy thereof, but is not limited thereto.

[0034] The semiconductor package 1 may further include the external connection terminal 170 disposed on the lower surface of the passivation layer 110. The external connection terminal 170 may be configured to electrically and physically connect the first redistribution structure 100 to an external device. Meanwhile, the external connection terminal 170 may have a structure of, for example, a solder ball or a conductive bump. The external connection terminal 170 may be electrically connected to the UBM layer 150 of the first redistribution structure 100 and electrically connected to an external device such as a module substrate or system board.

[0035] As shown in FIG. 3B, the external connection terminals 170 are not directly contacted and bonded to the plurality of conductive posts 210 surrounding the bridge chip 40, but the first redistribution structure 100 may be formed between the plurality of conductive posts 210 and the external connection terminals 170. When the first redistribution structure 100 is formed between the plurality of conductive posts 210 and the external connection terminals 170, the scale of a line width of the conductive layer 160 is less than the scale of the external connection terminal 170, and thus, a finer manufacturing process is possible. In addition, when the first redistribution structure 100 is formed between the plurality of conductive posts 210 and the external connection terminals 170, more external connection terminals 170 may be disposed than when the external connection terminals 170 are directly contacted and bonded to the plurality of conductive posts 210. When the semiconductor package 1 includes more external connection terminals 170, the semiconductor package 1 may receive power supply more stably.

[0036] A molding layer 200 and a plurality of conductive posts 210 may be disposed on the first redistribution structure 100. The molding layer 200 may cover the first device 30, the bridge chip 40, and the plurality of conductive posts 210 on the first redistribution structure 100. The molding layer 200 may completely seal the first device 30 and the bridge chip 40 between the first redistribution structure 100 and the second redistribution structure 300. The molding layer 200 may cover the side surfaces of the plurality of conductive posts 210 between the first redistribution structure 100 and the second redistribution structure 300.

[0037] The molding layer 200 may include, for example, a thermosetting resin, a thermoplastic resin, a UV-curable resin, or a combination thereof. The molding layer 200 may include, for example, epoxy resin, silicone resin, or a combination thereof. The molding layer 200 may include, for example, an EMC.

[0038] The plurality of conductive posts 210 may be disposed between the first redistribution structure 100 and the second redistribution structure 300 inside the molding layer 200. The plurality of conductive posts 210 may each provide an electrical connection path between the first redistribution structure 100 and the second redistribution structure 300. The plurality of conductive posts 210 may include, for example, copper (Cu), aluminum (Al), silver (Ag), gold (Au), tungsten (W), titanium (Ti), or a conductive material including a combination thereof.

[0039] The plurality of conductive posts 210 may have upper and lower surfaces spaced apart from each other in the vertical direction (Z direction). The upper surfaces of the plurality of conductive

posts 210 may be coplanar with an upper surface of the molding layer 200, and the lower surfaces of the plurality of conductive posts 210 may be coplanar with a lower surface of the molding layer 200. The plurality of conductive posts 210 may directly contact the conductive layer 160 exposed on the upper surface of the passivation layer 110. Specifically, the lower surfaces of the plurality of conductive posts 210 may be bonded to the upper surfaces of the conductive layers 160.

[0040] The plurality of conductive posts 210 may each have a single cylindrical shape. At this time, a diameter of each of the plurality of conductive posts 210 may be maintained constant in the vertical direction (Z direction). In another embodiment, the plurality of conductive posts 210 may each have a tapered shape with a diameter varying in the vertical direction (Z direction).

[0041] The second redistribution structure 300 may be disposed on the molding layer 200. The second redistribution structure 300 may include one or more redistribution insulating layers 310, a plurality of conductive line patterns 320, and a plurality of conductive vias 330.

[0042] The one or more redistribution insulating layers 310 may be stacked in the vertical direction (Z direction). The redistribution insulating layer 310 may include an insulating material, for example, a photo-imageable dielectric (PID) resin, and may further include photosensitive polyimide and/or an inorganic filler.

[0043] A conductive pattern including the plurality of conductive line patterns 320 and the plurality of conductive vias 330 may be disposed on at least one of upper and lower surfaces of the redistribution insulating layer 310. The plurality of conductive line patterns 320 may be disposed to extend in the horizontal direction (X direction and/or Y direction) inside the redistribution insulating layer 310. The plurality of conductive vias 330 may penetrate at least one redistribution insulating layer 310 in the vertical direction (Z direction) and may be respectively in contact with and electrically connected to some of the plurality of conductive line patterns 320.

[0044] In some embodiments, at least some of the plurality of conductive line patterns 320 may be integrally formed with some of the plurality of conductive vias 330. For example, the plurality of conductive line patterns 320 may be integrally formed with the plurality of conductive vias 330 in contact with the upper surfaces of the plurality of conductive line patterns 320.

[0045] In some embodiments, the plurality of conductive vias 330 may each have a tapered shape extending from the top to the bottom with a narrow horizontal width. That is, the plurality of conductive vias 330 may each have a narrower horizontal width further away from the first semiconductor chip 10.

[0046] A plurality of redistribution patterns including the plurality of conductive line patterns 320 and the plurality of conductive vias 330 may each include, for example, metal such as copper (Cu), aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), indium (In), molybdenum (Mo), manganese (Mn), cobalt (Co), tin (Sn), nickel (Ni), magnesium (Mg), rhenium (Re), beryllium (Be), gallium (Ga), ruthenium (Ru), or an alloy thereof, but is not limited thereto.

[0047] The first semiconductor chip 10, the second semiconductor chip 20, and the stiffener 70 may be disposed on an upper surface of the second redistribution structure 300, and the third device 30, the bridge chip 40, the first molding layer 200, and the conductive post 210 may be disposed on a lower surface of the second redistribution structure 300. The first semiconductor chip 10 and the second semiconductor chip 20 may be spaced apart in the horizontal direction (X direction and/or Y direction) on the second redistribution structure 300. In addition, the first device 30 and the bridge chip 40 may be spaced apart in the horizontal direction (X direction and/or Y direction) on the second redistribution structure 300.

[0048] The first semiconductor chip 10 may include a first substrate 12 and a first chip pad 14, and the second semiconductor chip 20 may include a second substrate 22 and a second chip pad 24. Each of the first and second substrates 12 and 22 may include an active surface and an inactive surface that are opposite to each other. The active surface may be disposed adjacent to a lower surface of each of the first and second substrates 12 and 22, and the inactive surface may be disposed adjacent to an upper surface thereof.

[0049] In some embodiments, at least one of the first semiconductor chip 10 and the second semiconductor chip 20 may be a memory chip or a logic chip. The memory chip may be, for example, a volatile memory chip such as dynamic random access memory (DRAM) or static random access memory (SRAM), or may be a non-volatile memory chip such as phase-change random access memory (PRAM), magnetoresistive random access memory (MRAM), ferroelectric random access memory (FeRAM), or resistive random access memory (RRAM). In addition, the logic chip may be, for example, a microprocessor, an analog element, or a digital signal processor.

[0050] The first and second substrates 12 and 22 may each include an integrated circuit. The integrated circuit may be a memory circuit, a logic circuit, or any type of integrated circuit including a combination thereof. The memory circuit may include, for example, a dynamic random access memory (DRAM) circuit, a static random access memory (SRAM) circuit, a flash memory

circuit, an electrically erasable and programmable read-only memory (EEPROM) circuit, a phase-change random access memory (PRAM) circuit, a magnetic random access memory (MRAM) circuit, a resistive random access memory (RRAM) circuit, or a combination thereof. The logic circuit may include, for example, a central processing unit (CPU) circuit, a graphics processing unit (GPU) circuit, a controller circuit, an application specific integrated circuit (ASIC) circuit, an application processor (AP) circuit, or a combination thereof.

[0051] In addition, the first and second substrates 12 and 22 may each include a semiconductor material, such as a Group IV semiconductor material, a Group III-V semiconductor material, a Group II-VI semiconductor material, or a combination thereof. The Group IV semiconductor material may include, for example, silicon (Si), germanium (Ge), or a combination thereof. The III-V semiconductor material may include, for example, gallium arsenide (GaAs), indium phosphorus (InP), gallium phosphorus (GaP), indium arsenide (InAs), indium antimony (InSb), indium gallium arsenide (InGaAs), or a combination thereof. The group II-VI semiconductor material may include, for example, zinc telluride (ZnTe), cadmium sulfide (CdS), or a combination thereof.

[0052] The first and second chip pads 14 and 24 may be respectively disposed on the lower surfaces of the first and second substrates 12 and 22, and may extend along the lower surfaces of each of the first and second substrates 12 and 22 which is the active surfaces. In addition, a first connection member 16 may be disposed between the first semiconductor chip 10 and the second redistribution structure 300, and a second connection member 26 may be disposed between the second semiconductor chip 20 and the second redistribution structure 300.

[0053] The first chip pad 14 may be in contact with the first connection member 16, and the second chip pad 24 may be in contact with the second connection member 26. Each of the first and second connection members 16 and 26 may contact the conductive line pattern 320 and/or the conductive via 330 of the second redistribution structure 300. Accordingly, the first connection member 16 may provide an electrical connection path between the first semiconductor chip 10 and the second redistribution structure 300, and the second connection member 26 may provide an electrical connection path between the second semiconductor chip 20 and the second redistribution structure 300.

[0054] The first and second chip pads 14 and 24 may include, for example, copper (Cu), aluminum (Al), silver (Ag), gold (Au), tungsten (W), titanium (Ti), or a conductive material including a

combination thereof. In addition, the first and second connection members 16 and 26 may each include, for example, a solder ball.

[0055] The stiffener 70 may have a quadrangular ring shape surrounding the first semiconductor chip 10 and the second semiconductor chip 20 when viewed from the upper surface of the semiconductor package 1. An upper surface of the stiffener 70 may be disposed at a lower vertical level than the upper surfaces of the first and second semiconductor chips 10 and 20. That is, with respect to the upper surface of the second redistribution structure 300, a height H1 of the upper surface of the stiffener 70 may be less than a height H2 of each of the upper surfaces of the first semiconductor chip 10 and the second semiconductor chip 20. As a result, heat may be effectively dissipated from the first semiconductor chip 10 and the second semiconductor chip 20.

[0056] The first device 30 may be disposed on the lower surface of the second redistribution structure 300. The first device 30 may include various types of passive components or various forms of surface mountable components. For example, the first device 30 may be referred to as a passive device. For example, a passive component may include one or more selected from a resistor, a capacitor, an inductor, a thermistor, an oscillator, a ferrite bead, an antenna, a varistor, and a crystal. For example, the passive component may include a Multi Layer Ceramic Capacitor (MLCC), Low Inductance Chip Capacitor (LICC), Land Side Capacitor (LSC), Integrated Passive Device (IPD), etc.

[0057] A third connection member 32 may be disposed between the first device 30 and the second redistribution structure 300. The first device 30 may be electrically connected to the second redistribution structure 300 through the third connection member 32. For example, the third connection member 32 may be a solder ball.

[0058] The bridge chip 40 may also be disposed on the lower surface of the second redistribution structure 300. The bridge chip 40 may provide an electrical connection path between the first semiconductor chip 10 and the second semiconductor chip 20 on the second redistribution structure 300. Specifically, the first semiconductor chip 10 and the second semiconductor chip 20 may be electrically connected to each other through a bridge circuit within the bridge chip 40. As shown in FIG. 3A, each of the first and second semiconductor chips 10 and 20 may overlap at least a part of the bridge chip 40 in the vertical direction (Z direction).

[0059] The bridge chip 40 may include a bridge substrate 42 and a bridge circuit. The bridge chip 40 is not directly electrically connected to the first redistribution structure 100, but may be

electrically connected to the first redistribution structure 100 through the conductive post 210 and the second redistribution structure 300.

[0060] An active surface of the bridge substrate 42 may be disposed adjacent to an upper surface of the bridge substrate 42, and an inactive surface of the bridge substrate 42 may be disposed adjacent to a lower surface of the bridge substrate 42. The bridge substrate 42 may include a semiconductor material, such as a Group IV semiconductor material, a Group III-V semiconductor material, a Group II-VI semiconductor material, or a combination thereof. The Group IV semiconductor material may include, for example, silicon (Si), germanium (Ge), or a combination thereof. The III-V semiconductor material may include, for example, gallium arsenide (GaAs), indium phosphorus (InP), gallium phosphorus (GaP), indium arsenide (InAs), indium antimony (InSb), indium gallium arsenide (InGaAs), or a combination thereof. The group II-VI semiconductor material may include, for example, zinc telluride (ZnTe), cadmium sulfide (CdS), or a combination thereof. In addition, the bridge substrate 42 may include not only a semiconductor material but also glass or ceramic.

[0061] The bridge circuit may be formed within the bridge substrate 42. The bridge circuit may have a pitch corresponding to a fine pitch of a chip pad of each of the first and second semiconductor chips 10 and 20. The bridge circuit may have a finer pitch than the conductive layer 160. For example, a line width of the bridge circuit may be less than a line width of the conductive layer 160.

[0062] A fourth connection member 44 may be disposed between the bridge chip 40 and the second redistribution structure 300. The fourth connection member 44 may electrically connect the second redistribution structure 300 to the bridge chip 40. The fourth connection member 44 may contact the conductive line pattern 320 and/or the conductive via 330 of the second redistribution structure 300. For example, the fourth connection member 44 may include a conductive pillar. For example, the fourth connection member 44 may have a single cylindrical shape. At this time, a diameter of the fourth connection member 44 may be maintained constant in the vertical direction (Z direction). In another embodiment, the fourth connection member 44 may have a tapered shape with a diameter varying in the vertical direction (Z direction). For example, the fourth connection member 44 may include copper (Cu), aluminum (Al), silver (Ag), gold (Au), tungsten (W), titanium (Ti), or a conductive material including a combination thereof.

[0063] In another embodiment, each of the first device 30 and/or the bridge chip 40 may include a chip pad. When the first device 30 includes a chip pad, a first device chip pad may contact the third connection member 32. In addition, when the bridge chip 40 includes a chip pad, a bridge chip pad may contact the fourth connection member 44.

[0064] The semiconductor package 1 may further include an underfill layer 50 surrounding the third connection member 32 and the fourth connection member 44. The underfill layer 50 may fill between the first device 30 and the second redistribution structure 300 and between the bridge chip 40 and the second redistribution structure 300. The underfill layer 50 may include an outer surface having an inclination. The underfill layer 50 may include epoxy resin or two or more types of silicone hybrid materials. Accordingly, the third connection member 32 and the fourth connection member 44 may contact the underfill layer 50. However, the inventive concept is not limited thereto, and the underfill layer 50 may be omitted.

[0065] The first device 30 and the bridge chip 40 may be located at a vertical level higher than the lower surface of the first redistribution structure 100. In addition, the first device 30 and the bridge chip 40 may be arranged to be spaced apart from the upper surface of the first redistribution structure 100 in the vertical direction (Z direction). That is, the first device 30 and the bridge chip 40 may be spaced apart from the first redistribution structure 100. That is, the molding layer 200 may be disposed between the first device 30 and the first redistribution structure 100 and between the bridge chip 40 and the first redistribution structure 100.

[0066] In addition, inside the molding layer 200, the first device 30 may have a third height H3, and the bridge chip 40 may have a fourth height H4. The third height H3 and the fourth height H4 may be different from each other. In another embodiment, the third height H3 and the fourth height H4 may be equal to each other.

[0067] The semiconductor package 1 according to the inventive concept may first form the stiffener 70 including a plurality of openings each having a quadrangular cross-section, thereby securing mechanical stability without a wafer supporting system (WSS) process.

[0068] FIG. 4 is a cross-sectional view illustrating a semiconductor package 2 according to an embodiment. The semiconductor package 2 of FIG. 4 is described with reference to FIGS. 3A and 3B together.

[0069] Referring to FIG. 4, the semiconductor package 2 may include the first semiconductor chip 10, the second semiconductor chip 20, the first device 30, the bridge chip 40, a second device 60,

the redistribution structure 100, the molding layer 200, the second redistribution structure 300, and the stiffener 70. The first semiconductor chip 10, the second semiconductor chip 20, the first device 30, the bridge chip 40, the redistribution structure 100, the molding layer 200, the second redistribution structure 300, and the stiffener 70 of the semiconductor package 2 of FIG. 4 are substantially the same as first semiconductor chip 10, the second semiconductor chip 20, the first device 30, the bridge chip 40, the redistribution structure 100, the molding layer 200, the second redistribution structure 300, and the stiffener 70 of the semiconductor package 1 of FIG. 3B, respectively, and thus, the second device 60 is mainly described.

[0070] The second device 60 may be disposed on a lower surface of the second redistribution structure 300. The second device 60 may be spaced apart from each of the first device 30 and the bridge chip 40 in the horizontal direction (X direction and/or Y direction). Each of the first device 30, bridge chip 40, and second device 60 may be surrounded by the molding layer 200.

[0071] For example, the second device 60 may include a chiplet. The chiplet may include a plurality of IP blocks, and the plurality of IP blocks may perform different functions. Each of the plurality of IP blocks may include a plurality of integrated circuits. In another embodiment, the second device 60 may be an active device. In another embodiment, the second device 60 may be a semiconductor chip. For example, the second device 60 may be an input/output chip (I/O chip) or a power management chip. The power management chip may include a power management integrated circuit (PMIC).

[0072] The second device 60 may be spaced apart from the first redistribution structure 100 in the vertical direction (Z direction). That is, the molding layer 200 may be disposed between the second device 60 and the first redistribution structure 100.

[0073] In addition, the second device 60 may have a fifth height H5 from a lower surface of the second redistribution structure 300 to a lower surface of the second device 60. The third to fifth heights H3, H4, and H5 may be different from each other. In another embodiment, at least two of the third to fifth heights H3, H4, and H5 may be the same.

[0074] A fifth connection member 62 may be disposed between the second device 60 and the second redistribution structure 300. The second device 60 may be electrically connected to the second redistribution structure 300 through the fifth connection member 62. The fifth connection member 62 may contact the conductive line pattern 320 and/or the conductive via 330 of the second

redistribution structure 300. The plurality of fifth connection members 62 may also be surrounded by the underfill layer 50.

[0075] In another embodiment, the second device 60 may include a chip pad. When the second device 60 includes a second device chip pad, the second device chip pad may contact the fifth connection member 62.

[0076] In addition, although not additionally shown in the drawings of the specification, the fourth connection member 44 of each of the semiconductor packages 1 and 2 may include a solder ball, and the third connection member 32 may include a conductive pillar. The conductive pillar may have a single cylindrical shape. At this time, a diameter of the conductive pillar may be maintained constant in the vertical direction (Z direction). In another embodiment, the conductive pillar may have a tapered shape with a diameter varying in the vertical direction (Z direction). For example, the third and fourth connection members 32 and 44 may each include copper (Cu) or aluminum (Al), silver (Ag), gold (Au), tungsten (W), titanium (Ti), or a conductive material including a combination thereof. The third and fourth connection members 32 and 44 may be modified in various ways.

[0077] FIG. 5 is a cross-sectional view illustrating a semiconductor package 3 according to an embodiment. The semiconductor package 3 of FIG. 5 is described with reference to FIG. 4.

[0078] Referring to FIG. 5, the semiconductor package 3 may include the first semiconductor chip 10, the second semiconductor chip 20, the first device 30, the bridge chip 40, the second device 60, the redistribution structure 100, the molding layer 200, the second redistribution structure 300, and the stiffener 70. The first semiconductor chip 10, the second semiconductor chip 20, the first device 30, the bridge chip 40, the second device 60, the redistribution structure 100, the molding layer 200, the second redistribution structure 300, and the stiffener 70 of the semiconductor package 3 of FIG. 5 100 are substantially the same as the first semiconductor chip 10, the second semiconductor chip 20, the first device 30, the bridge chip 40, the second device 60, the redistribution structure 100, the molding layer 200, the second redistribution structure 300, and the stiffener 70 of FIG. 4, respectively, and thus, the conductive post 210 is mainly described.

[0079] The conductive post 210 may include a pillar portion 210a including copper (Cu) and a connection layer 210b that allows the pillar portion 210a to adhere to the first redistribution

structure 100. The connection layer 210b may include lead (Pb), but a material of the connection layer 210b is not limited thereto.

[0080] Referring to FIGS. 6 and 7 together, semiconductor packages 4 in FIG. 6 and 5 in FIG. 7 may respectively further include heat sinks 80 in FIG. 6 and 80b in FIG. 7.

[0081] Referring first to FIG. 6, the first and second semiconductor chips 10 and 20 may be attached to the heat sink 80 through an interface material layer 82. The interface material layer 82 may include a thermally conductive and electrically insulating material. For example, the interface material layer 82 may include a polymer including metal powder such as silver or copper, thermal grease, white grease, or a combination thereof. The heat sink 80 may directly contact the first and second semiconductor chips 10 and 20 through the interface material layer 82, thereby improving heat dissipation characteristics. In FIG. 6, an upper surface of the stiffener 70 is shown to be spaced apart from a bottom surface of the heat sink 80, but the arrangement of the stiffener 70 is not limited thereto, and the upper surface of the stiffener 70 may be formed in direct contact with the bottom surface of the heat sink 80. In addition, an interface material layer (not shown) may be disposed on the upper surface of the stiffener 70, and the stiffener 70 may contact the heat sink 80 through the interface material layer. In a plan view, the heat sink 80 may have a shape protruding into openings of the stiffener 70.

[0082] Next, referring to FIG. 7, the interface material layer 82 of FIG. 7 is the same as the interface material layer 82 of FIG. 6, and thus, a description thereof is omitted, and differences between the heat sink 80b and the heat sink 80 of FIG. 6 are mainly described.

[0083] The heat sink 80b may include a protrusion portion protruding downward from a part in contact with the first and second semiconductor chips 10 and 20 through the interface material layer 82. In FIG. 7, the upper surface of the stiffener 70 is shown to be spaced apart from a bottom surface of the heat sink 80b, but the arrangement of the stiffener 70 is not limited thereto, and the upper surface of the stiffener 70 may be formed in direct contact with the bottom surface of the heat sink 80b. In addition, an interface material layer (not shown) may be disposed on the upper surface of the stiffener 70, and the stiffener 70 may contact the heat sink 80b through the interface material layer. In a plan view, the heat sink 80b may have a shape protruding into openings of the stiffener 70.

[0084] FIG. 8 is a cross-sectional view illustrating a semiconductor package 6 according to an embodiment. For convenience of explanation, only the first semiconductor chip

10, the second semiconductor chip 20, the bridge chip 40, the first redistribution structure 100, and the stiffener 70 are shown in FIG. 8. The semiconductor package 6 of FIG. 8 is described with reference to FIGS. 3A and 3B together.

[0085] Referring to FIG. 8, the bridge chip 40 may be disposed on a lower surface of the second redistribution structure 300. The bridge chip 40 may provide an electrical connection path between the first semiconductor chip 10 and the second semiconductor chip 20 on the second redistribution structure 300. Specifically, the first semiconductor chip 10 and the second semiconductor chip 20 may be electrically connected to each other through a bridge circuit inside the bridge chip 40. As shown in FIG. 8, two first semiconductor chips 10 spaced apart in the horizontal direction (X direction and/or Y direction) and two second semiconductor chips 20 spaced apart in the horizontal direction (X direction and/or Y direction) may each overlap at least a part of the bridge chip 40 in the vertical direction (Z direction). The inventive concept is not limited thereto, and the first semiconductor chip 10, the second semiconductor chip 20, and the bridge chip 40 may be disposed in various ways. The bridge chip 40 may electrically connect a plurality of semiconductor chips to each other.

[0086] FIGS. 9A to 9H are cross-sectional views illustrating a method of manufacturing a semiconductor package according to an embodiment. The method of FIGS. 9A to 9H is described with reference to FIGS. 1A to 8.

[0087] Referring to FIG. 9A, the second redistribution structure 300 may be formed. The second redistribution structure 300 may include the one or more redistribution insulating layers 310, the conductive line pattern 320, and the conductive via 330.

[0088] The one or more redistribution insulating layers 310 may be stacked in the vertical direction (Z direction). The conductive line pattern 320 may extend in the horizontal direction (X direction and/or Y direction) inside the redistribution insulating layer 310. The conductive via 330 may extend in the vertical direction (Z direction) inside the redistribution insulating layer 310 and may be electrically connected to at least one conductive line pattern 320.

[0089] First, the lowermost bottom conductive line pattern 320 is formed and then, a preliminary lowermost redistribution insulating layer covering the lowermost bottom conductive line pattern 320 is formed. Thereafter, at least a part of the preliminary lowermost redistribution insulating layer may be removed by performing an exposure process, and the lowermost redistribution insulating layer 310 including a via hole may be formed. The via hole may be formed to have a

narrow horizontal width from an upper surface of the lowermost redistribution insulating layer 310 to a lower surface thereof. A base redistribution conductive layer may be formed and patterned on the lowermost redistribution insulating layer 310, and a base conductive pattern including the conductive line pattern 320 and the conductive via 330 may be formed. Thereafter, the second redistribution structure 300 may be formed by repeatedly forming the redistribution insulating layer 310 and conductive patterns.

[0090] Referring to FIG. 9B, the stiffener 70 may be formed. The stiffener 70 may include openings extending from an upper surface to a lower surface. As will be described below, a semiconductor chip may be disposed in the opening. Referring to FIGS. 1A to 1C and FIGS. 2A and 2B together, in some embodiments, the stiffener 70 may be fixed by being adhered through an adhesive layer (not shown).

[0091] Referring to FIG. 9C, the conductive post 210 may be formed. For example, the conductive post 210 may include copper (Cu), aluminum (Al), silver (Ag), gold (Au), tungsten (W), titanium (Ti), or a conductive material including a combination thereof. Referring to FIG. 6 together, the conductive post 210 may include the pillar portion 210a including copper (Cu) and the connection layer 210b that allows the pillar portion 210a to adhere to the first redistribution structure 100. At this time, the connection layer 210b may include lead (Pb), but a material of the connection layer 210b is not limited thereto.

[0092] Referring to FIG. 9D, the first device 30 and the bridge chip 40 may be attached to the second redistribution structure 300. Each of the first device 30, the bridge chip 40, and the conductive post 210 may be spaced apart from each other in the horizontal direction (X direction and/or Y direction).

[0093] The first device 30 may be attached by the third connection member 32, and the bridge chip 40 may be attached by the fourth connection member 44. The third connection member 32 and the fourth connection member 44 may be surrounded by the underfill layer 50, but the inventive concept is not limited thereto.

[0094] At this time, the first device 30 may be attached using a solder bonding method, and the bridge chip 40 may be attached using an oxide bonding method. Accordingly, the third connection member 32 may include a solder ball, and the fourth connection member 44 may include a conductive pillar. However, the bonding method of the first device 30 and/or the bridge chip 40 may be modified in various ways.

[0095] Referring to FIG. 9E, the molding layer 200 may be formed by forming a molding material surrounding the first device 30, the bridge chip 40, and the conductive post 210 and removing at least a part of the molding material.

[0096] A material of the molding material may be the same as a material of the molding layer 200 described with reference to FIG. 3B. After the molding material is formed, an upper portion of the molding material and an upper portion of the conductive post 210 may be removed by grinding. The molding layer 200 may be formed by grinding the molding material. When the molding layer 200 is completed, an upper surface of the molding layer 200 may be coplanar with an upper surface of the conductive post 210.

[0097] Referring to FIG. 9F, the first semiconductor chip 10 and the second semiconductor chip 20 may be disposed on the second redistribution structure 300. FIG. 7F may show an inverted form of the result of FIG. 7E. The first semiconductor chip 10 may include the first substrate 12 and the first chip pad 14, and the second semiconductor chip 20 may include the second substrate 22 and the second chip pad 24.

[0098] The first connection member 16 may be disposed between the first semiconductor chip 10 and the second redistribution structure 300, and the second connection member 26 may be disposed between the second semiconductor chip 20 and the second redistribution structure 300. The first connection member 16 and the second connection member 26 may be electrically connected to the conductive line pattern 320 and/or the conductive via 330.

[0099] Referring to FIG. 9G, the first redistribution structure 100 may be formed on the molding layer 200. The first redistribution structure 100 may include the passivation layer 110, the UBM layer 150, and the conductive layer 160. The passivation layer 110 may completely cover lower and side surfaces of the conductive layer 160 and expose an upper surface of the conductive layer 160. In addition, a part of a lower surface of the passivation layer 110 may be covered by the UBM layer 150.

[0100] To form the first redistribution structure 100, the conductive layer 160 may first be formed on the molding layer 200. The conductive layer 160 may be formed through a plating process. Thereafter, a seed layer may be additionally formed on the edge of the conductive layer 160 to prevent a metal material of the conductive layer 160 from diffusing into the passivation layer 110. After the conductive layer 160 is formed, a first operation of forming the passivation layer 110 covering the conductive layer 160 and including a via hole, a second operation of forming a UBM

via to fill the via hole, and a third operation of forming a UBM pad integrally formed with the UBM via and covering a part of the upper surface of the passivation layer 110 may be performed. The second and third operations of respectively forming the UBM via and UBM pad may include a plating process. In the first operation, the passivation layer 110 may be formed, for example, by lamination, application, chemical vapor deposition (CVD), physical vapor deposition (PVD), or a combination thereof.

[0101] Referring to FIG. 9H, the semiconductor package 1 may be completed by attaching the external connection terminal 170 to the UBM layer 150. The external connection terminal 170 may have, for example, a solder ball structure or a conductive bump structure.

[0102] While the inventive concept has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:
 - a first redistribution structure;
 - a second redistribution structure disposed on the first redistribution structure;
 - a plurality of semiconductor chips disposed on an upper surface of the second redistribution structure;
 - a bridge chip disposed on a lower surface of the second redistribution structure;
 - a molding layer disposed between the first redistribution structure and the second redistribution structure and surrounding the bridge chip; and
 - a stiffener disposed on the upper surface of the second redistribution structure and comprising a plurality of openings,wherein the plurality of semiconductor chips are disposed in the plurality of openings of the stiffener.
2. The semiconductor package of claim 1, wherein a horizontal cross-section of each of the plurality of openings of the stiffener is a quadrangular shape.
3. The semiconductor package of claim 1 or claim 2, wherein an upper surface of the stiffener is disposed at a lower vertical level than an upper surface of each of the plurality of semiconductor chips.
4. The semiconductor package of any one of claims 1 to 3, further comprising:
 - an adhesive layer disposed between a lower surface of the stiffener and the upper surface of the second redistribution structure.
5. The semiconductor package of any one of claims 1 to 4, wherein the plurality of semiconductor chips disposed in the plurality of openings of the stiffener are spaced apart from side walls of the plurality of openings of the stiffener by a constant interval.

6. The semiconductor package of claim 5, wherein the constant interval is in a range of about 2 mm to about 3 mm.

7. The semiconductor package of any one of claims 1 to 6, wherein the bridge chip is electrically connected to the first redistribution structure through the second redistribution structure, and in a plan view, overlaps in a vertical direction at least two semiconductor chips among the plurality of semiconductor chips.

8. The semiconductor package of any one of claims 1 to 7, further comprising: a plurality of conductive posts disposed inside the molding layer, and spaced apart from the bridge chip in a horizontal direction.

9. The semiconductor package of claim 8, wherein each of the plurality of conductive posts includes copper (Cu), and further includes a connection layer including lead (Pb) in a surface in contact with the first redistribution structure.

10. The semiconductor package of any one of claims 1 to 9, further comprising: a connection member disposed between the bridge chip and the second redistribution structure, wherein the connection member is in direct contact with the molding layer.