ABSTRACT

Provided herein is a memory device and a method of manufacturing the memory device. The memory device including a stacked body, a channel layer penetrating the stacked body, a tunnel isolation layer enclosing an outer side surface of the channel layer, a capping layer extending from the channel layer and protruding upward from the stacked body, a spacer enclosing an outer side surface of the capping layer on the stacked body, and a liner layer extending along a top surface of the stacked body and an outer side surface of the spacer. In an embodiment, the tunnel isolation layer having a first thickness, and the spacer may have a second thickness greater than the first thickness. In an embodiment, the spacer having a first height, and the liner layer having a second height lower than the first height.

FIG. 3