

[Title of Invention] SEMICONDUCTOR DEVICE, AND METHOD
FOR MANUFACTURING SAME

[Technical Field]

5 [0001]

Embodiments described herein relate generally to a semiconductor device and a method of manufacturing a semiconductor device.

10 [Background Art]

[0002]

There has been proposed a memory device with a three-dimensional structure in which a memory hole is formed in a stacked body in which multiple electrode layers are stacked
15 and a charge storage film and a semiconductor film are extended in a stacking direction of the stacked body in the memory hole. The memory device has multiple memory cells (MC) connected in series between a drain-side select transistor (STD) and a source-side select transistor (STS). The structure
20 where STD, MC, and STS are connected in series is called a "memory string (or a NAND string)". The electrode layer is gate electrodes (a drain-side selection gate SGD, a word line WL, and a source-side selection gate SGS) of the STD, the MC, and the STS. In the stacked body, multiple slits starting from an
25 upper surface of the stacked body and reaching the substrate are formed. A region between the slits is called a "block". The number of SGDs provided in one "block" is typically "one". In recent years, there has been proposed a memory device in which two SGDs are juxtaposed in one "block". When
30 operating the memory device, one of the two SGDs is "selected". A memory string including the selected SGD is electrically connected to a bit line BL. In such a memory device, there is a circumstance that a high-resistance electrode layer may be likely to occur. For example, when a high resistance electrode
35 layer occurs, the resistance of the electrode layer is changed for every memory string. Thus, for example, the resistance

difference of the word WL is increased between memory strings. It is desired to prevent an increase in resistance difference of the electrode layer.

5 [Citation List]

[Patent Literature]

[0003]

[Patent Literature 1] US 2015/0109862

[Patent Literature 2] US 8,697,982

10 [Patent Literature 3] US 8,787,061

[Summary of the Invention]

[Technical Problem]

[0004]

15 Embodiments provide a semiconductor device capable of preventing an increase in resistance difference of an electrode layer and a method of manufacturing the semiconductor device.

[Solution to Problem]

20 [0005]

 The semiconductor device of the embodiment includes a stacked body, at least two first insulating layers, a first staircase portion, a second staircase portion, and a second insulating layer. The stacked body includes a first electrode layer and a second electrode layer provided to be electrically insulated from the first electrode layer in a stacking direction. The at least two first insulating layers are provided in the stacked body to range from an upper end of the stacked body to a lower end of the stacked body and extend in a first direction intersecting the stacking direction. The first staircase portion is provided in a first end region of the stacked body between the at least two first insulating layers. The second staircase portion is provided in a second end region of the stacked body located on a side opposite to the first end region between the at least two first insulating layers. The second insulating layer extends in the first direction and is provided in the stacked body

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between the at least two first insulating layers. The second insulating layer divides the second electrode layer in the first direction. A length in the first direction of the second insulating layer is longer than a length in the first direction of the second electrode layer and shorter than a length in the first direction of the second electrode layer.

[Brief Description of Drawings]

[0006]

10 FIG. 1 is a schematic plan view of a semiconductor device of a first embodiment;

FIG. 2 is a schematic perspective view of the inside of a one-dot chain line frame A in FIG. 1;

15 FIG. 3 is a schematic plan view of the inside of the one-dot chain line frame A in FIG. 1;

FIG. 4 is a schematic cross-sectional view taken along line IV-IV in FIG. 3;

FIG. 5 is an enlarged schematic cross-sectional view showing one example of the column-shaped portion;

20 FIG. 6 is a schematic perspective view of the semiconductor device of the first embodiment;

FIG. 7 is a schematic plan view of the semiconductor device of the first embodiment;

25 FIG. 8 is a schematic perspective view of a semiconductor device of a reference example;

FIGS. 9A and 9B are schematic plan views of a semiconductor device of another reference example;

FIG. 10 is a schematic cross-sectional view showing a variation of the first embodiment;

30 FIG. 11 is a schematic perspective view of a semiconductor device of a second embodiment;

FIG. 12 is a schematic plan view of the semiconductor device of the second embodiment;

35 FIG. 13 is a schematic perspective view of a semiconductor device according to a third embodiment;

FIG. 14 is a schematic cross-sectional view of a

semiconductor device of a fourth embodiment;

FIGS. 15A and 15B are schematic plan views showing a method of manufacturing the semiconductor device of the fourth embodiment;

5 FIGS. 16A to 16H are schematic cross-sectional views showing the method of manufacturing the semiconductor device of the fourth embodiment;

FIG. 17 is a schematic plan view of a semiconductor device of a fifth embodiment;

10 FIG. 18 is a schematic cross-sectional view taken along line XVIII-XVIII in FIG. 17;

FIG. 19 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

15 FIG. 20 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

20 FIG. 21 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

FIG. 22 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

25 FIG. 23 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

FIG. 24 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

30 FIG. 25 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

35 FIG. 26 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

FIG. 27 is a schematic cross-sectional view showing a

method of manufacturing the semiconductor device of the fifth embodiment;

FIG. 28 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment;

FIG. 29 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment; and

FIG. 30 is a schematic cross-sectional view showing a method of manufacturing the semiconductor device of the fifth embodiment.

[Description of Embodiments]

[0007]

Hereinafter, embodiments will be described with reference to the drawings. In each figure, the same components are denoted by the same reference numerals. In the embodiment, "up" denotes a direction away from, for example, a substrate, and "down" denotes a direction towards, for example, a substrate. The semiconductor device of the embodiment is a semiconductor storage device having a memory cell array.

[0008]

(First Embodiment)

<Semiconductor Device>

FIG. 1 is a schematic plan view of a semiconductor device of a first embodiment. FIG. 2 is a schematic perspective view of the inside of a one-dot chain line frame A in FIG. 1. In FIG. 1 and FIG. 2, two directions parallel to a major surface of a substrate 10 and perpendicular to each other are defined as an X-direction (first direction) and a Y-direction (second direction), and a direction intersecting, for example, a direction perpendicular to both the X-direction and the Y-direction is defined as a Z-direction (stacking direction of a stacked body 100).

[0009]

As shown in FIG. 1 and FIG. 2, the semiconductor device of the first embodiment includes a memory cell array 1 and a staircase portion 2. The memory cell array 1 and the staircase portion 2 are provided in the stacked body 100. The stacked body 100 is provided on a major surface 10a of the substrate 10. The substrate 10 includes, for example, a crystallized silicon layer. The conductivity type of the silicon layer is, for example, a p-type.

[0010]

In the range shown in FIG. 1, two staircase portions 2 are shown. One of the staircase portions 2 is provided in a first end region 101 of the stacked body 100. The other staircase portion 2 is provided in a second end region 102 of the stacked body 100. The second end region 102 is on a side opposite to the first end region 101 in the X-direction. The memory cell array 1 is provided in an intermediate region 103 between the first end region 101 and the second end region 102. In the range shown in FIG. 1, the memory cell array 1 is adjacent to the two staircase portions 2 in the X-direction.

[0011]

The stacked body 100 includes multiple insulators 40 and multiple electrode layers 41 which are alternately stacked. The electrode layer 41 contains a conductive material. The conductive material is, for example, conductive silicon (Si), tungsten (W), molybdenum (Mo), or the like. The insulator 40 contains an insulating material, which is, for example, silicon oxide. The insulating material may be an air gap. The electrode layer 41 is provided in the stacked body 100 so as to be electrically insulated in the Z-direction by the insulator 40.

[0012]

The electrode layer 41 includes at least one source-side selection gate (SGS), multiple word lines (WL), and at least one drain-side selection gate (SGD). SGS is a gate electrode of a source-side select transistor (STS). WL is a gate electrode of a memory cell (MC). SGD is a gate electrode of a drain-side select transistor (STD). Any number of electrode layers 41

may be stacked.

[0013]

The SGS is provided in a lower region of the stacked body 100. The SGD is provided in an upper region of the stacked body 100. The lower region denotes the region of the stacked body 100 close to the substrate 10, and the upper region denotes the region of the stacked body 100 far from the substrate 10. For example, at least one of the multiple electrode layers 41 including the electrode layer 41 closest to the substrate 10 is the SGS. At least one of the multiple electrode layers 41 including the electrode layer 41 farthest from the substrate 10 is the SGD. The WL is provided between the SGS and the SGD.

[0014]

The semiconductor device of the first embodiment has multiple MCs connected in series between the STD and the STS. The structure where the STD, the MC, and the STS are connected in series is called a "memory string (or a NAND string)". The memory string is connected to a bit line (BL), for example, via a contact Cb. The BL is provided above the stacked body 100 and extends in the Y-direction.

[0015]

FIG. 3 is a schematic plan view of the inside of the one-dot chain line frame A in FIG. 1. FIG. 4 is a schematic cross-sectional view taken along line IV-IV in FIG. 3.

[0016]

In the stacked body 100, a first slit ST, a second slit SHE, and a column-shaped portion CL are provided.

[0017]

The first slit ST is provided to range from the upper end of the stacked body 100 to the lower end of the stacked body 100. In the range shown in FIG. 3 and FIG. 4, two first slits ST are shown. The two first slits extend in the X-direction. A first insulating layer 45 is provided on the side wall of the first slit ST. The first insulating layer 45 contains an insulating material. The insulating material is, for example, silicon oxide.

The stacked body 100 is divided in the X-direction by the first insulating layer 45. The region of the stacked body 100 interposed between the two first slits is called block (BLOCK). The BLOCK becomes, for example, a minimum unit of information erase. The erase size is set to one BLOCK or a combination of multiple BLOCKs.

[0018]

A conductive layer LI is provided along the first insulating layer 45 in the first slit ST. The conductive layer LI reaches the substrate 10. An n-type semiconductor layer 11 is provided in the substrate 10. The conductive layer LI is electrically connected to the semiconductor layer 11. The conductive layer LI contains a conductive material. The conductive material is, for example, W. The conductive layer LI functions as, for example, a source line (SL).

[0019]

The second slit SHE is provided in the BLOCK of the stacked body 100. The second slit SHE extends in the X-direction. Unlike the first slit ST, the second slit SHE needs not to be provided to range from the upper end of the stacked body 100 to the lower end of the stacked body 100. The second slit SHE may divide the SGD into, for example, two SGDs in the X-direction within one BLOCK. A second insulating layer 46 is provided in the second slit SHE. The second insulating layer 46 contains an insulating material. The insulating material is, for example, silicon oxide. The second insulating layer 46 extends in the X-direction and divides the SGD into two SGDs in the X-direction. In the specification, one of the two divided SGDs is called an "SGD0", and the other one is called an "SGD1". The memory string including the SGD0 belongs to "String0". The memory string including the SGD1 belongs to "String1". The "String0" and the "String1" are connected in parallel between the SL and the BL.

[0020]

In the semiconductor device shown in FIG. 4, the SGD0 includes three of SGDA0 to SGDC0. The SGDA0 to the SGDC0

are electrically connected to each other. The SGD1 includes three of SGDA1 to SGDC1. The SGDA1 to the SGDC1 are electrically connected to each other. The SGS includes one SGSA. The WL includes a drain-side dummy word line (WLDD) and a source-side dummy word line (WLDS) in addition to n WLS of WL0 to WLn-1 actually used.

[0021]

The WLDD is provided between the WLn-1 and the SGDA0 and between the WLn-1 and the SGDA1. The WLDD of the embodiment includes three of WLDD0 to WLDD2.

[0022]

The WLDS is provided between the WL 0 and the SGSA. The WLDS of the embodiment includes two of WLDS0 to WLDS1.

[0023]

The column-shaped portion CL is provided in the intermediate region 103 of the stacked body 100 shown in FIG. 1. The column-shaped portion CL extends in the Z-direction and is provided to range from the upper end of the stacked body 100 to the lower end of the stacked body 100.

[0024]

FIG. 5 is an enlarged schematic cross-sectional view showing one example of the column-shaped portion. The cross section shown in FIG. 5 corresponds to, for example, the cross section shown in FIG. 4.

[0025]

As shown in FIG. 5, a memory hole MH is provided in the stacked body 100. The memory hole MH is an opening extending in the Z-direction. The column-shaped portion CL is provided in the memory hole MH. The memory hole MH is formed in a column shape or an elliptical column shape. The lower end of the memory hole MH reaches the substrate 10.

[0026]

The column-shaped portion CL includes a memory film 30, a semiconductor body 20, and a core layer 50. The memory film 30, the semiconductor body 20, and the core layer 50 are

provided in the memory hole MH. The memory film 30 includes a charge storage portion in the film. The charge storage portion includes, for example, a trap site that traps charges and/or a floating gate. The threshold voltage of the MC varies
5 depending on the presence or absence of charges or the amount of charges in the charge storage portion. Accordingly, the MC retains information. Although omitted in FIG. 5, the memory film 30 has a tunnel insulating film between the charge storage portion and the semiconductor body 20.

10 [0027]

Similarly, although omitted in FIG. 5, the memory film 30 is provided with a first block insulating film between the charge storage portion and the electrode layer 41. When erasing information and programing information, in the tunnel
15 insulating film, charge tunneling, for example, electron and hole tunneling occurs. The memory film 30 may be removed in the portion where the electrode layer 41 which is to be the SGD (SGDA to SGDC) is formed. In this case, instead of the memory film 30, a gate insulating film of the STD is provided.

20 [0028]

The semiconductor body 20 extends in the Z-direction. The semiconductor body 20 contains, for example, crystallized P-type silicon. The semiconductor body 20 is electrically connected to the substrate 10 via, for example, a
25 semiconductor pillar 10b. The semiconductor pillar 10b is provided on the bottom of the memory hole MH. The semiconductor pillar 10b contains, for example, crystallized P-type silicon. The semiconductor pillar 10b is in contact with the substrate 10 and constitutes a portion of the substrate 10.
30 The semiconductor pillar 10b faces, for example, the electrode layer 41 (SGSA) via a gate insulating film 31. The semiconductor pillar 10b may be omitted. In a case where the semiconductor pillar 10b is omitted, for example, the memory film 30 and the semiconductor body 20 extend to the portion
35 where the STS is formed, and the semiconductor body 20 is in direct contact with the substrate 10.

[0029]

The core layer 50 contains an insulating material. The insulating material is, for example, silicon oxide. The core layer 50 buries the memory hole MH provided with the memory film 30 and the semiconductor body 20.

[0030]

A second block insulating film 42 is provided between the electrode layer 41 and the insulator 40 and between the electrode layer 41 and the memory film 30. The second block insulating film 42 contains, for example, silicon oxide and aluminum oxide. The second block insulating film 42 prevents back tunneling of charges from the WL to the charge storage portion in the memory film 30, for example, during the erasing operation.

[0031]

FIG. 6 is a schematic perspective view of the semiconductor device of the first embodiment. FIG. 6 shows the electrode layers 41 (SGDA0 to SGDC 3, WLDD0, WLDD, and WLn-1). FIG. 7 is a schematic plan view of the semiconductor device of the first embodiment.

[0032]

As shown in FIGS. 6 and 7, the second insulating layer 46 divides the three electrode layers 41 which are to be the SGDs into six electrode layers 41 (SGDA0) to 41 (SGDC3) in the X-direction. The electrode layers 41 (SGDA0) to 41 (SGDC0) belong to the String0.

[0033]

For example, a signal Ssgd0 is commonly supplied from a drain-side selection gate driving circuit (not shown) to the electrode layers 41 (SGDA0) to 41 (SGDC0) via a first interconnection 60. The first interconnection 61 is provided, for example, above the first end region 101.

[0034]

The electrode layers 41 (SGDA1) to 41 (SGDC1) belongs to the String1. For example, a signal Ssgd1 is commonly supplied to the electrode layers 41 (SGDA1) to 41 (SGDC1)

from a drain-side selection gate driving circuit (not shown) via a second interconnection 62. The second interconnection 61 is provided, for example, above the first end region 101.

[0035]

5 A third interconnection 63 is provided above the second end region 102. The third interconnection 63 short-circuits the electrode layers 41 (SGDA0) to 41 (SGDC0) with each other in the second end region 102. Similarly, a fourth interconnection 64 is provided above the second end region 102. The fourth
10 interconnection 64 short-circuits the electrode layers 41 (SGDA1) to 41 (SGDC1) with each other in the second end region.

[0036]

15 The second insulating layer 46 reaches one of the electrode layers 41 which are to be the WL, for example, the electrode layer 41 which is to be the WLDD. In FIG. 6, the second insulating layer 46 reaches the electrode layer 41 (WLDD0).

[0037]

20 The length L1 of the second insulating layer 46 in the X-direction is greater than the length L2 of each of the electrode layer 41 (SGDA0) and the electrode layer 41 (SGDA1) in the X-direction. The electrode layer 41 (SGDA0) and the electrode layer 41 (SGDA1) are the electrode layers having the
25 longest length in the X-direction among the electrode layers 41 which are to be the SGD.

[0038]

30 However, the length L1 of the second insulating layer 46 of the first embodiment in the X-direction is smaller than the length L3 of the electrode layer 41 (WLDD0) in the X-direction. The electrode layer 41 (WLDD0) is the electrode layer having the shortest length in the X-direction among the electrode layers 41 which are to be the WL.

[0039]

35 According to the first embodiment, even if the second insulating layer 46 reaches the electrode layer 41 which is to be

the WL and the second insulating layer 46 completely penetrates, for example, the electrode layer 41 which is to be the WL, the electrode layer 41 which is to be the WL can be prevented from being divided by the second insulating layer 46.

5 For example, in the example shown in FIG. 6 and FIG. 7, the electrode layer 41 (WLDD0) may be connected in both the first end region 101 and the second end region 102.

[0040]

For example, when the electrode layer 41 (WLDD0) is
10 divided by the second insulating layer 46, the following situation occurs.

[0041]

FIG. 8 is a schematic perspective view of a
semiconductor device of a reference example. The portions
15 shown in FIG. 8 correspond to the portions shown in FIG. 6.

[0042]

As shown in FIG. 8, when the electrode layer 41 (WLDD0) is divided by the second insulating layer 46, for example, the resistance of the electrode layer 41 is increased as
20 compared with the undivided electrode layer 41 (WLDD1). For example, the width of the electrode layer 41 (WLDD0) in the Y-direction is decreased by the amount of the second insulating layer 46 provided. For this reason, the cross-sectional area of the electrode layer 41 (WLDD0) in the Y-direction is decreased,
25 and thus, the resistance is increased.

[0043]

For the reference example, in the first embodiment, as shown in FIGS. 6 and 7, the electrode layer 41 (WLDD0) remains connected, for example, in both the first end region
30 101 and the second end region 102. For this reason, even if the second insulating layer 46 is penetrated, the electrode layer 41 (WLDD0) has a "resistance of parallel connection" in terms of an equivalent circuit. Therefore, according to the first embodiment, it is possible to prevent an increase in resistance
35 of the electrode layer 41 (WLDD0) as compared with the reference example shown in FIG. 8.

[0044]

In the reference example shown in FIG. 8, it is assumed that a connection node between a word line driving circuit (not shown) and the electrode layer 41 (WLDD0) is provided in the first end region 101. In this case, the electrode layer 41 (WLDD0) is charged and discharged from the first end region 101 towards the second end region 102. In the figure, "Near" indicates a side close to the connection node, and "Far" indicates a side far from the connection node.

10 [0045]

Herein, it is assumed that the width W0 on the String0 side and the width W1 on the String1 side in the Y-direction of the electrode layer 41 (WLDD0) are different. In this case, the resistance of the electrode layer 41 (WLDD0) on the String0 side and the resistance of the electrode layer 41 (WLDD0) on the String1 side are different. For this reason, a difference occurs between the charging/discharging time of the electrode layer 41 (WLDD0) on the String0 side and the charging/discharging time of the electrode layer 41 (WLDD0) on the String1 side.

20 [0046]

The difference in charging/discharging time becomes a delay difference between the "rising/falling time" of the electrode layer 41 (WLDD0) in the String0 and the "rising/falling time" of the electrode layer 41 (WLDD0) in the String1.

25 [0047]

In order to correctly operate the semiconductor device, the operation timing needs to be coincident with one String with a slow "rising/falling time" between the String0 and the String1. This hinders the improvement of the performance of the semiconductor device, for example, speeding up the operation.

30 [0048]

In contrast to such a reference example, in the first embodiment, as shown in FIGS. 6 and 7, the electrode layer 41 (WLDD0) is connected in the second end region 102. For this

reason, in the second end region 102, the charging/discharging is performed from the String with a fast "rising/falling time" between the String0 and the String1 toward the String with a slow "rising/falling time".

5 [0049]

In the example shown in FIGS. 6 and 7, it is assumed that the "rising/falling time" in the String0 is faster than the "rising/falling time" in the String1. In this case, the charging/discharging of the electrode layer 41 (WLDD0) in the String0 is completed before the charging/discharging of the electrode layer 41 (WLDD0) in the String1. When the charging/discharging of the String0 reaches the second end region 102, the charging/discharging is repeatedly performed toward the String1. The direction in which the charging/discharging is performed is indicated by a "dotted arrow" in FIGS. 6 and 7. Reference numeral "CC" shown in FIG. 7 indicates a connection node between a word line driving circuit (not shown) and the electrode layer 41 (WLDD0).

[0050]

20 As described above, in the first embodiment, in the second end region 102 far from the connection node with the word line driving circuit (not shown), the charging/discharging can be performed from the String with a fast "rising/falling time" toward the String with a slow "rising/falling time". For this reason, as compared with the reference example, the delay difference between the "rising/falling time" in the String0 and the "rising/falling time" in the String1 can be reduced. Therefore, as compared with the reference example, the first embodiment has an advantage of improving the performance of the semiconductor device, for example, increasing the speed of the operation.

[0051]

FIGS. 9A and 9B are schematic plan views of a semiconductor device of another reference example. Another reference example is an example in which, for example, after forming the column-shaped portion CL in the stacked body 100,

the first slit ST is formed in the stacked body 100.

[0052]

As shown in FIGS. 9A and 9B, the resistance of the electrode layer 41 depends on the width S_y of a region S in the Y-direction, for example, between the first slit ST and a column-shaped portion CLedg closer to the first slit ST. No column-shaped portion CL is provided to the region S.

For this reason, it is easy to keep the resistance of the region S low.

10 [0053]

FIG. 9A shows a case where there is no "misalignment" of the photomask between the column-shaped portion CL and the first slit ST. In this case, the width S_y is equal in both the String0 and the String1. For this reason, the resistance of the region S is equal in both the String0 and the String1. Therefore, there is no difference between the charging/discharging time of the electrode layer 41 (WLDD0) on the String0 side and the charging/discharging time of the electrode layer 41 (WLDD0) on the String1 side.

20 [0054]

FIG. 9B shows a case where "misalignment" of the photomask occurs between the column-shaped portion CL and the first slit ST. In another reference example shown in FIG. 9B, for example, the photomask used for forming the first slit ST is shifted by " Δma " in the Y-direction. In this case, the width S_y is, for example, narrow in the String0 and is wide in the String1. For this reason, the resistance of the region S is high in the String0 and is low in the String1. Therefore, as in the reference example shown in FIG. 8, a difference occurs between the charging/discharging time of the electrode layer 41 (WLDD0) on the String0 side and the charging/discharging time of the electrode layer 41 (WLDD0) on the String1 side. The difference in charging/discharging time becomes a delay difference between the "rising/falling time" of the electrode layer 41 (WLDD0) in the String0 and the "rising/falling time" of the electrode layer 41 (WLDD0) in the String1.

[0055]

Such a delay difference is remarkably likely to occur in the semiconductor device in which the second slit SHE is provided to overlap, for example, a column-shaped portion CLctr disposed at the center of the BLOCK in the Y-direction. This is because the region in which there is no column-shaped portion CL like the region S is not between the second slit SHE and the column-shaped portion CL.

[0056]

For another reference example, in the first embodiment, as shown in FIGS. 6 and 7, the electrode layer 41 (WLDD0) remains connected, for example, in both the first end region 101 and the second end region 102. Therefore, even if the resistance of the region S is different between the String0 and the String1, as compared with another reference example, the delay difference between the "rising/falling time" in the String0 and the "rising/falling time" in the String1 can be reduced. Therefore, as compared with another reference example, the first embodiment has an advantage of improving the performance of the semiconductor device, for example, increasing the speed of the operation.

[0057]

FIG. 10 is a schematic cross-sectional view showing a variation of the first embodiment. The cross section shown in FIG. 10 corresponds to, for example, the cross section shown in FIG. 4.

[0058]

As shown in FIG. 10, the variation is different from the first embodiment shown in FIG. 4, for example, in that the second slit SHE is provided to overlap the column-shaped portion CL. The second slit SHE is provided in the column-shaped portion CL, for example, on the column-shaped portion CLctr disposed at the center in the Y-direction of the BLOCK.

[0059]

For example, as described with reference to FIG. 9, in a

case where the second slit SHE is provided to overlap the column-shaped portion CL, if the "misalignment" of the photomask occurs between the column-shaped portion CL and the first slit ST, the delay difference between the "rising/falling time" in the String0 and the "rising/falling time" in the String1 is easily increased.

[0060]

However, in the first embodiment, the electrode layer 41 (WLDD0) is maintained to be connected to, for example, both the first end region 101 and the second end region 102. For this reason, it is possible to reduce the delay difference between the "rising/falling time" in the String0 and the "rising/falling time" in the String1.

[0061]

Therefore, the first embodiment can be more effectively applied to the semiconductor device in which the second slit SHE is provided to overlap the column-shaped portion CL as shown in FIG. 10. The variation shown in FIG. 10 can also be applied to all the embodiments described below.

[0062]

(Second Embodiment)

<Semiconductor Device>

FIG. 11 is a schematic perspective view of a semiconductor device of a second embodiment. The portion shown in FIG. 11 corresponds to the portion shown in FIG. 6.

[0063]

As shown in FIG. 11, the second embodiment is different from the first embodiment shown in, for example, FIG. 6 in that a fifth interconnection 65 is provided. The fifth interconnection 65 electrically connects the electrode layer 41 (WLDD0) and the electrode layer 41 (WLDD1). The signal Swldd from the word line driving circuit (not shown) is supplied to the fifth interconnection 65.

[0064]

The fifth interconnection 65 is provided above at least one of the first end region 101 and the second end region 102.

In the second embodiment, the fifth interconnection 65 includes a fifth interconnection 65a provided above the first end region 101 and a fifth interconnection 65b provided above the second end region 101.

5 [0065]

According to the second embodiment, the fifth interconnection 65 electrically connects the electrode layer 41 (WLDD0) and the electrode layer 41 (WLDD1). For this reason, even if the electrode layer 41 (WLDD0) is divided by the second
10 insulating layer 46, similarly to the first embodiment, the delay difference between the "rising/falling time" in the String0 and the "rising/falling time" in the String1 can be reduced.

[0066]

In this manner, the fifth interconnection 65 for
15 electrically connecting the electrode layer 41 (WLDD0) and the electrode layer 41 (WLDD1) may be provided above at least one of the first end region 101 and the second end region 102.

[0067]

Furthermore, in the second embodiment, the electrode
20 layer 41 (WLDD0) and the electrode layer 41 (WLDD1) are electrically connected to each other by the fifth interconnection 65. For this reason, for example, similarly to the reference example shown in FIG. 8, the electrode layer 41 (WLDD0) may be divided by the second insulating layer 46.

25 [0068]

<Example of Planar Pattern of Fifth Interconnection 65>

FIG. 12 is a schematic plan view of the semiconductor device of the second embodiment. The plane shown in FIG. 12 corresponds to the plane shown in FIG. 7. FIG. 12 shows one
30 example of the planar pattern of the fifth interconnection 65.

[0069]

The fifth interconnection 65a includes, for example, contacts CCa00 to CCa11. The contacts CCa00 to CCa11 extend in the Z-direction. The contacts CCa00 and CCa01
35 belong to String0. The contacts CCa10 and CCa11 belong to String1.

[0070]

The fifth interconnection 65b includes, for example, contacts CCb00 to CCb11. The contacts CCb00 to CCb11 have, for example, the same structure as the contacts CCa00 to CCa11. Each of the contacts CCa00 to CCb11 contains a conductive material. An example of the conductive material is W.

[0071]

The contact CCa00 is electrically connected to the String0 side of the electrode layer 41 (WLDD0) in the first end region 101. Similarly, the contact CCa01 is electrically connected to the electrode layer 41 (WLDD1). The contact CCa10 is electrically connected to the String1 side of the electrode layer 41 (WLDD0). The contact CCa11 is electrically connected to the electrode layer 41 (WLDD1).

[0072]

The contact CCb00 is electrically connected to the String0 side of the electrode layer 41 (WLDD0) in the second end region 102. Similarly, the contact CCb01 is electrically connected to the electrode layer 41 (WLDD1). The contact CCb10 is electrically connected to the String1 side of the electrode layer 41 (WLDD0). The contact CCb11 is electrically connected to the electrode layer 41 (WLDD1).

[0073]

A sixth interconnection 66 is provided above the contacts CCa00 to CCb11. The second embodiment includes sixth interconnections 66a and 66b. The sixth interconnection 66a is electrically connected to the contacts CCa00 to CCa11 above the first end region 101. The sixth interconnection 66b is electrically connected to the contacts CCb00 to CCb11 above the second end region 102.

[0074]

The signal Swldd is supplied from the word line driving circuit (not shown) to the sixth interconnection 66a via a seventh interconnection 67. The seventh interconnection 67 is provided, for example, above the sixth interconnection 66a.

[0075]

In the case of implementing the semiconductor device of the second embodiment, for example, a planar pattern as shown in FIG. 12 may be used.

5 [0076]

(Third Embodiment)

<Semiconductor Device>

FIG. 13 is a schematic perspective view of a semiconductor device according to a third embodiment. The portion shown in FIG. 13 corresponds to the portion shown in FIG. 6.

[0077]

As shown in FIG. 13, the third embodiment is an example of a combination of, for example, the second embodiment shown in FIG. 11 and the first embodiment shown in FIG. 6.

[0078]

Similarly to the third embodiment, the second embodiment may be combined with the first embodiment.

[0079]

20 (Fourth Embodiment)

<Semiconductor Device>

FIG. 14 is a schematic cross-sectional view of a semiconductor device of a fourth embodiment. The cross section shown in FIG. 14 corresponds to the cross section shown in FIG. 4. FIG. 14 is an enlarged view of the upper layer portion of the stacked body 100 around the second slit ST.

[0080]

As shown in FIG. 14, for example, the fourth embodiment is different from the second embodiment shown in FIG. 11 in that a fifth interconnection 65c for electrically connecting the electrode layer 41 (WLDD0) and the electrode layer 41 (WLDD1) is provided in the stacked body 100. The fifth interconnection 65c is provided below the second insulating layer 46. The fifth interconnection 65c is provided, for example, in the second slit SHE and extends in the Z-direction. In the embodiment, the fifth interconnection 65c is along the

column-shaped portion CL. The column-shaped portion CL is, for example, a dummy column-shaped portion CLshe provided to penetrate the second slit SHE.

[0081]

5 In the fourth embodiment, the column-shaped portion CLshe is also provided in the second insulating layer 46. The column-shaped portion CLshe has the same structure as the other column-shaped portion CL. The column-shaped portion CLshe is provided at the same position as, for example, the
 10 column-shaped portion CLctr shown in FIGS. 9 and 10. The fifth interconnection 65c is provided along the column-shaped portion CLshe. However, the structure shown in FIG. 14 is one example, and the fourth embodiment is not limited to the structure shown in FIG. 14. The fifth interconnection 65c may
 15 be provided in the stacked body 100 and may be electrically connected to the electrode layer 41 (WLDD0) and the electrode layer 41 (WLDD1).

[0082]

<Manufacturing Method>

20 FIGS. 15A and 15B are schematic plan views showing a method of manufacturing the semiconductor device of the fourth embodiment. The planes shown in FIGS. 15A and 15B correspond to the planes shown in FIG. 1. FIGS. 16A to 16H are schematic cross-sectional views showing the method of
 25 manufacturing the semiconductor device of the fourth embodiment. The cross sections shown in FIGS. 16A to 16H correspond to the cross section along line XVI-XVI in FIGS. 15A and 15B. FIG. 15A to FIG. 16H show one example of the method of manufacturing the semiconductor device of the
 30 fourth embodiment.

[0083]

1. Formation of Stacked Body 100

As shown in FIG. 15A and FIG. 16A, the stacked body 100 is formed on the substrate 10 (not shown in FIG. 15A and
 35 FIG. 16A). The stacked body 100 is formed by alternately stacking the insulators 40 and first sacrificial layers 47 in the

Z-direction. The material of which etching selection ratio of each other can be obtained is selected for the insulator 40 and the first sacrificial layer 47. For example, in a case where silicon oxide is selected for the insulator 40, for example, silicon nitride is selected for the first sacrificial layer 47.

[0084]

2. Formation of Staircase Portion 2

As shown in FIG. 15B, the staircase portion 2 is formed in the first end region 101 and the second end region 102. The staircase portion 2 is formed by a well-known method such as "resist slimming method". Accordingly, the staircase portion 2 and the memory cell array 1 are obtained in the stacked body 100.

[0085]

3. Formation of Second Slit SHE

As shown in FIG. 16B, the second slit SHE is formed in the stacked body 100. The second slit SHE is formed in the stacked body 100 by, for example, anisotropic etching by using a photoresist as a mask. In the embodiment, the second slit SHE is formed so as to reach, for example, the first sacrificial layer 47 which is to be replaced with the WLDD1.

[0086]

4. Formation of Second Sacrificial Layer 48

As shown in FIG. 16C, a second sacrificial layer 48 is formed on the stacked body 100. For example, the same material as the first sacrificial layer 47 is selected as the material of the second sacrificial layer 48. For example, in a case where the first sacrificial layer 47 is silicon nitride, the silicon nitride is selected for the second sacrificial layer 48. The thickness of the second sacrificial layer 48 is set to a level that allows the second slit SHE to be buried. Next, the second sacrificial layer 48 is, for example, etched back, and the second slit SHE is buried by the second sacrificial layer 48.

[0087]

5. Recess of Second Sacrificial Layer 48

As shown in FIG. 16D, the second sacrificial layer 48 is

recessed. The second sacrificial layer 48 remains to bury the first sacrificial layer 47 which is to be replaced with, for example, the WLDD0 and the WLDD1 in the second slit SHE. Reference numeral 70 indicates a portion where the second sacrificial layer 48 is recessed.

[0088]

6. Formation of Second Insulating Layer 46

As shown in FIG. 16E, the second insulating layer 46 is formed on the stacked body 100. For example, the same material as the insulator 40 is selected as the material of the second insulating layer 46. For example, in a case where the insulator 40 is silicon oxide, the silicon oxide is selected for the second insulating layer 46. The thickness of the second insulating layer 46 is set to a level that allows the recessed portion 70 to be buried. Next, the second insulating layer 46 is, for example, etched back, and the recessed portion 70 is buried by the second insulating layer 46.

[0089]

7. Formation of Memory Hole MH

As shown in FIG. 16F, the memory hole MH is formed in the stacked body 100. The memory hole MH is formed in the stacked body 100 by, for example, anisotropic etching by using a photoresist as a mask. The memory hole MH is formed to penetrate the stacked body 100 and to reach the substrate 10 (not shown). In the embodiment, the memory hole MH is also formed in a portion 71 where the second slit SHE is formed. In the portion 71, the memory hole MH penetrates the second insulating layer 46 and the second sacrificial layer 48.

[0090]

8. Formation of Column-Shaped Portion CL

As shown in FIG. 16G, the column-shaped portion CL is formed in the memory hole MH. By the column-shaped portion CL, for example, the memory film 30 is formed on the stacked body 100. Next, the portion of the memory film 30 on the bottom (not shown) of the memory hole MH is removed, and thus, the substrate 10 (not shown) is exposed from the bottom

of the memory hole MH. Next, the semiconductor body 20 is formed on the memory film 30. Next, the core layer 50 is formed on the semiconductor body 20. The core layer 50 buries the memory hole MH in which the memory film 30 and the semiconductor body 20 are formed.

[0091]

9. Removal of First Sacrificial Layer 47 and Second Sacrificial Layer 48 (Replacement Staircase)

As shown in FIG. 16H, the first slit ST (not shown) is formed in the stacked body 100. Next, the first sacrificial layer 47 and the second sacrificial layer 48 are removed via the first slit ST. Accordingly, a space 43 is formed between the insulators 40. In the embodiment, the space 43 is also formed in a portion under a second insulating layer 46b. The space 43 formed under the second insulating layer 46b is formed to range over the space 43 existing along the column-shaped portion CL in the Z-direction via the insulator 40.

[0092]

10. Burying of Electrode Layer 41 (Replacement Process)

As shown in FIG. 14, the space 43 is buried by the electrode layer 41. Accordingly, the electrode layer 41 and the fifth interconnection 65c are formed in the stacked body 100.

[0093]

The semiconductor device of the fourth embodiment may be manufactured, for example, by the manufacturing method shown in FIG. 15A to FIG. 16H.

[0094]

(Fifth Embodiment)

<Semiconductor Device>

FIG. 17 is a schematic plan view of a semiconductor device of a fifth embodiment. A plane shown in FIG. 17 corresponds to the plane shown in FIG. 3. FIG. 18 is a schematic cross-sectional view taken along line XVIII-XVIII in FIG. 17.

[0095]

As shown in FIGS. 17 and 18, the fifth embodiment is

different from, for example, the fourth embodiment shown in FIG. 14 in that an eighth interconnection 68 is provided. Similarly to the fifth interconnection 65c, the eighth interconnection 68 is provided in the stacked body 100 and extends in the Z-direction.

[0096]

The eighth interconnection 68 is different from the fifth interconnection 65c of the fourth embodiment in that the fifth interconnection 65c electrically connects the electrode layer 41 (WLDD0) and the electrode layer 41 (WLDD1) which are to be the dummy word line and the eighth interconnection 68 electrically connects the electrode layers 41 (SGDA) to 41 (SGDC) which are to be the drain-side selection gates. In the fifth embodiment, there are three types of eighth interconnections 680 to 682. The eighth interconnection 680 electrically connects the electrode layers 41 (SGDA0) to (SGDC0) belonging to the String0. The eighth interconnection 681 electrically connects the electrode layers 41 (SGDA1) to (SGDC1) belonging to the String1. The eighth interconnection 682 electrically connects the electrode layers 41 (SGDA2) to (SGDC 2) belonging to the String 2.

[0097]

Similarly to the fifth interconnection 65c, the eighth interconnection 68 is provided in the second slit SHE. In the fourth embodiment, although the example in which the column-shaped portion CL is provided also in the second slit SHE is shown, in the fifth embodiment, the case where the column-shaped portion CL is not provided in the second slit SHE is shown.

[0098]

According to the fifth embodiment, the electrode layers 41 (SGDA), 41 (SGDB), and 41 (SGDC) are electrically connected by the eighth interconnection 68. For this reason, the delay difference in the "rising/falling time" between the Strings can be reduced.

[0099]

In the fifth embodiment, three Strings of the String0 to the String 2 are provided in one BLOCK. In the semiconductor device with the second slit SHE which stops in the middle of the stacked body 100, the number of Strings provided in one BLOCK is usually two. One reason why more than two Strings can be provided in one BLOCK is due to the manufacturing method described below.

[0100]

<Manufacturing Method>

FIG. 19 to FIG. 30 are schematic cross-sectional views showing a method of manufacturing the semiconductor device of the fifth embodiment. The cross sections shown in FIG. 19 to FIG. 30 correspond to the cross sections shown in FIG. 18. FIG. 19 to FIG. 30 show one example of the method of manufacturing the semiconductor device of the fifth embodiment.

[0101]

1. Formation of Stacked Body 100

As shown in FIG. 19, for example, the stacked body 100 is formed on the major surface 10a of the substrate 10 by the same method as the method described with reference to FIG. 15A and FIG. 16A.

[0102]

2. Formation of Staircase Portion 2

Although not particularly shown, the staircase portion 2 is formed in the first end region 101 and the second end region 102 of the stacked body 100 by a method similar to, for example, the method described with reference to FIG. 15B.

[0103]

3. Formation of Memory Hole MH

As shown in FIG. 20, for example, the memory hole MH is formed in the stacked body 100 by a method similar to, for example, the method described with reference to FIG. 16F.

[0104]

4. Formation of Column-Shaped Portion CL

As shown in FIG. 21, for example, the column-shaped

portion CL is formed in the memory hole MH by a method similar to, for example, the method described with reference to FIG. 16G. Next, the third insulating layer 31 is formed on the stacked body 100 on which the column-shaped portion CL is formed. The third insulating layer 31 contains an insulating material. The insulating material is, for example, silicon oxide. [0105]

5. Formation of Second Slit SHE

As shown in FIG. 22, the second slit SHE is formed in the stacked body 100 by a method similar to, for example, the method described with reference to FIG. 16B. In the embodiment, the second slit SHE is formed so as to reach, for example, the first sacrificial layer 47 which is to be replaced with the SGDA.

[0106]

6. Formation of Third Sacrificial Layer 49

As shown in FIG. 23, a third sacrificial layer 49 is formed on the side wall of the second slit SHE. For example, the same material as the first sacrificial layer 47 is selected as the material of the third sacrificial layer 49. For example, when the first sacrificial layer 47 is silicon nitride, the silicon nitride is selected for the third sacrificial layer 49.

[0107]

7. Formation of Second Insulating Layer 46

As shown in FIG. 24, the second insulating layer 46 is formed in the second slit SHE formed with the third sacrificial layer 49. For example, the same material as the insulator 40 is selected as the material of the second insulating layer 46. For example, in a case where the insulator 40 is silicon oxide, the silicon oxide is selected for the second insulating layer 46.

[0108]

8. Formation of First Slit ST

As shown in FIG. 25, the first slit ST is formed in the stacked body 100. The first slit ST is formed so as to reach, for example, the substrate 10. Next, an impurity of a conductivity type different from that of the substrate 10, for

example, an n-type impurity, is introduced into the substrate 10 via the first slit ST. Accordingly, the n-type semiconductor layer 11 is formed in the substrate 10.

[0109]

5 9. Removal of First Sacrificial Layer 47 and Third Sacrificial Layer 49 (Replacement Process)

As shown in FIG. 26, the first sacrificial layer 47 and the third sacrificial layer 49 are removed via the first slit ST and the second slit SHE. Accordingly, the space 43 is formed between
10 the insulators 40. In the embodiment, the first sacrificial layer 47 and the third sacrificial layer 49 are removed, and the space 43 is formed even in the region 104 interposed between the second slits. In the embodiment, the third sacrificial layer 49 is formed in the second slit SHE. For this reason, the space 43
15 can be formed even in the region 104 interposed between the second slits.

[0110]

10 10. Burying of Electrode Layer 41 (Replacement Staircase)

As shown in FIG. 27, the space 43 is buried by the electrode layer 41. Accordingly, the electrode layer 41 and the eighth interconnection 68 are formed in the stacked body 100.

[0111]

15 11. Formation of First Insulating Layer 45

As shown in FIG. 28, the electrode layer 41 is removed from the side wall of the first slit ST. Next, the first insulating layer 45 is formed on the side wall of the first slit ST.

[0112]

20 12. Formation of Conductive Layer LI

As shown in FIG. 29, the first insulating layer 45 is removed from the bottom of the first slit ST. Accordingly, the semiconductor layer 11 is exposed to the bottom of the first slit ST. Next, the conductive layer LI is formed in the first slit ST. The conductive layer LI is electrically connected to the
30 semiconductor 11.

[0113]

13. Formation of First Conductive Material M

As shown in FIG. 30, a fourth insulating layer 52 is formed on the stacked body 100 on which the conductive layer LI is formed. The fourth insulating layer 52 contains an insulating material. The insulating material is, for example, silicon oxide. Next, a first opening 55 is formed in the fourth insulating layer 52 and a third insulating layer 51. The first opening 55 reaches the column-shaped portion CL. Next, a first conductive material M is formed in the first opening 55. The first conductive material M contains, for example, W. The first conductive material M is electrically connected to the semiconductor body 20 (not shown) of the column-shaped portion CL.

[0114]

14. Formation of Second Conductive Material V

Next, a fifth insulating layer 53 is formed on the stacked body 100 on which the first conductive material M is formed. The fifth insulating layer 53 contains an insulating material. The insulating material is, for example, silicon oxide. Next, a second opening 56 is formed in the fifth insulating layer 53. The second opening 56 reaches the first conductive material M. Next, a second conductive material V is formed in the second opening 56. The second conductive material V contains, for example, W. The second conductive material V is electrically connected to the first conductive material M. The first conductive material M and the second conductive material V constitute the contact Cb shown in, for example, FIG. 2.

[0115]

15. Formation of Bit Line BL

Next, the bit line BL is formed on the stacked body 100 on which the second conductive material V is formed.

[0116]

The semiconductor device of the fifth embodiment may be manufactured, for example, by the manufacturing method shown in FIGS. 19 to 30.

[0117]

Heretofore, the first to fifth embodiments have been described. However, the embodiment is not limited to the first to fifth embodiments. These embodiments are presented as
5 examples and are not intended to limit the scope of the invention. These novel embodiments may be implemented in various other forms, and various omissions, substitutions, and changes may be made without departing from the spirit of the invention.

10

Claims

[Claim 1]

A semiconductor device comprising:

5 a stacked body including a first electrode layer, a second electrode layer, and a third electrode layer, the second electrode layer provided to be electrically insulated from the first electrode layer in a stacking direction, the third electrode layer interposed between the second electrode layer and the first electrode layer in
10 the stacking direction and provided to be electrically insulated from the second electrode layer;

 at least two first insulating layers provided in the stacked body to range from an upper end of the stacked body to a lower end of the stacked body, and extending in a first direction
15 intersecting the stacking direction;

 a second insulating layer extending in the first direction, the second insulating layer provided in the stacked body between a third insulating layer and a fourth insulating layer neighboring each other among the at least two first insulating layers, the
20 second insulating layer electrically dividing the second electrode layer into a fourth electrode layer and a fifth electrode layer in a third direction intersecting the stacking direction and the first direction, and electrically dividing the third electrode layer into a sixth electrode layer and a seventh electrode layer in the third
25 direction;

 a plurality of first memory columns extending in the stacking direction through the stacked body and arranged in at least four rows each extending in the first direction between the second insulating layer and the third insulating layer;

30 a plurality of second memory columns extending in the stacking direction through the stacked body and arranged in at least four rows each extending in the first direction between the second insulating layer and the fourth insulating layer;

a first staircase portion in a first end region of the stacked body between the at least two first insulating layers;

a first interconnection electrically connecting the fourth electrode layer and the sixth electrode layer; and

5 a second interconnection electrically connecting the fifth electrode layer and the seventh electrode layer, wherein

each of the plurality of first memory columns includes a first semiconductor body extending in the stacking direction, and a first charge storage portion provided between the first semiconductor
10 body and the first electrode layer, and

each of the plurality of second memory columns includes a second semiconductor body extending in the stacking direction, and a second charge storage portion provided between the second semiconductor body and the first electrode layer.

15

[Claim 2]

The device according to claim 1, wherein
the first electrode layer is a first word line,
the second electrode layer is a first selection gate layer, and
20 the third electrode layer is a second selection gate layer.

[Claim 3]

The device according to claim 2, wherein
the first word line is a first dummy word line.

25

[Claim 4]

The device according to claim 1, wherein
the first and second interconnections are provided in the stacked body, and
30 the first and second interconnections are provided below the second insulating layer.

[Claim 5]

The device according to claim 4, further comprising a third column-shaped portion extending in the stacked body in the stacking direction, wherein

5 the second insulating layer extends in the third column-shaped portion in the stacking direction,

the third column-shaped portion has the same structure as one of the plurality of first memory columns, and

the first and second interconnections are provided along the third column-shaped portion.

10

[Claim 6]

The device according to claim 1, further comprising:

15 a second staircase portion provided in a second end region of the stacked body located on a side opposite to the first end region between the at least two first insulating layers.

[Claim 7]

The device according to claim 6, wherein

20 the plurality of first memory columns are provided in an intermediate region of the stacked body located between the first end region and the second end region, and

the plurality of second memory columns are provided in the intermediate region of the stacked body.

25 [Claim 8]

The device according to claim 6, wherein

the first and second interconnections are provided outside the stacked body, and

30 the first and second interconnections are provided above at least one of the first end region and the second end region.