Flash Memory Process with High Voltage LDMOS Embedded

ABSTRACT OF THE DISCLOSURE

A method of embedding the forming of peripheral devices such as HV-LDMOS into the forming of flash memory is presented. A layered structure is formed with a first insulating layer formed on a substrate, and a poly silicon formed on the first insulating layer in the flash memory region. A mask layer is formed. Openings are formed in the flash memory region in the peripheral region. A local oxidation of silicon (LOCOS) is performed to form thick oxides on poly silicon, and a field oxide on silicon substrate respectively. The mask layer is removed. A control gate and a control gate oxide are formed on the thick oxide and the poly silicon. A gate electrode is formed with at least one end residing on a field oxide so that the resulting HV-LDMOS has a high breakdown voltage. Spacers and a source/drain of the flash cells and HV-LDMOSs are then formed.

Figure 11A