

ABSTRACT OF THE DISCLOSURE

BOND PAD FOR MULTI-CONDUCTOR LAYER SEMICONDUCTOR I/C CHIP

A semiconductor integrated circuit device chip has multiple interconnected conductive layers separated by insulating layers. The chip is fabricated by successive layering of conductive layers onto the surfaces of insulating layers. Upon the surface of the uppermost conductive layer of the chip is formed a passivation layer. Windows are etched through the passivation layer to form bond pads on the exposed surfaces of the uppermost conductive layer. Beneath the bond pads reside flat portions of underlying insulating and conductive layers. The flat portion of an underlying conductive layer serves as a buffering element to dissipate and deflect mechanical stresses which might otherwise cause cracking and delamination within the chip when a bond wire is bonded onto the bond pad.

(Fig. 5A)