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COMPLETE SPECIFICATION.

Semiconductor Devices and Method of Fabricating Same.

We, TEXAS INSTRUMENTS INCORPORATED of 6000 Lemmon Avenue, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices. More particularly, this invention relates to a method of fabricating high-current transistors.

The requirement of high-current carrying capability in power transistors has led to increased experimentation and research in the semiconductor fabrication field in an effort to develop devices which can carry high currents and which display improved emitter injection efficiency and lower collector saturation resistance. Recent investigations have demonstrated that the electronic characteristics of semiconductor devices are very strongly dependent upon conditions existing at the surface of the semiconductor material. In junction devices, the protection of the exposed portion of the rectifying barrier where it intersects the surface of the wafer is especially important.

It is now understood that the base-emitter junction at its intersection with the wafer surface is rather critically related to the performance of a transistor device, and particularly to the current-carrying and internal-power dissipation characteristics displayed by such devices. Thus, the current-carrying capacity of a transistor is related to the length of this junction at its intersection with the surface in that the junction length effects the injection of minority carriers from the emitter into the base region.

[*Price* 4*s.* 6*d.*]

The present invention is a semiconductor device comprising a semiconductor wafer having a diffused zone of conductivity type opposite to that of the semiconductor material adjacent it with the P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, said wafer further having a plurality of diffused elongated portions on said one major wafer face within said enclosed area, each elongated portion having a conductivity type opposite to that of the semiconductor material immediately underlying it with the P—N junction therebetween terminating at said one major wafer face, and conductive material ohmically interconnecting said elongated portions.

The present invention is also a transistor comprising a semiconductor wafer having a diffused collector zone and a base zone of opposite conductivity types with the collector-base P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, the emitter of said transistor including a plurality of diffused elongated portions of said wafer on said one major wafer face within said enclosed area and each having a conductivity type opposite to that of said base zone, conductive material ohmically interconnecting said elongated portions and ohmic contacts connected to said collector and base zones.

The present invention is also a method of fabricating a semiconductor device, comprising the steps of forming two zones of opposite conductivity types in a semiconductor wafer with the P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, including the step of diffusing a conductivity type determining impurity into said wafer, forming, in said wafer, a plurality of elongated portions

on said one major wafer face within said enclosed area, each elongated portion having a conductivity type opposite to that of the semiconductor material immediately underlying it with the P—N junction therebetween terminating at said one major wafer face, including the step of masking said one major wafer face to expose elongated areas thereon and diffusing a conductivity type determining impurity into the exposed areas to form said elongated portions, applying conductive material on said one major wafer face ohmically interconnecting said elongated portions, applying conductive material on said one major wafer face in ohmic contact with the semiconductor material immediately underlying said elongated portions and applying an ohmic contact to the semiconductor material outside said enclosed area.

The present invention is also a method of fabricating a semiconductor device, comprising the steps of diffusing an opposite conductivity type determining impurity into all the surfaces of an extrinsic semiconductor wafer to form a P—N junction, lapping one surface of said wafer to remove the diffused region adjacent said one surface whereby said P—N junction terminates at said one surface and there defines an enclosed area, masking said wafer to expose ane area on said one surface within said enclosed area, diffusing an opposite type conductivity determining impurity into said area and applying an ohmic contact on said area and an ohmic contact on said enclosed area outside said area.

The method of the present invention may result in the fabrication of a high-current transistor having a diffused collector region and a diffused emitter region. By the selection of an appropriate geometrical configuration for the emitter, a long base-emitter junction can be obtained from a relatively small emitter area. As hereinbefore explained, the long base-emitter junction imparts to the transistor a greater current-carrying capacity, and the base-emitter junction capacity is low because of the small emitter area. The small emitter area also allows a device of small physical size to be constructed.

An embodiment of the invention will now be described by way of example, with reference to the accompanying drawings, in which:—

Figs. 1*a*, 1*b*, and 1*c* depict in sequence a flow or operational diagram illustrating a method according to the invention of fabricating a high current transistor;

Figure 2 is a view, in transverse, horizontal section, of a semiconductor wafer as it appears at step 3 of the fabrication process following the initial lapping, polishing, and the diffusion of conductivity-determining impurities into all the surfaces of the wafer;

Figure 3 is a transverse, vertical sectional view through the centre of the wafer after one surface has been lapped away to expose the base region of the semiconductor wafer;

Figure 4 is a sectional view similar to Figure 3 illustrating the appearance of the wafer following steam treatment to form an oxide film on each of its surfaces;

Figure 5 illustrates a mask or stencil which is to be employed in conjunction with a photosensitive material to provide for selective removal of the oxide film according to a predetermined pattern;

Figure 6 is a top perspective view of the wafer shown in Figure 4 with the photosensitive resist material applied to the upper surface thereof and the mask or stencil depicted in Figure 5 superimposed over the photosensitive resist;

Figure 7 is a view in section of the wafer depicted in Figure 6 taken along line 7—7;

Figure 8 is a top perspective view illustrating the appearance of the upper surface of the wafer following the removal of the unexposed portion of the resist and the underlying oxide film;

Figure 9 is a top perspective view illustrating the wafer as it appears following the diffusion of appropriate conductivity-determining impurities into the exposed base region and the subsequent removal of the developed portion of the resist and the oxide film from the upper surface of the wafer;

Figure 10 is a section through the wafer depicted in Figure 9 taken along line 10—10;

Figure 11 is a plan view of a mask or stencil employed in conjunction with a photosensitive resist to form protective bands of resist over the base-emitter and base-collector junctions;

Figure 12 is a transverse, vertical section taken through the centre of a wafer which has been coated with a photosensitive material and having the stencil of Figure 11 overlying the photosensitive material;

Figure 13 is a top perspective view of the wafer as it appears following the formation of the protective band of developed photosensitive resist over the base-emitter and base-collector junctions;

Figure 14 is a view similar to Figure 13 illustrating the appearance of the wafer after a coating of nickel has been formed upon the wafer;

Figure 15 is a view in transverse, vertical section of the wafer depicted in Figure 14 taken along lines 15—15; and

Figure 16 is a view in elevation of a semiconductor element according to the present invention mounted upon a header by the use of a sandwich-type bond.

Referring now to the figures, the steps of the fabrication process of the present invention are graphically illustrated in the

flow or operational diagram of Figure 1. In describing the method of this invention, reference will be made to the several figures following Figure 1 in conjunction with the appropriate step of the process as it is set forth sequentially in Figure 1.

At the outset of the process, a silicon block or wafer is lapped on both sides until a wafer of approximately 12 mils thickness remains. The silicon may be of either N- or P-type, but for purposes of describing the invention, it will be assumed that the method is being carried out using silicon of P-type conductivity. The resistivity of the silicon wafer is chosen to provide a desired base resistivity.

After the wafer has been reduced by lapping to a thickness of approximately 12 mils, either the lower surface or both the upper and lower surfaces of the wafer are optically polished. The collector region of the semiconductor device to be fabricated is then formed by the diffusion of N-type impurities into the silicon wafer at each of its surfaces. The diffusion is controlled so that the conductivity-determining impurities reach a depth of about 2 to 4 mils in the silicon body. At this point in the process, the semiconductor wafer appears as it is shown in Figure 2. There, the P-type silicon which is to form the base region of the final semiconductor device is depicted at 1. The collector region formed by diffusion of N-type impurities into the silicon is depicted at 2 in the form of a diffused surface layer which completely surrounds the remaining P-type material.

Following the formation of the collector region, the upper surface of the wafer is again lapped, thereby reducing the thickness of the wafer to the extent that approximately 1 mil of P-type silicon remains between the upper surface of the wafer and the P—N diffused junction formed between the base and collector regions. A view in section of the wafer, as it appears following this lapping step, is depicted in Figure 3.

At this stage of the process, the collector and base regions of the semi conductor device have been formed in substantially the arrangement which will assume in the final device. The exposed portion of the base-collector junction is in the upper surface, rather than the side of the wafer. The next steps of the process are therefore directed to the location and formation of the multi-armed emitter region of the semi-conductor device. First, the side of the wafer which was lapped in step 4 of the process, as diagrammed in Figure 1, is polished to optical smoothness. Extreme care should be exercised in all phases of the polishing and lapping to avoid scratching the surface.

After the polishing has been completed, an oxide film is formed on all surfaces of the wafer by subjecting the wafer to a steam treatment. As will be appreciated by those skilled in the art, the SiO_2 layer produced by heating silicon in an oxidizing atmosphere will mask the wafer against many of the commonly-used diffusants, including the phosphorous used in the specific example of the present process.

When the wafer has been subjected to the steam treatment to form the oxide film on all its surfaces, it appears in cross section, as shown in Figure 4. In this figure, the base region is again designated by the numeral 1, the diffused collector region is shown at 2, and the oxide film is depicted at 3.

The oxidized wafer is next coated on its upper surface with a thin uniform coating of photosensitive material, such as Kodak (Registered Trade Mark) Photographic Resist (KPR) manufactured by Eastman Kodak Company. After coating the surface with the resist and allowing it to dry, a mask or stencil, as shown in Figure 5, is applied to the upper surface of the semiconductor wafer over the resist. In the preferred embodiment of the invention being described for purposes of illustration, stencil 4 carries in a centrally located position an opaque "E"-shaped indicia 5. The remaining portion of the mask 4 is a clear, transparent material 6. When the resist and stencil have been superimposed upon the wafer, the assembly appears as shown in Figure 6 where the thin uniform coating of resist is designated by the numeral 7. It will be perceived that the darkly coloured "E"-shaped indicia 5 is located on the upper surface of the wafer and overlies, and is centrally disposed upon the base region of the wafer. This may perhaps best be observed by reference to Figure 7 which is a view in section through the wafer depicted in Figure 6 taken along the line 7—7. The section line has been taken through the centre arm of the "E"-shaped indicia so that the relative location of the "E"-shaped indicia 5 to the base region 1 may be clearly seen.

The upper surface of the stencil is now subjected to appropriate lighting so that the photographic resist is exposed throughout, except for that portion which underlies the dark "E" of the mask or stencil. Care should be exercised, if Eastman (Registered Trade Mark) KPR resist is employed, to avoid pre-exposing the layer of resist to daylight, since this material is highly sensitive to ultraviolet radiation.

After exposing the resist, the undeveloped resist is removed by dissolving it in a appropriate solvent which does not attack or dissolve the exposed portion of the resist. In the case of KPR, a solvent called KPR developer which is supplied by the Eastman Kodak Company may be used. In this manner, when the wafer is subjected to

washing with the selective solvent described, the unexposed "E"-shaped portion of the resist is removed in solution while the exposed resist which surrounds the "E" or the top surface of the wafer remains as a thin protective coating.

The effect of the masking technique thus far is to leave exposed an "E"-shaped area of the oxide film overlying the upper surface of the wafer while masking the remaining portion of said film on that surface. With the wafer in this condition, a dilute hydrofluoric acid etch is applied to the upper surface of the wafer, and the exposed oxide film is dissolved therein. The wafer then appears as shown in Figure 8. After rinsing away the residual etchant, the exposed portion of the KPR is removed by dissolving it in methylene chloride or other appropriate solvent (Step 12 in Figure 1).

The wafer is now ready for the formation of the emitter region by diffusion of appropriate impurities into the upper surface of the base region. The condition of the upper surface of the wafer is such that all of the surface is protected, against penetration of the diffusant by the thin oxide film which covers it, except for the "E"-shaped portion of the base region, which is exposed. Since the silicon forming the base region is of P-type conductivity, the conductivity-determining impurity which is selected for diffusion into the base region to form the emitter must be of N-type material, and must be a diffusant which will not penerate the oxide film. Phosphorus has been found to be an especially appropriate material for this purpose. In this preferred example, the emitter is formed by diffusing phosphorus from a phosphorous pentoxide source into the exposed base region at a temperature of approximately 1200° C. for a sufficient time to permit its penetration to a depth of approximately 0.1 mil. The wafer is then subjected to an appropriate clean-up treatment to remove the oxide film from all surfaces. Following the clean-up, the wafer appears as shown in Figure 9 wherein the base, collector and emitter regions are depicted at 1, 2, and 8, respectively. A section through the wafer of Figure 9, taken along the line 10—10, is shown in Figure 10.

In order to enhance the P-conductivity of the base region and improve the ohmic contact which is subsequently to be bonded thereon, a follow-up diffusion of P-type gallium into the entire base-emitter surface of the wafer is then carried out. The diffusion of the gallium is carried out at 1200° C. and during this step, the phosphorus which was diffused into the base to form the emitter region is diffused an additional 0.2 mil to 0.3 mil into the silicon wafer. The concentration of gallium in the emitter region is not sufficient to alter its N-type conductivity attributable to the diffused phosphorus.

The next steps of the process commencing with step 16, depicted in Figure 1, are directed to the preparation of the wafer for the selective application of a thin coating of nickel. Although considerably more difficulty is generally experienced in plating upon silicon than upon germanium, a coating of nickel may be applied to the surface of the silicon by the employment of known electroless plating process which forms a very adherent and uniform plating over the entire surface reached by the electroless solution. The electroless technique is particularly well suited for plating semiconductor surfaces for the purpose of obtaining electrical contact thereto.

Prior to the application of the nickel coating, however, it is necessary to provide some means for protecting the junctions of the semiconductor device to prevent short-circuiting by the nickel plating. This is accomplished by a masking technique similar to that employed in forming the emitter region.

Initially, the wafer is again coated with KPR. After the KPR has been applied to the entire surface of the element and allowed to dry, a junction line mask or stencil of the type depicted in Figure 11 is placed over the lacquer. By reference to Figure 11, it will be perceived that the junction line stencil consists of an opaque sheet 10 having a centrally located band 10a of clear transparent material. The band 10a forms the outline of a block "E" and conforms to the junction betwen "E"-shaped emitter region 8 and the base region 1. This band is approximately 5 mils wide, and when the mask 9 is superimposed on the upper surface of the semiconductor wafer, the transparent band 10*a* overlies or straddles the base emitter junction so that it extends a distance of approximately 2.5 mils on either side of the junction. This relationship is illustrated in Figure 12.

The mask 9 includes a second band 10*b* of clear transparent material. The band 10*b* is square in shape and conforms to the junction between the base region 1 and the collector region 2. Band 10*b* is approximately 15 mils wide, and when the mask 9 is superimposed upon the upper surface of the semiconductor wafer, the band 10*b* overlies or straddles the base-collector junction, as shown in Figure 12. The band 10*b* is considerably wider than the band 10*a*. This is desirable, as the base-collector junction is not so precisely located on the surface of the wafer as the base-emitter junction.

With the KPR coating 23 applied and the junction line mask in place (see Fig. 12), the KPR is again exposed in a manner similar to that used in forming the emitter region

in Step 9 of Figure 1a. Since the small narrow bands 10*a* and 10*b* are the only portions of the mask or stencil which are transparent, the portion of the KPR which underlies these bands will be the only portion of the KPR which is exposed. The unexposed portion of the KPR is removed in KPR developer or other appropriate solvent. The wafer now appears, as shown in Figure 13, where the narrow band of developed KPR 11 is shown overlying the junction between the base 1 and emitter region 8 and the band 12 of KPR overlies the base-collector junction.

Prior to the electroless application of the nickel coating to the upper surface of the wafer, it is necessary to roughen this surface to enhance the adherence of the nickel coating. To this end, the wafer is sandblasted lightly in order to roughen the surface while avoiding the removal of the KPR mask overlying the base-emitter and base-collector junctions. Following the roughening of the surface of the wafer by sandblasting, approximately 100 microinches of nickel 24 are deposited upon the wafer surface by an electroless nickel-plating technique, and the protective resist is then removed from over the junctions, where, of course, no nickel-plating is effected.

In some instances, such as when the wafers are not of uniform size or are of irregular shape, it will not be possible to mask the base-collector junction with the photoresist. In this instance, the mask 9 will not include the transparent band 10b, and the thin layer of nickel will cover the base-collector junction. It is therefore necessary to free the base-collector junction from the nickel plating 24 to prevent the short circuiting of this junction which would otherwise result. To accomplish this, all of the lower surface and upper surface except a five to ten mil wide perimeter extending around the edge of the upper surface is masked with an etch-resistant wax. From the geometry of the collector region, as it has been depicted in Figures 3, 9 and 12, it will be understood that the sides of the wafer and that part of the upper surface containing the collector region and the portion of the base region which is adjacent the base-collector junction will be free of the wax masking. A suitable etchant, such as nitric acid, may then be used to remove the thin layer of nickel from the unmasked regions, including that which overlies the base-collector junction.

After the nickel has been etched away from the unmasked regions, the element is cleaned up, utilizing a CP—4 etch. The wax mask is then removed from both surfaces using a suitable solvent, such as trichloroethylene, and the protective resist 11 is removed to expose the base-emitter junction.

As mentioned before, it is extremely difficult to produce a nickel plate which will adhere strongly to the silicon surface. In some instances, it is desirable to perform the plating operation in two steps. Thus, a thin layer of nickel is plated onto the wafer in the manner described above. The nickel-plated wafer is then placed in a furnace, and the thin layer of nickel plate is sintered into the silicon wafer. Sintering at 700° C. for one hour in a nitrogen atmosphere has provided acceptable results. The wafer is again masked with the photoresist to protect the junctions, and a second layer of nickel is applied using the electroless nickel-plating process. Contacts formed in this manner are appreciably stronger than those formed without the sintering operation.

In order to make it easire to attach leads to the surfaces of the wafer, a layer of solder is next applied to the base-emitter surface and to the collector surface. A suitable solder must readily bond to the nickel plating, its melting point must be above the maximum operating temperature of the device, and must be etch resistant. As has been previously indicated, Indalloy, the trade name of a metallic alloy of indium manufactured by the Indium Corporation of America, Utica, New York, has proved to be an excellent material for this purpose. Indalloy is first placed on the upper and lower surface of the wafer over the nickel plating, and the wafer is then placed in an inert atmosphere and heated above the melting point of the Indalloy. The liquid Indalloy will wet the neckel surfaces and leave the base-collector and base-emitter junctions free and clean.

Instead of first applying the Indalloy to the wafer and then bonding the wafer to the header, the semiconductor element may be mounted upon a header by a sandwich-type bond. The manner in which this bond is built up may best be perceived by reference to Figure 16 where the semiconductor element is shown bonded collector side down to a gold-plated header. A layer of flux 15 is first applied to the layer 14 of gold plate which covers the header 25. Then, layers of Indalloy 16, flux 17, nickel-plated molybdenum 18, flux 19, Indalloy 20, and flux 21 are positioned upon the gold-plated header 25. The nickel-plated wafer is then added to the combination with the lower surface abutting the layer 21 of flux. Layer 22 of flux and 26 of Indalloy are placed on the base-emitter surface. The entire assembly is then placed in an inert atmosphere and heated above the melting point of the Indalloy. In this manner, the bonding of the Indalloy to the upper or emitter-base surface of the wafer and the bonding of the wafer to the header are simultaneously accomplished. The liquid Indalloy will wet the nickel surfaces and leave the base-collector

and base emitter functions free and clean. Wire leads may later be cold-pressure bonded to the Indalloy emitter and base contacts.

A layer 18 of molybdenum is placed between the wafer and the header. The molybdenum has a coefficient of thermal expansion substantially equal to that of silicon, whereas the normal header materials do not. By mounting the wafer on the layer of molybdenum rather than directly to the header, it is possible to minimize the stresses induced in the wafer as the temperature of the unit is changed.

Devices fabricated by the method of the present invention hereinbefore described have exhibited certain improved characteristics not present in devices of the prior art. First, the "E"-shaped or multi-armed emitter zone provides a long, extended emitter-base junction which results in greater current-carrying capacity.

The deep diffused collector region is of very low resistivity, thus effectively reducing the collector saturation resistance. In fact, the collector saturation resistance obtained with the transistor of the present invention is sufficiently low that it approaches the value of saturation resistance obtained with alloy-type transistors.

As all of the exposed portions of both the base-collector and the base-emitter junctions are located in the relatively protected upper surface of the water, there is considerably less danger of shorting one of the junctions and the leakage current of this transistor is considerably less than that of prior art transistors, as there is less contamination of the active junctions.

The advantages accruing from the use of Indalloy to form the base, emitter and collector contacts have been previously mentioned. The primary advantage in such use of this material stems from its property of wetting or adhering to the nickel plating without adherance to the exposed junction areas of the wafer. This makes possible the formation of all contacts and the mounting of the wafer on the header simultaneously.

Although this invention has been disclosed by means of an illustrative embodiment thereof, the invention is not intended to be limited to this embodiment and modification may be made. Thus, for example, the emitter region, instead of being "E"-shaped as described, might have an asterisk or starfish-shaped configuration, resulting in a long base-emitter junction and a relatively small emitter area. Also, in those instances wherein the emitter area is not so critical, other configurations, such as a circle, could be used.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor wafer having a diffused zone of conductivity type opposite to that of the semiconductor material adjacent it with the P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, said wafer further having a plurality of diffused elongated portions on said one major wafer face within said enclosed area, each elongated portion having a conductivity type opposite to that of the semiconductor material immediately underlying it with the P—N junction therebetween terminating at said one major wafer face, and conductive material ohmically interconnecting said elongated portions.

2. A semiconductor device according to claim 1, wherein said one major wafer face is a plane surface.

3. A semiconductor device according to claim 1 or 2, wherein said elongated portions are arranged to define a multi-armed configuration.

4. A semiconductor device according to any preceding claim, including an ohmic contact secured to said one major wafer face inside said enclosed area and outside said elongated portions, said ohmic contact and said conductive material being interleaved with each other.

5. A semiconductor device according to any preceding claim, wherein said wafer is rectangular parallelepiped shaped.

6. A transistor comprising a semiconductor wafer having a diffused collector zone and a base zone of opposite conductivity types with the collector-base P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, the emitter of said transistor including a plurality of diffused elongated portions of said wafer on said one major wafer face within said enclosed area and each having a conductivity type opposite to that of said base zone, conductive material ohmically interconnecting said elongated portions, and ohmic contacts connected to said collector and base zones.

7. A transistor according to claim 6, wherein said one major wafer face is plane.

8. A method of fabricating a semiconductor device, comprising the steps of forming two zones of opposite conductivity types in a semiconductor wafer with the P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, including the step of diffusing a conductivity type determining impurity into said wafer, forming, in said wafer, a plurality of elongated portions on said one major wafer face within said enclosed area, each elongated portion having a conductivity type opposite to that of the semiconductor material immediately underlying it with the P—N junction therebetween terminating at said one major wafer face, including the

and base emitter functions free and clean. Wire leads may later be cold-pressure bonded to the Indalloy emitter and base contacts.

A layer 18 of molybdenum is placed between the wafer and the header. The molybdenum has a coefficient of thermal expansion substantially equal to that of silicon, whereas the normal header materials do not. By mounting the wafer on the layer of molybdenum rather than directly to the header, it is possible to minimize the stresses induced in the wafer as the temperature of the unit is changed.

Devices fabricated by the method of the present invention hereinbefore described have exhibited certain improved characteristics not present in devices of the prior art. First, the "E"-shaped or multi-armed emitter zone provides a long, extended emitter-base junction which results in greater current-carrying capacity.

The deep diffused collector region is of very low resistivity, thus effectively reducing the collector saturation resistance. In fact, the collector saturation resistance obtained with the transistor of the present invention is sufficiently low that it approaches the value of saturation resistance obtained with alloy-type transistors.

As all of the exposed portions of both the base-collector and the base-emitter junctions are located in the relatively protected upper surface of the water, there is considerably less danger of shorting one of the junctions and the leakage current of this transistor is considerably less than that of prior art transistors, as there is less contamination of the active junctions.

The advantages accruing from the use of Indalloy to form the base, emitter and collector contacts have been previously mentioned. The primary advantage in such use of this material stems from its property of wetting or adhering to the nickel plating without adherance to the exposed junction areas of the wafer. This makes possible the formation of all contacts and the mounting of the wafer on the header simultaneously.

Although this invention has been disclosed by means of an illustrative embodiment thereof, the invention is not intended to be limited to this embodiment and modification may be made. Thus, for example, the emitter region, instead of being "E"-shaped as described, might have an asterisk or starfish-shaped configuration, resulting in a long base-emitter junction and a relatively small emitter area. Also, in those instances wherein the emitter area is not so critical, other configurations, such as a circle, could be used.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor wafer having a diffused zone of conductivity type opposite to that of the semiconductor material adjacent it with the P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, said wafer further having a plurality of diffused elongated portions on said one major wafer face within said enclosed area, each elongated portion having a conductivity type opposite to that of the semiconductor material immediately underlying it with the P—N junction therebetween terminating at said one major wafer face, and conductive material ohmically interconnecting said elongated portions.

2. A semiconductor device according to claim 1, wherein said one major wafer face is a plane surface.

3. A semiconductor device according to claim 1 or 2, wherein said elongated portions are arranged to define a multi-armed configuration.

4. A semiconductor device according to any preceding claim, including an ohmic contact secured to said one major wafer face inside said enclosed area and outside said elongated portions, said ohmic contact and said conductive material being interleaved with each other.

5. A semiconductor device according to any preceding claim, wherein said wafer is rectangular parallelepiped shaped.

6. A transistor comprising a semiconductor wafer having a diffused collector zone and a base zone of opposite conductivity types with the collector-base P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, the emitter of said transistor including a plurality of diffused elongated portions of said wafer on said one major wafer face within said enclosed area and each having a conductivity type opposite to that of said base zone, conductive material ohmically interconnecting said elongated portions, and ohmic contacts connected to said collector and base zones.

7. A transistor according to claim 6, wherein said one major wafer face is plane.

8. A method of fabricating a semiconductor device, comprising the steps of forming two zones of opposite conductivity types in a semiconductor wafer with the P—N junction therebetween terminating at one major wafer face and there defining an enclosed area, including the step of diffusing a conductivity type determining impurity into said wafer, forming, in said wafer, a plurality of elongated portions on said one major wafer face within said enclosed area, each elongated portion having a conductivity type opposite to that of the semiconductor material immediately underlying it with the P—N junction therebetween terminating at said one major wafer face, including the

step of masking said one major wafer face to expose elongated areas thereon and diffusing a conductivity type determining impurity into the exposed areas to form said elongated portions, applying conductive material on said one major wafer face, ohmically interconnecting said elongated portions, applying conductive material on said one major wafer face in ohmic contact with the semiconductor material immediately underlying said elongated portions and applying an ohmic contact to the semiconductor material outside said enclosed area.

9. A method according to claim 8, wherein the conductive material ohmically interconnecting said elongated portions and the conductive material ohmically connected to the semiconductor material immediately underlying the elongated portions are the same material.

10. A method according to claim 9, wherein the conductive material is nickel.

11. A method according to claim 8 or 9, wherein an impurity is diffused into said enclosed area prior to the application of said conductive material which impurity is insufficient to alter the conductivity types of each elongated portion and the semiconductor material immediately underlying it.

12. A method according to any of claims 8 to 11, wherein the step of applying the conductive material interconnecting the elongated portions and the step of applying the conductive material in ohmic contact with the semiconductor material immediately underlying said elongated portions includes the step of masking said one surface whereby the P—N junctions are covered and only the contact areas are exposed.

13. A method according to any of claims 8 to 11, wherein the step of applying conductive material in ohmic contact with the semiconductor material immediately underlying said elongated portions includes applying the conductive material on the P—N junction defining said enclosed area and thereafter removing such conductive material.

14. A method according to any of claims 8 to 13, including the step of applying a solder to the conductive material interconnecting said elongated portions and the conductive material in ohmic contact with the semiconductor material immediately underlying said elongated portions and there after attaching leads thereto.

15. A method of fabricating a semiconductor device comprising the steps of diffusing an opposite conductivity type determining impurity into all the surfaces of an extrinsic semiconductor wafer to form a P—N junction, lapping one surface of said wafer to remove the diffused region adjacent said one surface whereby said P—N junction terminates at said one surface and there defines an enclosed area, masking said wafer to expose an area on said one surface within said enclosed area, diffusing an opposite type conductivity determining impurity into said area and applying an ohmic contact on said area and an ohmic contact on said enclosed area outside said area.

16. A method according to claim 15, wherein said wafer is silicon and wherein said step of masking comprises oxidizing at least the lapped surface of said wafer to form silicon oxide thereon, applying photosensitive material over said lapped surface, superimposing upon said photosensitive material a stencil bearing a centrally located, opaque indicia, developing portions of said photosensitive material by exposing it to light through said stencil, dissolving the undeveloped portion of said photosensitive material to expose an area of said silicon oxide on said lapped surface, and dissolving the silicon oxide from said area to expose the area on said one surface.

17. A method according to claim 16, wherein said silicon oxide is removed from at least said one surface prior to said step of applying the ohmic contacts.

18. A method according to claim 16 or 17, wherein said area on said one surface is multi-armed in configuration.

19. A semiconductor device when produced by the method of any of claims 8 to 18.

20. A semiconductor device substantially as described herein with reference to the accompanying drawings.

21. A method of fabricating a semiconductor device substantially as described herein with reference to the accompanying drawings.

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