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TITLE OF THE INVENTION

A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a technique for manufacturing semiconductor devices and, more particularly, to a technique which is effectively applied to the technique of manufacturing semiconductor devices each constituted in such a manner that electrode pads are relocated in the state of semiconductor wafer and the bump electrodes are formed on the relocated electrode pads.

2. Description of the Related Art:

A semiconductor device incorporated into a small-sized electronic appliance such as a portable telephone, a portable type information processing terminal equipment, a portable type personal computer or the like is required to be made thin, miniaturized and multi-pinned. Thus, as a semiconductor device suited to such a demand, a semiconductor device called CSP (Chip Size Package) type has been developed. Concerning this CSP type semiconductor device, semiconductor devices of various structures have been proposed and commercialized; and, recently, as disclosed in *Nikkei Microdevices* (August issue, 1998, pp. 44 to 71) published by Nikkei Business

Publications, Inc., the new CSP type semiconductor device (hereinafter referred to as wafer-level CSP type semiconductor device) manufactured by a manufacturing technique according to which the wafer process (preliminary process) and the package process (post process) are integrally put together has been developed. In this wafer-level CSP type semiconductor device, the plane size of the package is approximately the same as the plane size of the semiconductor chip, so that this wafer-level CSP type semiconductor device can be more miniaturized and lowered in costs as compared with the CSP type semiconductor device (hereinafter referred to as chip-level CSP type semiconductor device) manufactured in such a manner that the semiconductor chip split from a semiconductor wafer is each subjected to package process.

The wafer-level CSP type semiconductor device is of a constitution comprising mainly a semiconductor chip on which a circuit is formed, a layer for relocating pad arrangement which layer is formed on a circuit forming surface being the front surface of the front and rear surfaces (one major surface and the other major surface which are opposed to each other) of this semiconductor chip, and bump electrodes disposed as external connection terminals on this pad arrangement relocating layer. The semiconductor chip comprises mainly a semiconductor

substrate, a multilayer wiring layer formed by stacking a plurality of insulating layers and wiring layers on the circuit forming surface being the front surface (one major surface) of the front and rear surfaces (one major surface and the other major surface which are opposed to each other), and a surface protection film formed so as to cover this multilayer wiring layer. On the uppermost wiring layer of the multilayer wiring layer, electrode pads are formed, and, in the surface protection film, bonding holes which expose the electrode pads are formed. The pad arrangement relocating layer is a layer for forming electrode pads which have an arranging pitch wider with respect to the electrode pads of the semiconductor chip. The electrode pads on the pad arrangement relocating layer are electrically connected to the corresponding electrode pads of the semiconductor chip and arranged at the same arranging pitch as the arranging pitch of the electrode pads of the printed circuit board on which the semiconductor device is mounted. The bump electrodes are formed on the electrode pads of the relocating layer and electrically and mechanically connected to them.

SUMMARY OF THE INVENTION

The present inventor found the following problematic points prior to the development of the wafer-level CSP type

semiconductor device:

(1) The wafer-level CSP type semiconductor device is mounted in the state in which the bump electrodes are opposed to the mounting surface of a printed circuit board. Therefore, in the wafer-level CSP type semiconductor device, it is necessary to form identifying marks such as the product name, the company name, the kind of the product, the manufacture lot number, etc. The formation of the identifying marks should desirably be carried out before dividing the semiconductor wafer into the respective chip forming regions, in other words, in the state of semiconductor wafer. The reason therefor is that, after the semiconductor wafer is divided into the respective chip forming regions, the treating units are increased to several hundreds of times as much as those of the wafer state, so that the treatment becomes troublesome, thus affecting the quality and the costs.

The formation of the identifying marks in the wafer state can be executed by forming the respective identifying marks in the regions on the rear surface side (the other major surface side) of the semiconductor wafer which regions correspond to a plurality of chip forming regions formed on the circuit forming surface being the front surface (one major surface) of the front and rear surfaces (one major surface and the other major surface which are

opposed to each other) of the semiconductor wafer.

However, the formation of the identifying marks in the wafer state is performed by vacuum-fixing the semiconductor wafer to the vacuum chuck stage of the marking apparatus, so that, in the case the identifying marks are formed after the formation of the bump electrodes, the bump electrodes are apt to be deformed; and thus, it becomes a cause for lowering the yield of the wafer-level CSP type semiconductor devices. Further, due to the projections and depressions of the bump electrodes, the rear surface of the semiconductor wafer becomes projected and depressed, so that, regardless of whether the marking apparatus is of the contact type such as a direct printing type marking apparatus etc. or of the non-contact type such as an ink jet type marking apparatus etc., defective identifying marks are produced; and thus, the yield of the wafer-level CSP type semiconductor devices is lowered.

(2) The semiconductor wafers tend to be increased in diameter in order to enhance the chip obtaining rate, but, as a result of this, the semiconductor wafers become liable to warp, so that, as the diameter thereof is made larger, the thickness of the semiconductor wafers increases, too. On the other hand, the semiconductor device which is incorporated into a small-sized electronic appliance such as a portable telephone, a portable information processing

terminal equipment, a portable type personal computer or the like is required to be made thinner. Thus, a back grind treatment for grinding the rear surface of the semiconductor wafer for reducing the thickness thereof needs to be performed after the semiconductor wafer is subjected to a wafer preliminary step treatment.

However, since the back grind treatment is carried out by vacuum-fixing the semiconductor wafer to the vacuum chuck stage of the grinding apparatus, so that, in the case the back grind treatment is carried out after the bump electrodes are formed, the thickness of the semiconductor wafer becomes uneven due to the influence by the projections and depressions of the bump electrodes. In the case the thickness of the semiconductor wafer becomes uneven, cracks are apt to be caused in the semiconductor wafer in the dicing step for dividing the semiconductor wafer into the respective chip forming regions, whereby the yield of the wafer-level CSP type semiconductor devices is lowered.

(3) In the case the back grind treatment is carried out after the identifying marks are formed on the rear surface side of the semiconductor wafer, the stress produced concentrates on the projections and depressions of the identifying marks, and thus, cracks are apt to be caused in the semiconductor wafer, so that the yield of

the wafer-level CSP type semiconductor devices is lowered.

(4) It is pointed out that, in a semiconductor device in which a memory circuit such as, e.g., a DRAM (Dynamic Random Access Memory), an SRAM (Static Random Access Memory) and the like are incorporated as the circuit, partial products (partially non-defective memories) are picked out to utilize them, but, in the case of utilizing them, it is necessary to record a large amount of information in order to transmit the mat-wise information (the partial state: Bank partial, address partial, I/O partial) on good or bad (non-defective or defective) of the memory circuit. In the case of the so far known method of recording information in a semiconductor chip, the amount of information is limited, so that the method of recording the information by dividing the trays in accordance with the order in which the semiconductor chips are placed side by side in the trays or in accordance with the respective kinds is considered.

However, managing the characteristic information in accordance with the order in which the semiconductor chips are placed side by side in a tray results in the transmission of wrong information in the case the order on the tray changes unintentionally, thus leading to manufacturing problems such as the fall in the yield and the like. Preparing trays in the number corresponding to

the kinds of partial turns out not to be practical if the number of the kinds of products is taken into consideration, and in addition, when they are separated from the trays, the information is likewise lost. Further, in the information recording performed in a chip-level CSP type semiconductor device, only the manufacturing information of the semiconductor chips is contained, and no information pertaining to utilization of the partial products is contained; and in addition, the information which can be physically recorded is limited.

It is an object of the present invention to provide a technique which can enhance the yield of semiconductor devices.

Another object of the present invention is to provide a technique which can stably and safely utilize the partial products.

The above-mentioned and other objects of the present invention and its novel feature will be clarified through the description in the specification and the accompanying drawings.

Of the inventions disclosed in the present application, an outline of the representative ones will be briefly explained as follows:

(1) In a method of manufacturing semiconductor devices, after the step of forming a plurality of chip

forming regions having circuit systems on the front surface of the front and rear surfaces of a semiconductor wafer, but before the step of forming bump electrodes on the respective chip forming regions, there is provided the step of forming identifying marks in the regions on the rear surface side of the semiconductor wafer which regions correspond to the respective chip forming regions.

(2) In a method of manufacturing semiconductor devices, after the step of forming a plurality of chip forming regions having circuit systems on the front surface of the front and rear surfaces of a semiconductor wafer, but before the step of forming bump electrodes on the respective chip forming regions, there is provided the step of grinding the rear surface of the semiconductor wafer.

(3) In the method of manufacturing semiconductor devices described in the means (2), after the step of grinding the rear surface of the semiconductor wafer, there is provided the step of forming identifying marks in the regions on the rear surface side of the semiconductor wafer which regions correspond to the respective chip forming regions.

(4) In a method of manufacturing semiconductor devices, after the step of forming a plurality of chip forming regions having circuits on the front surface of the front and rear surfaces of a semiconductor wafer, but

before the step of dividing the semiconductor wafer into the respective chip forming regions, there are provided the step of measuring the electric characteristics of the circuits in the respective chip forming regions and the step of forming identifying marks containing the characteristic information based on the electric characteristic results of the respective circuits obtained at the measuring step on the rear surface side of the semiconductor wafer which regions correspond to the respective chip forming regions.

According to the means (1), when the identifying marks are formed on the rear surface side of the semiconductor wafer, the bump electrodes are not formed on the front surface side of the semiconductor wafer, so that it is possible to prevent the deformation of the bump electrodes which would otherwise be caused by vacuum-fixing the semiconductor wafer to the vacuum chuck stage of the marking apparatus. Further, the defects of the identifying marks which would otherwise be caused by the projections and depressions on the rear surface of the semiconductor wafer which projections and depressions result from the projections and depressions of the bump electrodes can be prevented. As a result, the yield of semiconductor devices can be enhanced.

According to the means (2), when the rear surface of

the semiconductor wafer is ground, the bump electrodes are not formed on the front surface side of the semiconductor wafer, so that the uneven thickness of the semiconductor wafer due to the projections and depressions of the bump electrodes can be prevented. As a result, at a dicing step for dividing the semiconductor wafer into the respective chip forming regions, the occurrence of cracks in semiconductor wafer which would be caused due to uneven thickness can be prevented, so that the yield of the semiconductor devices can be enhanced.

According to the means (3), when the rear surface of the semiconductor wafer is ground, the identifying marks are not formed on the rear surface side of the semiconductor wafer, so that it is possible to prevent the occurrence of cracks in the semiconductor wafer which would be caused due to the concentration of the stress on the projections and depressions of the identifying marks. As a result, the yield of the semiconductor devices can be enhanced.

According to the means (4), it becomes possible to manage the semiconductor devices in a state accompanied with partial product information, so that the semiconductor devices can be stably and safely managed without being swayed by unstable conditions such as the intra-tray positions and the like.

Further, the semiconductor device can be freely

handled alone, so that the convenience thereof when it is used as a part to be incorporated into a memory module is enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plane view of a semiconductor device being an embodiment of the present invention;

Fig. 2 is a bottom view of the semiconductor device being the embodiment of the present invention;

Fig. 3 is a sectional view of an essential portion of the semiconductor device being is the embodiment of the present invention;

Fig. 4 is a sectional view partially enlarging a portion of Fig. 3;

Fig. 5 is a flow chart for explaining the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 6 is a plane view of the semiconductor wafer used in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 7 is a plane view of a semiconductor wafer for explaining the wafer preliminary step treatment in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 8 is a sectional view of an essential portion

of the semiconductor wafer for explaining the wafer preliminary step treatment in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 9 is a sectional view of an essential portion of the semiconductor wafer for explaining the step of forming the pad arrangement relocating layer in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 10 is a sectional view of an essential portion of the semiconductor wafer for explaining the step of forming the pad arrangement relocating layer in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 11 is a sectional view of an essential portion of the semiconductor wafer for explaining the wafer rear surface grinding step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 12 is a sectional view of an essential portion of the semiconductor wafer for explaining the mark forming layer forming step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 13 is a diagram showing an outline of the constitution of the semiconductor manufacturing apparatus

used for the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 14 is a perspective view for explaining the wafer probing test step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 15 is a bottom view of the semiconductor wafer for explaining the marking step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 16 is a plane view of the semiconductor wafer for explaining the bump electrode forming step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 17 is a sectional view of an essential portion of the semiconductor wafer for explaining the bump electrode forming step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 18 is a sectional view of an essential portion for explaining the dicing step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 19 is a sectional view of an essential portion for explaining the pickup step in the manufacture of the semiconductor device being the embodiment of the present

invention;

Fig. 20 is a sectional view of an essential portion for explaining the jig packing step in the manufacture of the semiconductor device being the embodiment of the present invention;

Fig. 21 is a flow chart for explaining the manufacture of the memory module in which the semiconductor device being the embodiment of the present invention is incorporated;

Fig. 22 is a sectional view of the memory module in which the semiconductor device being the embodiment of the present invention is incorporated; and

Fig. 23 is a diagram showing an outline of the constitution of another semiconductor manufacturing apparatus used for the manufacture of the semiconductor device being the embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The constitution of the present invention will now be described together with the mode for carrying out the invention in which the present invention is applied to a wafer-level CSP (Chip Size Package) type semiconductor device. In the drawings for describing the mode for carrying out the invention, those portions which have the same functions will be referenced by the same reference

numerals to thereby omit the repetition of the description thereof.

Fig. 1 is a plane view of the semiconductor device which is an embodiment of the present invention, Fig. 2 is a bottom view of the semiconductor device, Fig. 3 is a sectional view of an essential portion of the semiconductor device, and Fig. 4 is a sectional view partially enlarging a portion of Fig. 3.

As shown in Fig. 1 and Fig. 2, the wafer-level CSP type semiconductor device 20 of this embodiment is formed with a plane shape of square; in this embodiment, it is formed in a rectangular shape of, e.g., 5 mm × 8 mm. The semiconductor device 20 is of a constitution, as shown in Fig. 3, comprising mainly a semiconductor chip 15, a layer 16 for relocating pad arrangement 16 which layer 16 is formed on a circuit forming surface 15X which is the front surface (one major surface) of the front and rear surfaces (one major surface and the other major surface which are opposed to each other) of this semiconductor chip 15, and a plurality of bump electrodes 11 disposed as external connection terminals on this pad arrangement relocating layer 16.

The semiconductor chip 15 is formed with the same plane size as the plane size of the semiconductor device 20. The semiconductor chip 15 is of a constitution, as

shown in Fig. 3 and Fig. 4, comprising mainly a semiconductor substrate 1A, a multilayer wiring layer 2 comprised of a plurality of insulating layers and a plurality wiring layers which are respectively stacked on a circuit forming surface being the front surface of the front and rear surfaces (one major surface and the other major surface which are opposed to each other) of this semiconductor substrate 1A, and a surface protection film 3 formed so as to cover this multilayer wiring layer 2. The semiconductor substrate 1A is formed of, for example, monocrystalline silicon; the insulating layers of the multilayer wiring layer 2 are formed of, for example, silicon oxide films, while the wiring layers of the multilayer wiring layer 2 are formed of, for example, aluminum (Al) films or aluminum alloy films; and the surface protection film 3 is formed of, for example, a silicon nitride film.

In the central portion of the circuit forming surface of the semiconductor chip 15, there are formed a plurality of electrode pads 2A arranged along the long side direction of the semiconductor chip 15. A plurality of electrode pads 2A are respectively formed on the uppermost wiring layer of the multilayer wiring layer 2 in the semiconductor chip 15. The uppermost wiring layer is covered by the surface protection film 3 formed as the upper layer thereof,

and, in this surface protection film 3, there are formed openings 3A (see Fig. 4) which expose the surfaces of the electrodes pads 2A. The plane shape of each of a plurality of electrode pads 2A is made into a square shape of, for example, 25 μm × 25 μm. Further, a plurality of electrode pads 2A are respectively arranged, for example, at an arranging pitch of about 85 μm.

On the semiconductor chip 15, a DRAM (Dynamic Random Access Memory) of, for example, 64 megabits is formed as a memory circuit. The memory array of this DRAM is comprised of, for example, four banks.

The pad arrangement relocating layer 16 is of a constitution, as shown in Fig. 3 and Fig. 4, comprising mainly an insulating layer 6 formed on the surface protection film 3, a plurality of wirings 7 extending on this insulating layer 6, an insulating layer 8 formed on the insulating layer 6 so as to cover a plurality of wirings 7, and a plurality of testing electrode pads 9A and a plurality of electrode pads 9B formed as the upper layer of the insulating layer 8.

One end side of each of a plurality of wirings 7 is electrically and mechanically connected to each of a plurality of electrode pads 2A through the opening 6A formed in the insulating layer 6 and the opening 3A formed in the surface protection film 3. The other end side of

each of those wirings 7 which are approximately half in the number of a plurality of wirings 7 is led out to one long side of the two mutually opposed long sides of the semiconductor device 20, while the other end side of each of the remaining wirings 7 is led out to the other long side of the two mutually opposed long sides of the semiconductor device 20 (see Fig. 2).

A plurality of testing electrode pads 9A are each electrically and mechanically connected to one end side of each of a plurality of wirings 7 through an opening 8A (See Fig. 4) formed in the insulating layer 8. A plurality of electrode pads 9B are each electrically and mechanically connected to one end side of each of a plurality of wirings 7 through an opening 8B (see Fig. 3) formed in the insulating layer 8. These testing electrode pads 9A and these electrode pads 9B are respectively formed of one and the same layer. The testing electrode pads 9A are not formed in some cases.

To each of a plurality of electrode pads 9B, a plurality of bump electrodes 11 disposed as external connection terminals on the pad arrangement relocating layer 16 are electrically and mechanically connected. Each of a plurality of bump electrodes 11 is formed of a metal material having a composition of, for example, 63 [wt%] of lead (Pb) and 37 [wt%] of tin (Sn).

The pad arrangement relocating layer 16 is a layer for relocating the arrangement of electrode pads 9B having a large arranging pitch with respect to the electrode pads 2A of the semiconductor chip 15, and the electrode pads 9B of the pad arrangement relocating layer 16 are arranged at the same arranging pitch as the arranging pitch of the electrode pads of the printed circuit board on which the semiconductor device 20 is mounted.

Each of a plurality of electrode pads 9B is arranged, though not limited to this, in two rows at the two mutually opposed long sides of the semiconductor device 20 along the respective long sides as shown in Fig. 2. The electrode pads 9B in each row are arranged at an arranging pitch of, for example, about 0.5 mm. The plane shape of each of a plurality of electrode pads 9B is formed in a circle with a diameter of, for example, about 0.25 mm. Each of a plurality of bump electrodes 11 is formed, for example, in a ball shape and its height (the distance from the insulating layer 8 to its highest portion) is, for example, about 0.15 mm.

In Fig. 2, only 22 bump electrodes 11 are shown for easier understanding of the drawing, but, ordinarily, a DRAM of 64 megabits has 50 to 60 electrode pads 9B and bump electrodes 11.

In the pad arrangement relocating layer 16, the

insulating layer 6 and the insulating layer 8 are formed of a material having a low modulus of elasticity as compared with the silicon nitride film and the silicon oxide film, in order to alleviate the concentration on the bump electrodes 11 of the stress caused by the difference in thermal expansion with respect to the printed circuit board after the semiconductor device 20 is mounted on the printed circuit board, and the insulating layer 6 and the insulating layer 8 are formed with thicknesses larger than that of the surface protection film 3. In this embodiment, each of the insulating layer 6 and the insulating layer 8 is formed of, for example, a polyimide series resin; the insulating layer 6 is formed with a thickness of, for example, about 5 to 100 μm, while the insulating layer 8 is formed with a thickness of, for example, about 5 to 100 μm.

The wirings 7 are formed of, for example, copper (Cu) films having a high conductivity. The electrode pads 9B are formed, though not limited to this, of a laminated film formed by successively stacking, for example, a chromium (Cr) film, an alloy film comprising 72 at% of nickel [Ni] - 28 at% of copper (Cu), and a gold (Au) film, respectively, in order to secure wettability when the bump electrodes 11 are formed. The gold film diffuses into the bumps when the bump electrodes 11 are formed, and it mostly

disappears.

As shown in Fig. 3, on the rear surface 15Y of the semiconductor chip 15, a mark forming layer 10 is formed so as to cover the rear surface 15Y. This mark forming layer 10 is formed of, for example, an epoxy series thermosetting resin to which carbon has been added. The epoxy series thermosetting resin has a high adhesion to silicon, and therefore, the mark forming layer 10 can be suppressed from peeling off.

As shown in Fig. 1, on the mark forming layer 10, an identifying mark 12 and an identifying mark 13 are formed. The identifying mark 12 is comprised of a mark indicative of information common within one semiconductor wafer such as, e.g., information indicative of the product name, the company name, the kind of the product, the manufacturing lot number and the like. The identifying mark 13 is comprised of a two-dimensional code mark which allows a large amount of information to be recorded with a small area. In this identifying mark 13, there are recorded the information peculiar to the semiconductor device 20 such as, e.g., the partial product information (the partial state: Bank partial, address partial I/O partial) of the DRAM and the like. Each of these identifying marks 12, 13 is formed by the laser marking method in the marking step of the manufacturing process. The laser marking

method is a method according to which a laser beam is irradiated to the surface of the mark forming region to burn the portion irradiated with the laser beam, whereby marking is made. The laser marking method does not require a cleaning treatment before the marking and a drying treatment after the marking; and, after the marking, the disappearance phenomenon that the identifying mark disappears is hard to take place.

Next, the manufacture of the above-mentioned wafer-level CSP type semiconductor device 20 will be described by referring to Fig. 5 to Fig. 20.

Fig. 5 is a flow chart for explaining the manufacture of the semiconductor device, Fig. 6 is a plane view of the semiconductor wafer used for the manufacture of the semiconductor device, Fig. 7 and Fig. 8 are a plane view of the semiconductor wafer and a sectional view of the essential portion thereof for explaining the wafer preliminary step treatment, Fig. 9 and Fig. 10 are sectional views of essential portions of the semiconductor wafer for explaining the electrode pad arrangement relocating step, Fig. 11 is a sectional view of an essential portion of the semiconductor wafer for explaining the wafers rear surface grinding (back grind) step, Fig. 12 is a sectional view of an essential portion of the semiconductor wafer for explaining the step of forming the

mark forming layer, Fig. 13 is a diagram showing an outline of the constitution of the semiconductor manufacturing apparatus used for the manufacture of the semiconductor device, Fig. 14 is a perspective view for explaining the wafer probing test step, Fig. 15 is a bottom view of the semiconductor wafer for explaining the marking step, Fig. 16 and Fig. 17 are a plane view of the semiconductor wafer and a sectional view of an essential portion thereof for explaining the bump forming step, Fig. 18 is a sectional view of an essential portion of the semiconductor wafer for explaining the dicing step, Fig. 19 is a sectional view of an essential portion for explaining the pickup step, and Fig. 20 is a plane view of an essential portion for explaining the jig packing step.

First, as shown in Fig. 6, as the semiconductor wafer, a semiconductor wafer (semiconductor substrate) 1 having a thickness of, for example, about 725 μm and comprising monocrystalline silicon is prepared.

Next, the semiconductor wafer 1 is subjected to the wafer preliminary step treatment <A>, whereby, as shown in Fig. 7 and Fig. 8, a plurality of chip forming regions 4 having DRAMs as circuits are formed in a matrix-wise state on a circuit forming surface 1X being the front surface (one major surface) of the front and rear surfaces (one major surface and the other major surface which are opposed

to each other) of the semiconductor wafer 1. Each of a plurality of chip forming regions 4 is disposed in a state spaced apart from one another through dicing regions (scribing regions) 5 for cutting the semiconductor wafer 1. Each of a plurality of chip forming regions 4 is formed by forming mainly a semiconductor element, the multilayer wiring layer 2, the electrode pads 2A, the surface protection film 3, the openings 3A and the like on the circuit forming surface 1X of the semiconductor wafer 1.

Next, the pad arrangement relocating layer 16 is formed on the respective chip forming regions 4 <B>. Specifically speaking, first the insulating layer 6 comprising, for example, a polyimide series resin is formed on the whole surface of the surface protection film 3 by the spin coating method. The insulating layer 6 is formed with a thickness of, for example, about 5 μm. Next, the openings 6A which expose the surfaces of the electrode pads 2A are formed in the insulating layer 6. Fig. 9 shows the steps carried out so far. Next, on the whole surface of the insulating film 6 including the interiors of the openings 6A, for example a copper (Cu) film is formed as a conductive film by the low pressure CVD (Chemical Vapor Deposition) method or the sputtering method. Next, the copper film is subjected to patterning to form the wirings 7. Next, on the whole surface of the insulating layer 6

including the wirings 7, the insulating layer 8 comprising, for example, a polyimide series resin is formed by the spin coating method. The insulating layer 8 is formed with a thickness of, for example, about 5 μm. Next, the openings 8A which expose the one-end sides of the wirings 7 and the openings 8B which expose the other-end sides of the wirings 7 are formed. Next, on the whole surface of the insulating layer 8 including the interiors of the openings 8A and the interiors of the openings 8B, a chromium (Cr) film, an alloy film comprising, for example, 72 at% of nickel (Ni)- 28 at% of copper (Cu), and a gold (Au) film are successively stacked, respectively, to form a laminated film. Next, the laminated film is subjected to patterning to form the testing electrode pads 9A and the electrode pads 9B. Consequently, the pad arrangement relocating layer 16 is formed, and at the same time, the electrode pads 9B having an arranging pitch larger than the arranging pitch of the electrode pads 2A are formed. The steps which have so far been carried out are shown in Fig. 10.

Next, as shown in Fig. 11, the rear surface 1Y of the semiconductor wafer 1 is ground to decrease the thickness thereof <C>. In this embodiment, the grinding is carried out until the thickness of the semiconductor wafer 1 becomes, for example, about 400 μm.

In this step, the semiconductor wafer 1 is

vacuum-fixed to the vacuum chuck stage of the grinding apparatus in the state in which the circuit forming surface 1X side of the semiconductor wafer 1 is opposed to the vacuum chuck stage, but, since the bump electrodes (11) are not formed on the circuit forming surface 1X side of the semiconductor wafer 1, the thickness of the semiconductor wafer 1 can be prevented from becoming uneven due to the projections and depressions of the bump electrodes (11).

In this step, since the identifying marks (12, 13) are not formed on the rear surface 1Y side of the semiconductor wafer 1 when the rear surface 1Y of the semiconductor wafer 1 is ground, the occurrence of cracks in the semiconductor wafer 1 which would otherwise be caused due to the concentration of the stress on the projections and depressions of the identifying marks (12, 13) can be prevented.

Then, as shown in Fig. 12, the mark forming layer 10 is formed on the rear surface 1Y of the semiconductor wafer 1 so as to cover the rear surface 1Y thereof <D>. The mark forming layer 10 of this embodiment is formed, though not limited to this, on the rear surface 1Y of the semiconductor wafer 1 by the spin coating method using a thermosetting resin comprising an epoxy series resin to which carbon and an organic solvent have been added, and thereafter, heat

treatment is carried out to harden the thermosetting resin, whereby the mark forming layer 10 is formed.

In this step, the semiconductor wafer 1 is vacuum-fixed to the vacuum chuck stage of the film forming apparatus in the state in which the circuit forming surface 1X thereof is opposed to the vacuum chuck stage, but, on the circuit forming surface 1X side of the semiconductor wafer 1, the bump electrodes (11) are not formed, so that the mark forming layer 10 can be formed without being affected by the projections and depressions of the bump electrodes (11).

The mark forming layer 10 may also be formed in such a manner that a resin film comprising a thermosetting resin comprising an epoxy series resin to which carbon has been added is bonded under thermo-compression to the rear surface 1Y of the semiconductor wafer 1. In this case, it is also possible to form the mark forming layer 10 without being affected by the projections and depressions of the bump electrodes (11).

Next, a wafer probing test <E> and marking <F> are carried out by using a semiconductor manufacturing apparatus 30A shown in Fig. 13. The semiconductor manufacturing apparatus 30A comprises a wafer probing test portion 31, a marking portion 32, a loader portion 33, a buffer portion 34, an unloader portion 35 and the like.

The loader portion 33 feeds the semiconductor wafer 1 to the wafer probing test portion 31. The buffer portion 34 accommodates the semiconductor wafer 1 which has been treated by the wafer probing test portion 31 and, thereafter, feeds the accommodated semiconductor wafer 1 to the marking portion 32. The unloader portion 35 accommodates the semiconductor wafer 1 which has been treated by the marking portion 32. The semiconductor manufacturing apparatus 30A of this embodiment puts the marks to the rear surface side of the semiconductor wafer 1 without reversing the upper and lower sides of the semiconductor wafer 1 which has been treated by the wafer probing test portion 31.

In the wafer probing test <E>, first the semiconductor wafer 1 fed from the loader portion 33 is vacuum-fixed to a vacuum chuck stage 31A. The vacuum-fixing of the semiconductor wafer 1 is effected in the state in which the rear surface 1Y of the semiconductor wafer 1 is opposed to the vacuum chuck stage 31A. The vacuum chuck stage 31A is constituted so as to be movable in the X-Y direction (the plane direction) and the Z direction (the vertical direction). Above the vacuum chuck stage 31A, there is disposed a probe card 36 fixed to a support stand 31B.

Next, as shown in Fig. 14, the vacuum chuck stage 31A is raised to approach the semiconductor wafer 1 to the probe

card 36, and, after the positional alignment of the semiconductor wafer 1 and the probe card 36 is made, probe needles 36A of the probe card 36 are contacted with the testing electrode pads 9A in the chip forming regions 4 of the semiconductor wafer 1.

Then the electric characteristics of the circuits in the respective chip forming regions 4 are measured by a tester electrically connected to the probe needles 36A of the probe card 36, and the characteristic information based on the electric characteristic results of the respective circuits is stored in the information recording device of the tester together with the positional information on the respective chip forming regions 4. By this step, the grades pertaining to the non-defective products, the defective products, the partial products, the operating frequencies and the like are determined with respect to the respective chip forming regions 4. The semiconductor wafer 1 which has undergone the wafer probing test is accommodated in the buffer portion 34 and, thereafter, fed to the marking portion 32. In this case, simultaneously with the feed of the semiconductor wafer 1 to the marking portion 32, the characteristic information and the positional information of the respective chip forming regions 4 in the semiconductor wafer 1 are transferred to the marking portion 32.

As for the marking <F>, first the semiconductor wafer 1 fed from the buffer portion 34 is vacuum-fixed to a vacuum chuck stage 32A. The suction fixing of the semiconductor wafer 1 is effected in the state in which the circuit forming surface 1X of the semiconductor wafer 1 is opposed to the vacuum chuck stage 32A. The vacuum chuck stage 32A is constituted so as to be movable in the X-Y direction and the Z-direction similar to the above-mentioned vacuum chuck stage 31A. Underneath the vacuum chuck stage 32A, a laser oscillator 32B and a pending mirror 32D are disposed.

Next, the positional information of the respective chip forming regions 4 is converted from the positional coordinates on the circuit forming surface 1X of the semiconductor wafer 1 to the positional coordinates on the rear surface of the semiconductor wafer 1, and, in accordance with the thus converted positional information of the respective chip forming regions 4, the identifying marks 13 containing the characteristic information based on the electric characteristic results of the respective circuits obtained by the wafer probing test are formed by the laser marking method in the regions on the rear surface 1Y side of the semiconductor wafer 1 which regions correspond to the respective chip forming regions 4, as shown in Fig. 15. Further, on the rear surface 1Y side

of the semiconductor wafer 1 which corresponds to the respective chip forming regions 4, the identifying marks 12 showing information common in the one semiconductor wafer 1, such as, the product name, the company name, the kind of the product, the manufacturing lot number, are also formed by the laser marking method. The identifying mark 13 is comprised of a two-dimensional code mark which allows a large amount of information to be recorded with a small area. The formation of the identifying marks 12, 13 by the laser marking method, as shown in Fig. 13, is carried out by irradiating a laser beam 32C to the surface of the mark forming layer 10 to burn the portions irradiated with the laser beam 32C, so that the phenomenon that the identifying marks (12, 13) disappear after effecting the marking is hard to take place, but it is difficult to form the identifying marks directly on the rear surface 1Y of the semiconductor wafer 1, that is, the semiconductor substrate, by the laser marking method. The reason therefor is that the rear surface 1Y of the semiconductor wafer 1 is flawed, and therefore, cracks are apt to be caused in the semiconductor wafer 1. Accordingly, the formation of the identifying marks on the rear surface 1Y side of the semiconductor wafer 1 by the laser marking method has so far not been practiced, but, by providing the mark forming layer 10 on the rear surface side of the

semiconductor wafer 1 as in this embodiment, the identifying marks (12, 13) can be formed on the rear surface 1Y side of the semiconductor wafer 1 by the laser making method.

In this step, the semiconductor wafer 1 is vacuum-fixed to the vacuum chuck stage 32A of the marking portion (marking apparatus) 32 in the state in which the circuit forming surface 1X side is opposed to the vacuum chuck stage 32A, but, since the bump electrodes (11) are not formed on the circuit forming surface 1X side of the semiconductor wafer 1, it is possible to prevent the deformation of the bump electrodes (11) which would be caused by vacuum-fixing the semiconductor wafer 1 to the vacuum chuck stage 32A of the marking portion 32. Further, it is possible to prevent the occurrence of defective identifying marks (12, 13) which would be caused by the projections and depressions of the rear surface 1Y of the semiconductor wafer 1 which projections and depressions result from the projections and depressions of the bump electrodes (11).

In this step, the mark forming layer 10 is formed of an epoxy series thermosetting resin to which carbon has been added. In the case a laser beam is irradiated to this mark forming layer 10, the carbon in the portions irradiated with the laser beam is evaporated, leaving the

irradiated portions in a white state. Accordingly, identifying marks with a good visual recognizability can be formed.

The wafer probing test is executed in such a manner that the electric characteristics are measured by contacting the probe needles 36A with the circuit forming surface 1X side of the semiconductor wafer 1, and the marking is made onto the rear surface 1Y side of the semiconductor wafer 1, so that the order and the coordinates of the chip forming regions 4 become reverse in plus and minus, in view of the coordinate system of the same apparatus, with respect to the direction in which the semiconductor wafer 1 is turned upside down; and therefore, in the marking step, it is necessary to make the conversion thereof.

Next, as shown in Fig. 17 and Fig. 18, the bump electrodes 11 are formed on the electrode pads 9B in the respective chip forming regions 4 of the semiconductor wafer 1 <G>. The formation of the bump electrodes 11 is carried out, though not limited to this, in such a manner that, for example, a spherical solder material is fed onto the electrode pad 9B by the ball feed method, and thereafter, the spherical solder material is melted by the infrared reflow method. Further, the formation of the bump electrodes 11 may also be executed in such a manner that

a solder paste material is printed on the electrode pads 9B by the screen printing method, and then, the solder paste material is melted by the infrared reflow method.

Next, a burn-in test is executed in the wafer-level state <H>. The burn-in test is a selecting test which has the purpose of excluding the defective products at the early stage before the delivery of the products to the customers and is carried out in such a manner that the circuit operation of the respective chip forming regions 4 is executed under a severe use condition (in a loaded state) as compared with the use condition of the customers to acceleratingly produce what turn out to be defects during the use by the customers, that is, defects in a certain sense.

Next, the semiconductor wafer 1 is mounted on an adhesive layer 40A side of a dicing sheet 40. The mounting of the semiconductor wafer 1 is performed in the state in which the circuit forming surface 1X of the semiconductor wafer 1 is turned upward.

Next, by the dicing apparatus, the semiconductor wafer 1, the mark forming layer 10 and the pad arrangement relocating layer 16 are divided in accordance with the respective chip forming regions 4 <I>. As a result, the semiconductor devices 20 are mostly completed as shown in Fig. 18.

Next, as shown in Fig. 19, by push-up needles 42 of a pickup apparatus, the semiconductor devices 20 are pushed upward from beneath the dicing sheet 40, and thereafter, the semiconductor devices 20 thus pushed upward are transported by a vacuum chuck collet 43 of the pickup apparatus <J>, and the semiconductor devices 20 are accommodated in a tray 44 as shown in Fig. 20 <K>. The accommodation of the semiconductor devices 20 into the tray 44 is executed in the state in which the identifying marks (12, 13) are turned upward.

Next, the manufacture of a memory module (electronic apparatus) into which the wafer-level CSP type semiconductor device 20 is incorporated will be described by referring to Fig. 21 and Fig. 22.

Fig. 21 is a flow chart for explaining the manufacture of the memory module, and Fig. 22 is a sectional view of the memory module.

First, a plurality of semiconductor devices 20 are placed on the front surface (one major surface) side of the front and rear surfaces (one major surface and the other major surface which are opposed to each other) of a printed circuit board 51 <L>, and thereafter, heat treatment is executed to mount a plurality of semiconductor devices 20 onto the front surface side of the printed circuit board 51 <M>. Next, on the rear surface side of the printed

circuit board 51, a plurality of semiconductor devices 20 are placed <N>, and thereafter, heat treatment is executed to mount a plurality of semiconductor devices 20 on the rear surface side of the printed circuit board 51 <O>. Next, the functional test of each of a plurality of semiconductor devices 20 is executed <P>, a resin 52 is then filled between the printed circuit board 51 and a plurality of semiconductor devices 20 <Q>, and thereafter, the functional test of each of a plurality of semiconductor devices 20 is executed again <R>. As a result, the memory module 50 is mostly completed.

In this way, according to this embodiment, the following effects can be obtained:

(1) The manufacture of semiconductor devices 20 comprises, after the step of forming a plurality of chip forming regions 4 having DRAMs on a circuit forming surface 1X of a semiconductor wafer 1, but before the step of forming bump electrodes 11 on the respective chip forming regions 4, the step of forming identifying marks (12, 13) in the regions on the rear surface 1Y side of the semiconductor wafer 1 which regions correspond to the respective chip forming regions 4.

Consequently, the bump electrodes 11 are not formed on the circuit forming surface 1X side of the semiconductor wafer 1 when the identifying marks are formed on the rear

surface 1Y side of the semiconductor wafer 1; and thus, it is possible to prevent the deformation of the bump electrodes 11 which would be caused by vacuum-fixing the semiconductor wafer 1 to the vacuum chuck stage 32A of the marking portion (marking apparatus). Further, it is also possible to prevent the occurrence of defective identifying marks which would be caused by the projections and depressions of the rear surface 1Y of the semiconductor wafer 1 which projections and depressions would result from the projections and depressions of the bump electrodes 11. Consequently, the yield of the semiconductor devices 20 can be enhanced.

(2) The manufacture of semiconductor devices 20 comprises the step of grinding the rear surface 1Y of a semiconductor wafer 1, after the step of forming a plurality of chip forming regions 4 having DRAMs on a circuit forming surface 1X of the semiconductor wafer 1, but before the step of forming the bump electrodes 11 on the respective chip forming regions 4.

Consequently, when the rear surface 1Y of the semiconductor wafer 1 is ground, the bump electrodes 11 are not formed on the circuit forming surface 1X side of the semiconductor wafer 1, so that it is possible to prevent the thickness of the semiconductor wafer 1 from becoming uneven due to the projections and depressions of the bump

electrodes 11. Consequently, in the dicing step of dividing the semiconductor wafer 1 in accordance with the respective chip forming regions 4, the occurrence of cracks in the semiconductor wafer 1 which would be caused by the uneven thickness can be prevented, so that the yield of the semiconductor devices 20 can be enhanced.

(3) The manufacture of semiconductor devices 20 comprises the step of forming identifying marks in the regions of the rear surface 1Y side of a semiconductor wafer 1 which regions correspond to the respective chip forming regions 4, after the step of grinding the rear surface 1Y of the semiconductor wafer 1.

Consequently, when the rear surface 1Y of the semiconductor wafer 1 is ground, the identifying marks are not formed on the rear surface 1Y side of the semiconductor wafer 1, so that it is possible to prevent the occurrence of cracks in the semiconductor wafer 1 which would be caused by the concentration of the stress on the projections and depressions of the identifying marks. Consequently, the yield of the semiconductor devices 20 can be enhanced.

(4) In the manufacture of semiconductor devices 20, the mark forming layer 10 is formed of an epoxy series resin to which carbon has been added. Consequently, in the case a laser beam is irradiated to the mark forming layer 10, the carbon in the portions irradiated with the laser beam

is evaporated, and the irradiated portions remain white. Accordingly, identifying marks which have a good visual recognizability can be formed.

(5) The manufacture of semiconductor devices 20 comprises, after the step forming a plurality of chip forming regions 4 having DRAMs as circuits on a circuit forming surface 1X of a semiconductor wafer 1, but before the step of dividing the semiconductor wafer 1 in accordance with the respective chip forming regions 4, the step of measuring the electric characteristics of the DRAMs in the respective chip forming regions 4, and the step of forming identifying marks 13 containing the characteristic information based on the electric characteristic results of the respective DRAMs obtained at the above-mentioned measuring step on the rear surface 1Y side of the semiconductor wafer 1 which regions correspond to the respective chip forming regions 4.

Consequently, it becomes possible to manage the semiconductor devices 20 in a state accompanied with partial product information, so that the stable and safe management of the semiconductor devices 20 can be executed without being swayed by unstable conditions such as the positions in the tray.

Further, the semiconductor devices can be freely handled alone, so that the convenience in the case they

are used as parts to be incorporated into memory modules is enhanced.

(6) In the manufacture of semiconductor devices 20, the identifying mark 13 is formed of a two-dimensional code mark. Due to this, a large amount of information can be recorded in a small area, and the reading thereof by a machine can be executed fast, so that the production efficiency of the memory modules 50 is enhanced.

This embodiment has been described with reference to an example of the case where the formation of the identifying marks is carried out by the laser marking method, but the formation of the identifying marks may also be carried out by the ink marking method using a direct print marking apparatus, an ink jet type marking apparatus or the like. In this case, the formation of the identifying marks on the rear surface 1Y of the semiconductor wafer 1 can be carried out, but the mark forming layer 10 is better in the attachment of the ink, and thus, the identifying marks become hard to be erased.

Further, this embodiment has been described with reference to an example of the case where the identifying marks (12, 13) are formed on the mark forming layer 10 by the laser making method, but the identifying marks (12, 13) may also be formed, without providing the mark forming layer 10, directly on the rear surface 1Y of the

semiconductor wafer 1 by the laser marking method. In this case, the marking is carried out with such a mark depth (the depth of the silicon to be burnt) that no crack is caused in the semiconductor wafer 1; for example, with a small mark depth of, for example, about 2 to 3 μm.

Further, this embodiment has been described with reference to an example of the case where the identifying marks (12, 13) are formed on the mark forming layer 10 by the laser marking method, but the identifying marks (12, 13) may also be formed directly on the rear surface 1Y of the semiconductor wafer 1 without providing the mark forming layer 10.

Further, this embodiment has been described with reference to the burn-in test in the state of wafer level, but the burn-in test may also be executed after the dicing step, that is, after the semiconductor wafer 1 is divided into the individual semiconductor devices 20.

Further, this embodiment has been described with reference to an example of the case where the semiconductor manufacturing apparatus 30A is used which performs marking without reversing the upper and lower sides of the semiconductor wafer 1, but, as shown in Fig. 23, a semiconductor manufacturing apparatus 30B may also be used, which is provided with a wafer inversion mechanism portion 37 between the wafer probing test portion 31 and the marking

portion 32. The wafer inversion mechanism portion 37 feeds the semiconductor wafer 1 to the marking portion 32 after inverting the upper and lower sides of the semiconductor wafer 1.

Further, this embodiment has been described with reference to an example of the case where the electric characteristics of the circuits in the respective chip forming regions 4 are measured by a tester, and, after the characteristic information based on the electric characteristic results of the respective circuits is stored in the information recording device of the tester together with the positional information of the respective chip forming regions 4, the positional information of the respective chip forming regions 4 is converted from the positional coordinates in the circuit forming surface 1X of the semiconductor wafer 1 into the positional coordinates on the rear surface 1Y of the semiconductor wafer 1, but the positional information of the respective chip forming regions 4 may also be stored in the information recording device of the tester after the positional information is converted from the positional coordinates on the circuit forming surface 1X of the semiconductor wafer 1 to the positional coordinates on the rear surface 1Y of the semiconductor wafer 1.

The invention achieved by the present inventor has

been concretely described hereinabove based on the foregoing embodiment, but it is a matter of course that the present invention is not limited to the above-mentioned embodiment and can be variously modified without deviating from the gist thereof.

For example, the present invention can be applied to an electronic apparatus in which a semiconductor chip (bare chip) is mounted in a bare state on a printed circuit board.

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What is claimed is:

1. A method of manufacturing a semiconductor device, comprising, after the step of forming a plurality of chip forming regions having circuits on the front surface of a semiconductor wafer, and before the step of forming bump electrodes on said respective chip forming regions, the step of forming identifying marks in the regions on the rear surface side of said semiconductor wafer which regions correspond to said respective chip forming regions.

2. A method of manufacturing a semiconductor device, comprising, after the step of forming a plurality of chip forming regions having circuits on the front surface of a semiconductor wafer, and before the step of dividing said semiconductor wafer into said respective chip forming regions, the step of relocating electrode pads in said respective chip forming regions, and the step of forming bump electrodes on said relocated electrode pads,

and further comprising the step of forming identifying marks respectively in the regions on the rear surface side of said semiconductor wafer which regions correspond to said respective chip forming regions, after the step of relocating said electrode pads, and before the step of forming said bump electrodes.

3. The method of manufacturing a semiconductor device according to Claim 1, wherein said identifying marks are

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formed on the rear surface of said semiconductor wafer by the laser marking method or the ink marking method.

4. The method of manufacturing a semiconductor device according to Claim 1, wherein said identifying marks are formed by the laser marking method or the ink marking method on a mark forming layer formed on the rear surface of said semiconductor wafer.

5. The method of manufacturing a semiconductor device according to Claim 4, wherein said mark forming layer is comprised of an epoxy series resin to which carbon has been added.

6. A method of manufacturing a semiconductor device, comprising the step of grinding the rear surface of a semiconductor wafer, after the step of forming a plurality of chip forming regions having circuits on the front surface of said semiconductor wafer, and before the step of forming bump electrodes on said respective chip forming regions.

7. A method of manufacturing a semiconductor device, comprising, after the step of forming a plurality of chip forming regions having circuits on the front surface of a semiconductor wafer, and before the step of dividing said semiconductor wafer into said respective chip forming regions, the step of relocating electrode pads in said respective chip forming regions, and the step of forming

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bump electrodes on said relocated electrode pads,

and further comprising the step of grinding the rear surface of said semiconductor wafer after the step of relocating said electrode pads, and before the step of forming said bump electrodes.

8. The method of manufacturing a semiconductor device according to Claim 6, wherein said method further comprises the step of forming identifying marks on regions on the rear surface side of said semiconductor wafer which regions correspond to said respective chip forming regions, after the step of grinding the rear surface of said semiconductor wafer, and before the step of forming said bump electrodes.

9. The method of manufacturing a semiconductor device according to Claim 8, wherein said identifying marks are formed on the rear surface of said semiconductor wafer by the laser marking method or the ink marking method.

10. The method of manufacturing a semiconductor device according to Claim 8, wherein said identifying marks are formed by the laser marking method or the ink marking method on a mark forming layer formed on the rear surface of said semiconductor wafer.

11. The method of manufacturing a semiconductor device according to Claim 10, wherein said mark forming layer is comprised of an epoxy series resin to which carbon has been added.

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12. A method of manufacturing a semiconductor device, comprising

the step of forming a plurality of chip forming regions having circuits, on the front surface of a semiconductor wafer,

the step of measuring the electric characteristics of the circuits in said respective chip forming regions, and

the step of forming identifying marks on the rear surface side of said semiconductor wafer which corresponds to said respective chip forming regions, said identifying marks containing the characteristic information based on the electric characteristic results of said respective circuits which have been obtained at said measuring step.

13. The method of manufacturing a semiconductor device according to Claim 12, wherein said method comprises the step of relocating electrode pads in said respective chip forming regions, after the step of forming said respective chip forming regions, and before the step of forming said identifying marks.

14. The method of manufacturing a semiconductor device according to Claim 13, wherein said method comprises the step of grinding the rear surface of said semiconductor wafer, after the step of relocating said electrode pads, and before the step of forming said identifying marks.

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15. The method of manufacturing a semiconductor device according to Claim 13, wherein said method comprises the step of forming bump electrodes on said relocated electrode pads, after the step of forming said identifying marks.

16. The method of manufacturing a semiconductor device according to Claim 15, wherein said method comprises the step of dividing said semiconductor wafer into said respective chip forming regions, after said bump electrode are formed.

17. The method of manufacturing a semiconductor device according to Claim 12, wherein said identifying marks comprise two-dimensional code marks.

18. The method of manufacturing a semiconductor device according to Claim 12, wherein said identifying marks are formed on the rear surface of said semiconductor wafer by the ink marking method.

19. The method of manufacturing a semiconductor device according to Claim 12, wherein said identifying marks are formed by the laser marking method or the ink marking method on a mark forming layer formed on the rear surface of said semiconductor wafer.

20. The method of manufacturing a semiconductor device according to Claim 19, wherein said mark forming layer is comprised of an epoxy series resin to which carbon has been added.

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