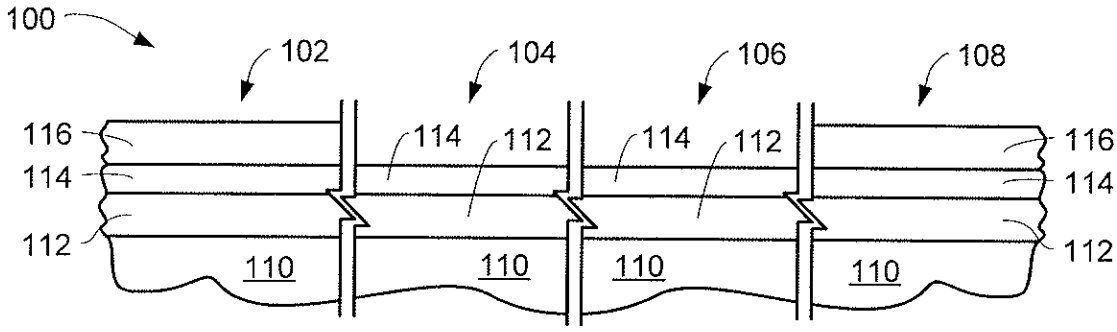


FIG. 1

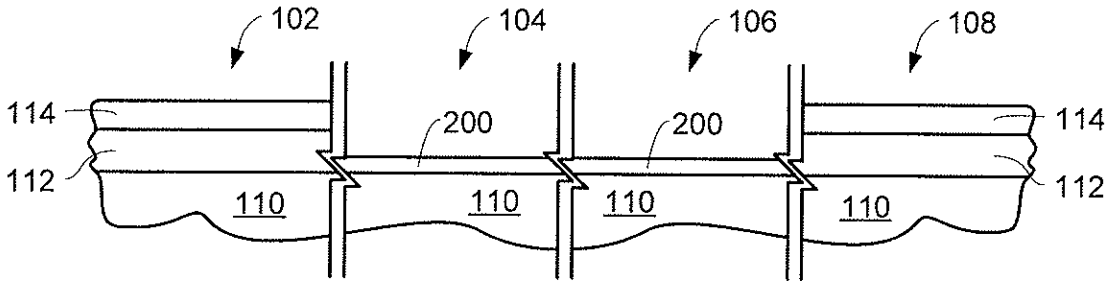


FIG. 2

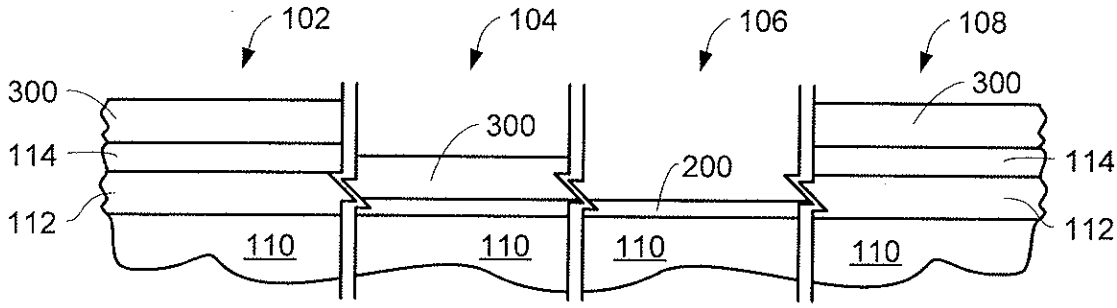


FIG. 3

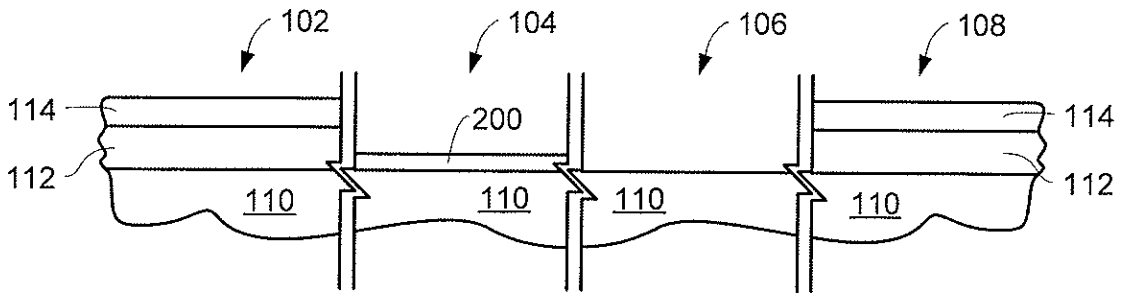


FIG. 4

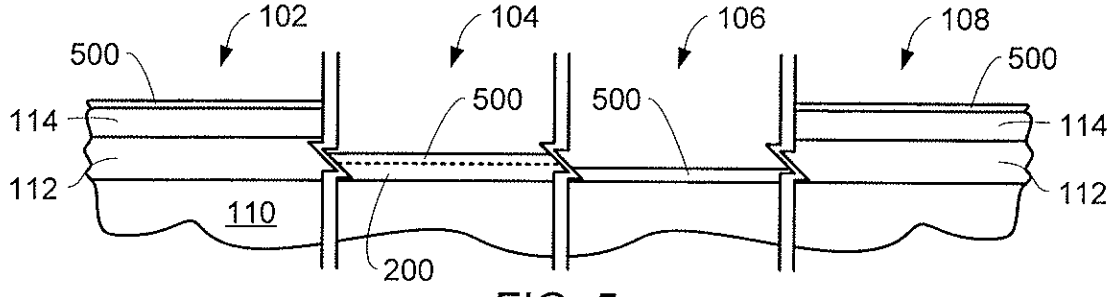


FIG. 5

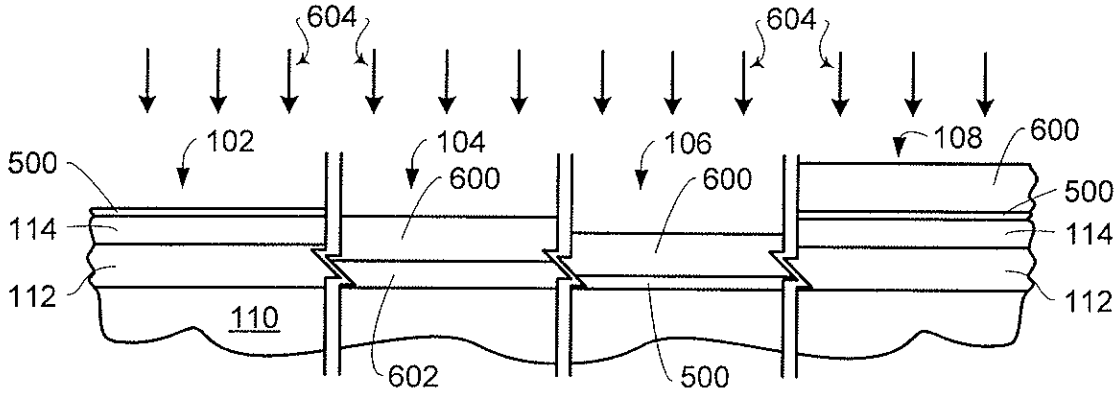


FIG. 6

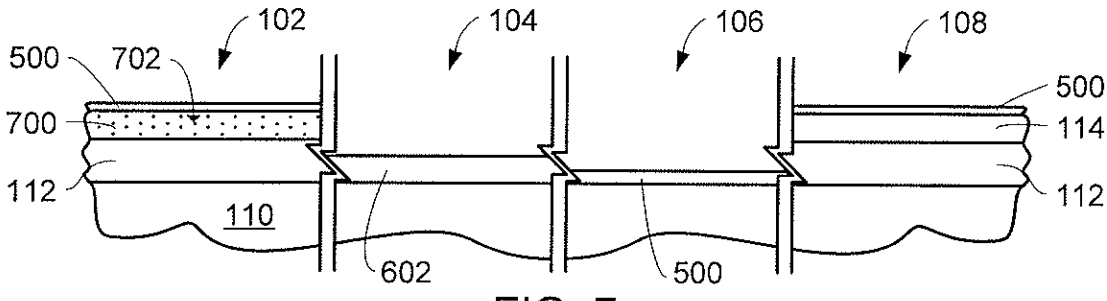


FIG. 7

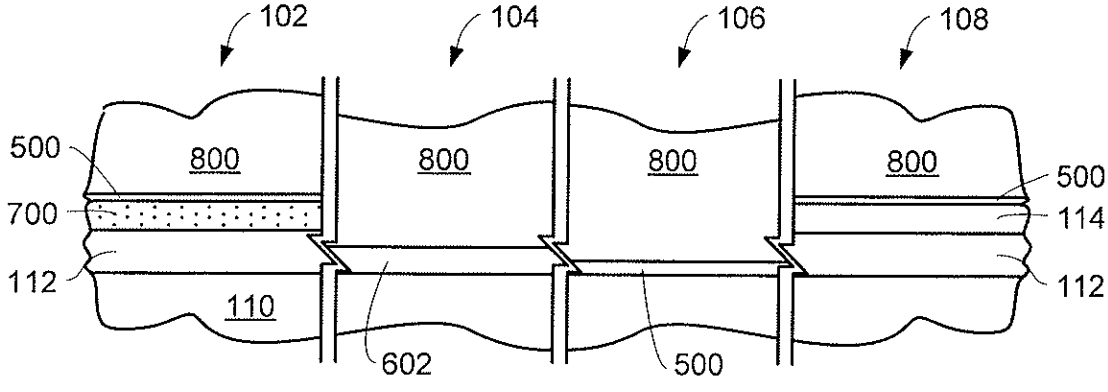


FIG. 8

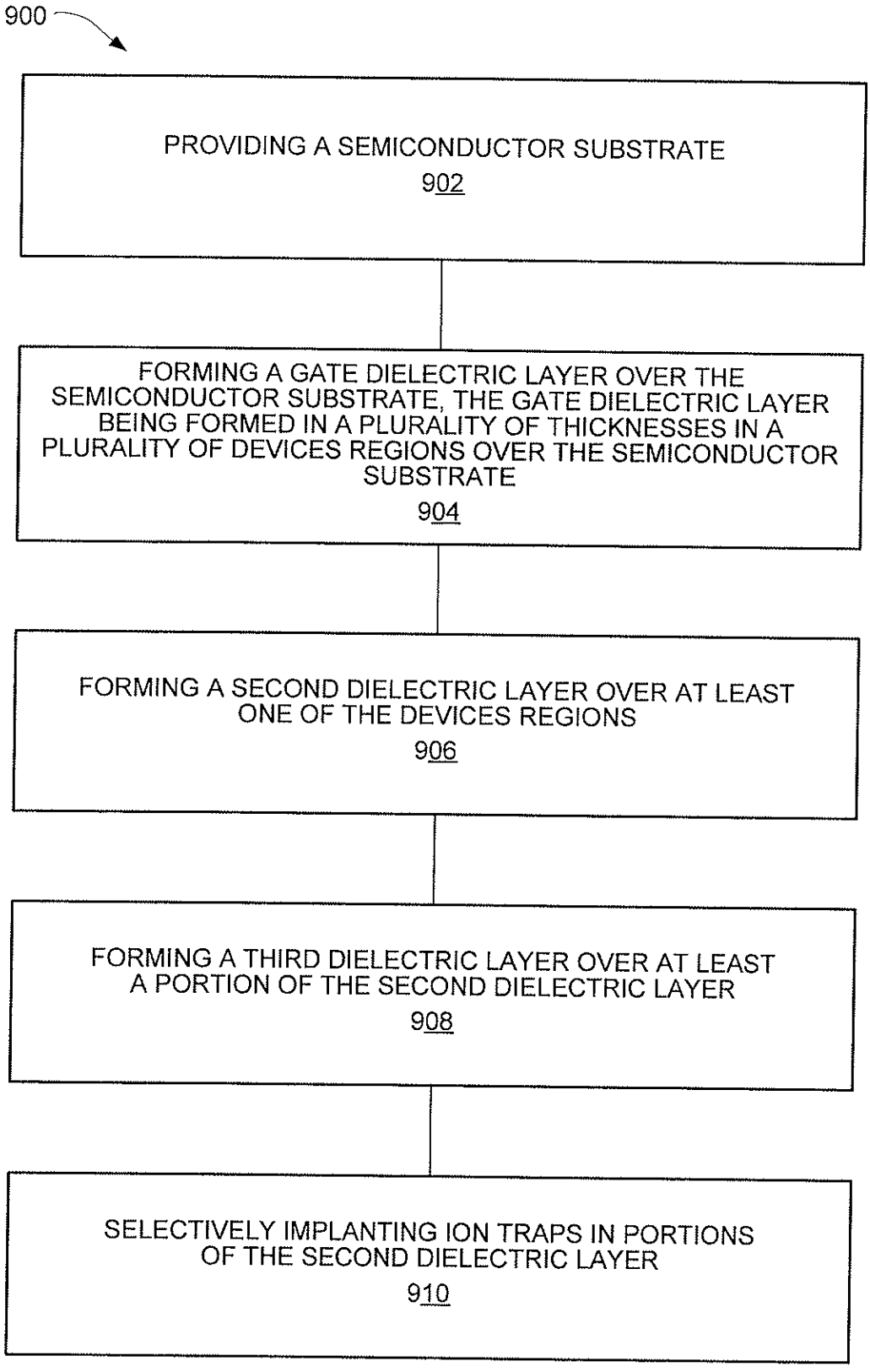

900
PROVIDING A SEMICONDUCTOR SUBSTRATE
902
FORMING A GATE DIELECTRIC LAYER OVER THE SEMICONDUCTOR SUBSTRATE, THE GATE DIELECTRIC LAYER BEING FORMED IN A PLURALITY OF THICKNESSES IN A PLURALITY OF DEVICES REGIONS OVER THE SEMICONDUCTOR SUBSTRATE
904
FORMING A SECOND DIELECTRIC LAYER OVER AT LEAST ONE OF THE DEVICES REGIONS
906
FORMING A THIRD DIELECTRIC LAYER OVER AT LEAST A PORTION OF THE SECOND DIELECTRIC LAYER
908
SELECTIVELY IMPLANTING ION TRAPS IN PORTIONS OF THE SECOND DIELECTRIC LAYER
910

FIG. 9