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Description

Method for connecting an integrated circuit to a substrate and corresponding circuit arrangement

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The present invention relates to a method for connecting an integrated circuit to a substrate and a corresponding circuit arrangement.

10 Although applicable in principle to any desired integrated circuits, the present invention and the problems underlying it are explained with respect to chips with integrated circuits in silicon technology.

15 Known CSP (Chip Size Package) or WLP (Wafer Level Package) solutions for connecting an integrated circuit to a substrate have reliability problems when there are changes in temperature, in particular in the case of large chips.

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In the case of Chip Size Packages and Wafer Level Packages, essentially two types of connection structures between the chip and the substrate are so far known.

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One customary solution for connecting an integrated circuit to a substrate is the use of ball grid arrays with rigid solder balls or bumps for mechanical connection, with additional use of an underfill to
30 increase the stability. In the case of this customary solution, the mismatching of the thermal properties of the chip and the substrate, in particular the coefficient of thermal expansion, leads to great risks in terms of reliability. The solder balls can be
35 sheared off when there are changes in temperature. In particular in the case of large chips, this reduces the reliability considerably.



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Various types of intermediate connecting plates, which serve as a stress buffer between the chip with a low coefficient of thermal expansion and the substrate with a high coefficient of thermal expansion, have been developed to prevent undesired defects of this type. Solutions of this type increase the height of the structure, the number of connections and at least the costs.

- 10 A further solution for connecting an integrated circuit to a substrate is the use of elastic elevations.

WO 00/79589 A1 discloses an electronic component which has flexible elevations of an insulating material on one surface, an electrical contact being disposed on the flexible elevation and a conduction path being disposed on the surface or in the interior of the flexible elevation between the electrical contact and the electronic circuit. The advantage of this solution is a lower height of the structure, greater reliability and lower costs. In this connection, it is known to solder or adhesively bond the elastic contact elements onto the substrate. Common to both groups is that the contact elements of the chip are firmly connected to the contact elements of the substrate, either by solder or by an adhesive.

Structures or methods in which the contact elements are not firmly connected to one another are not known.

30 An object of the present invention is to provide a simple and low-cost method for connecting an integrated circuit to a substrate and a corresponding circuit arrangement which remains largely uninfluenced by thermal mismatching.

This object is achieved according to the invention by the method for connecting an integrated circuit to a

substrate according to Claim 1 and the corresponding circuit arrangement according to Claim 15.

The idea on which the present invention is based is to
5 use a contact system in which the ends of the contact elements of the integrated circuit and substrate are not firmly connected to one another but are placed one on top of the other, while being under a specific pressure.

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In this case, the electrical contact structure of the integrated circuit and/or the electrical contact structure of the substrate may have elastic elevations.

15 The contact surfaces of the contact structures on both sides should be of such a nature that they are stable for a long time with regard to the pressure contact and have good electrical functionality. It must also be ensured that the material of the elastic elevations
20 retains the desired elasticity in the entire application range.

Advantageous developments and improvements of the respective subject matter of the invention can be found
25 in the subclaims.

According to one preferred development, the frame structure at least partially surrounds the integrated circuit laterally with a subregion.

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According to a further preferred development, the subregion is a peripheral annular region.

According to a further preferred development, the
35 subregion is an interrupted support region.

According to a further preferred development, the subregion does not touch the surface of the substrate

when the first electrical contact structure is placed onto the second electrical contact structure.

According to a further preferred development, heating
5 is carried out after placement to bring the frame structure to the substrate, the subregion expanding to such an extent that, at a specific temperature, the subregion touches the surface of the substrate and, when it cools down, the subregion remains attached to
10 the surface of the substrate.

In the case of this preferred development, a construction which independently has a pressure on the elastic elevations of the contact elements is used, it
15 having to be ensured that the connection can be maintained in the entire application range, in particular temperature range, without external assistance. Although this embodiment is very advantageous, it is of course also possible in the case
20 of the connection to apply an external pressure, either to create the connection in the first place or to assist this internal effect.

According to a further preferred development, a
25 compression stop region, which limits the compression of the elastic elevations, is provided on the first main area of the integrated circuit.

According to a further preferred development, a wiring
30 metallization is provided on the elastic elevations.

According to a further preferred development, the frame structure has a planar base region, on which the second main area of the integrated circuit is attached and
35 which protrudes laterally beyond the integrated circuit, the subregion being connected to the base region at a lateral distance from the integrated circuit.

According to a further preferred development, the frame structure is formed as one part.

- 5 According to a further preferred development, the subregion is adhesively bonded or soldered to the surface of the substrate.

10 According to a further preferred development, the first electrical contact structure and the second electrical contact structure are brought into mechanical contact in such a way that they are displaceable with respect to each other in the common plane when there is different thermal expansion of the substrate and the
15 integrated circuit. One particular advantage of this development is that, when there are changes in temperature, the contact elements are displaceable in relation to one another, so that the different expansion of the electrical circuit and the substrate
20 does not have any destructive effects, or it is not opposed.

According to a further preferred development, the first electrical contact structure has the elastic elevations
25 and the second electrical contact structure has planar terminal regions.

According to a further preferred development, the planar terminal regions have much greater expansion
30 than seating regions of the elastic elevations.

An exemplary embodiment of the invention is explained in more detail in the description which follows and is represented in the drawings, in which:
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Figure 1 shows a schematic view of part of a circuit arrangement according to one embodiment of the present invention; and

Figures 2a-c show schematic representations of a method for connecting the part according to Figure 1 to a substrate according to the embodiment of the present invention.

In the figures, the same reference numerals designate the same or functionally the same components.

Figure 1 is a schematic view of part of a circuit arrangement according to one embodiment of the present invention.

In Figure 1, reference numeral 1 designates an integrated circuit, which is integrated in a semiconductor chip, for example of silicon, which has a first, front main area HF1 and a second, rear main area HF2.

Although in the example which follows only one semiconductor chip is illustrated, it should be expressly mentioned that the method according to the invention and the corresponding circuit arrangement can be carried out at a higher level, for example wafer level.

Furthermore, in Figure 1 reference numeral 2 designates electrical contacts of the integrated circuit 1 on the first main area HF1, which is not represented in detail, with respect to a wiring metallization 4, the contact 2 being led through an insulating layer 7 lying in between.

Provided on the insulating layer 7 are elastic elevations 3, on the tips of which the wiring metallization 4 is led, since these tips represent the electrical contact regions.

Also located on the first main area HF1 of the integrated circuit 1, in the edge region, are compression stop elements 10, which are inelastic and are intended to limit the compression of the elastic elevations 3 to a predetermined maximum value, in order
5 in this way to counteract possible destruction of the same.

The second main area HF2 of the integrated circuit 1 is adhesively bonded onto a rear side element 20 of a
10 frame structure by a bonding agent 15, the rear side element 20 extending laterally beyond the extent of the integrated circuit 1. Provided laterally alongside the integrated circuit 1, at a distance created by an
15 intermediate space 5, is an annularly peripheral subregion 22 of the frame structure, which in the normal state, i.e. for example at room temperature, has an extent up to approximately half the height of the elastic elevations 3.

20 In the case of this embodiment, the subregion 22 is a peripheral ring, but could likewise comprise individual discrete supports. The annular form has the advantage that it allows the packing of the integrated circuit 1
25 to be made hermetic, i.e. protected from any environmental influences.

In this connection it should be noted that, in the case of this embodiment, the frame structure 20, 22 is
30 specified as being of two parts, but could also quite well be formed as one part.

Figures 2a-c are schematic representations of a method for connecting the part according to Figure 1 to a
35 substrate according to the embodiment of the present invention.

In order to attach the part of the circuit arrangement according to the embodiment of the invention, which is shown in Figure 1, onto a substrate 30, for example a circuit board, in the case of the present embodiment
5 the material of which the subregions 22 consist is a material which can be adhesively bonded onto the surface OS of the substrate 30.

In the case of the exemplary embodiment shown, firstly
10 the part of the circuit arrangement which is shown in Figure 1 is placed onto the substrate 30 in such a way that the contact structure on the first main area of the integrated circuit 1, comprising the elastic elevations 3 with the wiring metallization 4 located on
15 them, is placed onto corresponding planar contact regions 33 of the substrate. In this case, there is an intermediate space G between the lower end of the annular subregion 22 and the surface OS of the substrate 30 at normal temperature, for example at room
20 temperature.

The subregion 22 has a much greater coefficient of thermal expansion than the remaining structure enclosed by it, that is to say the adhesive 15, the
25 semiconductor chip with the integrated circuit 1, the elastic elevations 3 and the wiring metallization or else the compression stop elements 10.

For connecting the two components, heating then takes
30 place, during which the subregion 22 expands to such an extent that, at a predetermined temperature, it touches the surface OS of the substrate 30 and adhesively bonds to it. During the subsequent cooling down, the adhesive bond is retained, but an internal tensile
35 stress ST is produced, having the effect that the elastic elevations 3 are compressed and the wiring metallization 4 is firmly pressed at its tips onto the contact areas 33 of the substrate 30.

In order to avoid excessive compression of the elastic elevations 3, the compression stop region 10 restricts the approach of the electrical circuit 1 to the substrate 30 to a predetermined value.

A major advantage of this embodiment is that the pressure can be internally generated, without the application of an external pressure, for example to the outer area of the rear side element 20, being necessary. Of course, an external pressure of this type can be applied to assist or as an alternative.

When realizing a connection of this type, attention must be paid to the coefficients of thermal expansion and the Young's moduli during material selection. Suitable in particular as the material for the elastic elevations 3 are materials with a Young's modulus of $E \ll 100 \text{ GPa}$. Examples of such materials are silicones or combinations of silicones with gas bubbles to increase the Young's modulus.

Gold is expediently preferred as the contact material for the contact regions. It is inert and stable and is not damaged when there is possible lateral displacement during the cyclical changes in temperature.

Expedient as the material for the rear side element 20 is metal or a hard epoxy resin. If copper is used as the metal, the coefficient of thermal expansion would be the best that can be adapted to the substrate to avoid any further stresses in the construction.

Appearing to be suitable as the material for the subregion 22 would be an epoxy resin with a high coefficient of thermal expansion, which makes it possible to build up the internal pressure in the desired way. It would in this case be possible for the

adhesive bond to be realized by a thermoplastic adhesion process, which is not discontinued when cooling down and shrinking occur.

- 5 A typical application range lies between -45°C and 125°C . If, for example, 125°C is the maximum temperature of the application of the connection, the temperature at which the adhesive bond between the subregion 22 and the surface OS of the substrate forms
10 must lie above this, in order that the adhesive bond between the subregion 22 and the surface OS of the substrate still remains intact even at 125°C .

In the event that there is a strong thermal mismatch
15 between the subregion 22 and the rear side element 20, there could be problems with the annular form of the subregion 22, so that in this case division of the subregion 22 into individual supports would be helpful.

20 Although the present invention was described above on the basis of a preferred exemplary embodiment, it is not restricted to this, but can be modified in a variety of ways.

25 The present invention can be applied in particular not only to chips, but also to hybrids, wafers or other integrated circuits.

List of designations

1	integrated circuit
2	contacts
3	elastic elevation
4	wiring metallization
7	insulating layer
10	compression stop element
HF1, HF2	main areas
5	intermediate space
15	bonding agent
20	rear side element of the frame
22	annular subregion of the frame
30	circuit board
OS	upper side
33	planar contact elements
G	intermediate space
ST	internal stress

Patent claims

1. Method for connecting an integrated circuit (1), in particular of a chip or a wafer or a hybrid, to a substrate (30), which has the following steps:
 - provision of a first electrical contact structure (3, 4) on a first main area (HF1) of the integrated circuit (1);
 - provision of a corresponding second electrical contact structure (33) on an upper side (OS) of the substrate (30);
 - at least one of the first and second electrical contact structures (3, 4; 33) having elastic elevations (3);
 - attachment of a second main area (HF2) of the integrated circuit (1) to a frame structure (20, 22);
 - placement of the first electrical contact structure (3, 4) onto the second electrical contact structure (33), so that the two are in electrical contact; and
 - attachment of the frame structure (20, 22) to the substrate (30) in such a way that the elastic elevations (3) are compressed.
2. Method according to Claim 1, characterized in that the frame structure (20, 22) at least partially surrounds the integrated circuit (1) laterally with a subregion (22).
3. Method according to Claim 2, characterized in that the subregion (22) is a peripheral annular region.

4. Method according to Claim 2, characterized in that the subregion (22) is an interrupted support region.
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5. Method according to Claim 2, 3 or 4, characterized in that the subregion (22) does not touch the surface (OS) of the substrate (30) when the first electrical contact structure (3, 4) is placed onto
10 the second electrical contact structure (33).
6. Method according to Claim 5, characterized in that heating is carried out after placement to bring the frame structure (20, 22) to the substrate (30), the
15 subregion (22) expanding to such an extent that, at a specific temperature, the subregion (22) touches the surface (OS) of the substrate (30) and, when it cools down, the subregion (22) remains attached to the surface (OS) of the substrate.
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7. Method according to one of the preceding claims, characterized in that a compression stop region (10), which limits the compression of the elastic elevations (3), is provided on the first main area
25 (HF1) of the integrated circuit (1).
8. Method according to one of the preceding claims, characterized in that a wiring metallization (4) is provided on the elastic elevations (3).
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9. Method according to one of the preceding claims, characterized in that the frame structure (20, 22) has a planar base region (20), on which the second main area (HF2) of the integrated circuit (1) is
35 attached and which protrudes laterally beyond the integrated circuit (1), and the subregion (22) is connected to the base region (20) at a lateral distance from the integrated circuit (1).

10. Method according to one of the preceding claims,
characterized in that the frame structure (20, 22)
is formed as one part.
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11. Method according to one of the preceding Claims 2
to 10, characterized in that the subregion (22) is
adhesively bonded or soldered to the surface (OS)
of the substrate (30).
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12. Method according to one of the preceding claims,
characterized in that the first electrical contact
structure (3, 4) and the second electrical contact
structure (33) are brought into mechanical contact
15 in such a way that they are displaceable with
respect to each other in the common plane when
there is different thermal expansion of the
substrate (30) and the integrated circuit (1).
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13. Method according to one of the preceding claims,
characterized in that the first electrical contact
structure (3 , 4) has the elastic elevations (3)
and the second electrical contact structure (33)
has planar terminal regions.
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14. Method according to Claim 13, characterized in that
the planar terminal regions have much greater
expansion than seating regions of the elastic
elevations (3).
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15. Circuit arrangement which has a connection of an
integrated circuit (1), in particular of a chip or
a wafer or a hybrid, to a substrate (30), with:
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- a first electrical contact structure (3, 4) on a
first main area (HF1) of the integrated circuit
(1);

a corresponding second electrical contact structure (33) on an upper side (OS) of the substrate (30);

5 at least one of the first and second electrical contact structures (3, 4; 33) having elastic elevations (3);

10 a frame structure (20, 22), which is attached to a second main area (HF2) of the integrated circuit (1);

15 the first electrical contact structure (3, 4) having been placed onto the second electrical contact structure (33), so that the two are in electrical contact; and

20 the frame structure (20, 22) having been attached to the substrate (30) in such a way that the elastic elevations (3) are compressed.

25 16. Circuit arrangement according to Claim 15, characterized in that the frame structure (20, 22) at least partially surrounds the integrated circuit (1) laterally with a subregion (22).

17. Circuit arrangement according to Claim 16, characterized in that the subregion (22) is a peripheral annular region.

30 18. Circuit arrangement according to Claim 16, characterized in that the subregion (22) is an interrupted support region.

35 19. Circuit arrangement according to one of the preceding Claims 15 to 18, characterized in that a compression stop region (10), which limits the compression of the elastic elevations (3), is

provided on the first main area (HF1) of the integrated circuit (1).

20. Circuit arrangement according to one of the
5 preceding Claims 15 to 19, characterized in that a wiring metallization (4) is provided on the elastic elevations (3).
21. Circuit arrangement according to one of the
10 preceding Claims 15 to 20, characterized in that the frame structure (20, 22) has a planar base region (20), on which the second main area (HF2) of the integrated circuit (1) is attached and which protrudes laterally beyond the integrated circuit
15 (1), and the subregion (22) is connected to the base region (20) at a lateral distance from the integrated circuit (1).
22. Circuit arrangement according to one of the
20 preceding Claims 15 to 21, characterized in that the frame structure (20, 22) is formed as one part.
23. Circuit arrangement according to one of the
25 preceding Claims 15 to 22, characterized in that the subregion (22) is adhesively bonded or soldered to the surface (OS) of the substrate (30).
24. Circuit arrangement according to one of the
30 preceding Claims 15 to 23, characterized in that the first electrical contact structure (3, 4) and the second electrical contact structure (33) are brought into mechanical contact in such a way that they are displaceable with respect to each other in the common plane when there is different thermal
35 expansion of the substrate (30) and the integrated circuit (1).

25. Circuit arrangement according to one of the preceding Claims 15 to 24, characterized in that the first electrical contact structure (3 , 4) has the elastic elevations (3) and the second
5 electrical contact structure (33) has planar terminal regions.

26. Circuit arrangement according to Claim 25, characterized in that the planar terminal regions
10 have much greater expansion than seating regions of the elastic elevations (3).