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PATENT SPECIFICATION

DRAWINGS ATTACHED

Inventor: RAYMOND MYRL WARNER JR.

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COMPLETE SPECIFICATION

Compound Channel Insulated Gate Device

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to compound channel insulated gate devices such as metal - oxide - semiconductor (MOS) field effect transistor (FET) devices, and more particularly relates to an enhancement-mode device having an increased output impedance and a higher gain.

According to the present invention there is provided a compound-channel semiconductor device comprising first and second enhancement-mode channels each having a drain end, a source end and a control gate separated from the respective channel by an insulating layer, the first conductance channel having a greater transconductance than the second channel at a given gate bias, the drain of the first channel being the drain of the device, the source end of the first channel being joined at least electrically to the drain end of the second channel, the source of the second channel being the source of the device, and the control gates of the first and second channel being electrically joined.

The two channels may be fabricated on a common substrate and the different transconductance values achieved by differences in the width-to-length ratios of the channels, or differences in the thickness of the gate insulating layer over the respective channels.

The invention may best be understood by reference to the following detailed descrip-

tion of illustrative embodiments, when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a schematic circuit diagram of a compound-channel MOS device constructed in accordance with the present invention;

Figure 2 is a plot of drain current with respect to drain voltage of one of the channels of the device illustrated in Figure 1 for various voltages applied to the control gate of the channel;

Figure 3 is a plot similar to Figure 2 of drain current with respect to drain voltage of the other channel of the device of Figure 1 for various voltages applied to the control gate of the channel;

Figure 4 is a plot similar to Figures 2 and 3 of drain current with respect to drain voltage of the compound-channel device of Figure 1 for various voltages applied to the common control gate;

Figure 5 is a plan view of an embodiment of the device illustrated schematically in Figure 1 fabricated on a common substrate;

Figure 6 is a sectional view taken substantially on lines 6—6 of Figure 5;

Figure 7 is a plan view of another embodiment of the compound-channel device illustrated in Figure 1 which is also fabricated on a common substrate; and

Figure 8 is a sectional view taken substantially on lines 8—8 of Figure 7.

Referring now to the drawings, a compound-channel MOS device constructed in accordance with the present invention is indicated generally by the reference numeral 10 in the schematic diagram of Figure 1. The present invention is applicable to either a p-channel or an n-channel enhancement-mode MOS device, the only difference being that the polarities of the various voltages involved

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are changed. For convenience, however, only p-channel devices will herein be described. The compound-channel device 10 comprises first and second enhancement-mode channels A and B, respectively. The source of the first channel A is electrically common with the drain of the second channel B. The drain of the first channel A forms the drain of the compound-channel device and the source of channel B forms the source of the compound-channel device. The control gates of the two channels A and B are electrically common and form the input for the compound-channel device. Similarly, the substrate portions of each of the channels, which forms a back gate for each channel, are common with the source terminal of the compound-channel device. The transconductance, and hence the "saturation current" at a particular set of bias voltages, of the first channel A exceeds the transconductance of the second channel B at the given gate bias voltage, preferably by a substantial amount.

If the conductances of the individual channels A and B are G_A and G_B , respectively, at a given gate bias greater than the threshold voltage, then the conductance of the compound-channel device 10 may be represented by the following expression at lower drain voltages:

$$\frac{G_A G_B}{G_A + G_B} \quad (1)$$

As the drain voltage is increased in the proper direction, i.e., negatively for a p-channel device and positively for an n-channel device, expression (1) will initially hold. However, as a voltage drop develops from source to drain across channel B, the gate bias on channel A, which is the source-to-gate voltage, will decrease. It will be noted that the bias on the back gate or substrate of channel A is also affected by the voltage drop in channel B and that the effects of the bias on the control gate and the back gate are additive. Therefore, as the drain voltage increases and the gate bias of channel A decreases, the conductance of channel A will decrease markedly. Then as channel B approaches the saturation region, the voltage drop from source to drain of channel A will increase at a much greater rate than the voltage from source to drain of channel B. As a result, the current through the compound-channel device increases at a substantially slower rate with an increase in the drain voltage than would be the case for either channel A or B, individually. This means that the output impedance of the compound-channel device is materially increased.

In one embodiment of the invention, two discrete MOS transistors are connected in the configuration illustrated in Figure 1. The

transistor corresponding to channel A exhibited the current-voltage characteristics illustrated in Figure 3, and the transistor corresponding to channel B exhibited the current-voltage characteristics illustrated in Figure 2. The compound channel device resulting from the interconnection of the two MOS transistors exhibited the current-voltage characteristics illustrated in Figure 4. It will be readily noted that the curves in Figure 4 of the compound channel device are significantly flatter than the corresponding curves of either of the individual devices as illustrated by the curves of Figures 2 and 3.

The saturation current I_D of a conventional MOS device can be represented by the equation:

$$I_D = \frac{\mu_e}{2\Delta} \frac{W}{L} (V_G - V_T)^2 \quad (2)$$

where:

μ is the carrier mobility,
 ϵ is the dielectric constant of the gate insulator,
 Δ is the thickness of the gate insulator,
 W is the channel width, i.e., the plan view dimension normal to current flow,
 L is the channel length, i.e., the plan view dimension parallel to current flow,
 V_G is the gate voltage with respect to the source, and
 V_T is the threshold voltage, i.e., the gate voltage at which the channel first begins to conduct.

From expression (2), it will be noted that the saturation current, and hence the transconductance of channel A, can be made greater than that of channel B by either providing channel A with a greater width-to-length ratio $\frac{W}{L}$, or by providing channel A

with a thinner insulating layer as represented by the term " Δ ". A thinner insulating layer also decreases the threshold voltage V_T , thus increasing the value of the quantity in the brackets, which is squared. Although the compound-channel device can be fabricated from two discrete MOS transistors, the device is preferably fabricated on a common substrate using a geometry which will provide channel A with a greater transconductance than channel B as a result of either a greater width-to-length ratio or a thinner insulating layer.

A device constructed in accordance with this invention which provides a greater transconductance in channel A as a result of an increased width-to-length ratio is indicated generally by the reference numeral 20 in Figures 5 and 6. The device 20 comprises first and second p-type enhancement-mode channels A_1 and B_1 , as indicated by the dotted

lines, formed in an n-type substrate 22 between three spaced, heavily doped p-type regions 24, 26 and 28. A metal control gate 30 is formed over channels A₁ and B₁ and is insulated from the channels by dielectric layers 32 and 33, respectively, of the same thickness. A drain terminal 34 is in ohmic contact with the diffused region 24, and a source terminal 36 is in ohmic contact with diffused region 28. It will be noted that channels A₁ and B₁ have the same width, that is, the plan view dimension normal to the direction of current flow. However, the length, that is, the plan view dimension parallel to current flow, of channel B₁ is approximately twice that of channel A₁. Therefore, the width-to-length ratio of channel A is approximately twice the width-to-length ratio of channel B, as would be its transconductance.

Another compound-channel MOS device constructed in accordance with the present invention wherein the difference in transconductance is provided by a difference in the width-to-length ratios is indicated generally by the reference numeral 40 in Figures 7 and 8. The device 40 comprises channels A₂ and B₂ formed between heavily doped, p-type diffused regions 42, 44 and 46 in an n-type substrate 48. A common metal control gate 49 is formed over both channels A₂ and B₂ and is electrically insulated from the channels by an insulating layer 50 and layer 51, respectively, of the same thickness. A drain terminal 52 is in ohmic contact with diffused region 42, and a source terminal 54 is in ohmic contact with diffused region 46. In the device 40, the length of channel A₂ is equal to the length of channel B₂, but the width of channel A₂ is approximately twice the width of channel B₂ so that channel A₂ has a substantially higher transconductance for any given gate bias voltage and source and drain voltages.

As mentioned, the difference in transconductance between channels A and B can also be achieved by varying the thickness of the insulating layer separating the common gate from each of the channels. The lengths of the channels can then be the smallest value that technology permits, and the widths of the channels can be equal. As a result, the intermediate heavily doped p-type diffused region can be eliminated. This combination of factors means that the device can then occupy substantially less area for a given performance. However, the device then has the disadvantage of requiring greater processing complexity in order to achieve the two insulating layers having different thicknesses. The intermediate diffused regions 26 and 44 can also be eliminated to achieve a smaller device, if desired, by making the insulating layer 32 thinner along the junction between the two channels. Then the channel induced by the gate electrode overlying the thinner oxide

will produce an enhanced channel of greater depth which will simulate the diffused region and provide a relatively low resistance path at the junction between the channels.

The devices 20 and 40 may be fabricated using any conventional process for fabricating MOS transistor devices. Although the back gates of the channels are illustrated as common with the source of channel B, in some integrated circuit applications, such as when the device is used as a load for an amplifier, the back gates may not be common with the source.

WHAT WE CLAIM IS:—

1. A compound-channel semiconductor device comprising first and second enhancement-mode channels each having a drain end, a source end and a control gate separated from the respective channel by an insulating layer, the first conductance channel having a greater transconductance than the second channel at a given gate bias, the drain of the first channel being the drain of the device, the source end of the first channel being joined at least electrically to the drain end of the second channel, the source of the second channel being the source of the device, and the control gates of the first and second channel being electrically joined.
2. A device according to claim 1, wherein the first and second channels are both formed on a common substrate.
3. A device according to claims 1 and 2, wherein the said first and second channels are defined by three heavily doped regions of conductivity type opposite that of the substrate.
4. A device according to any of the preceding claims, wherein the width-to-length ratio of the first channel is greater than the width-to-length ratio of the second channel to produce the greater transconductance.
5. A device according to claim 4, wherein the width of the first channel is greater than the width of the second channel to produce the greater transconductance of the first channel.
6. A device according to claim 4, wherein the length of the second channel is greater than the length of the first channel to produce the greater transconductance of the first channel.
7. A device according to claim 1 or 2, wherein the insulating layer separating the control gate of the first channel from that channel is thinner than the insulating layer separating the control gate of the second channel.
8. A device according to claim 1, wherein each of said channels is a discrete device.
9. A compound channel insulated gate semiconductor device substantially as herein described with reference to Figure 1, Figures



lines, formed in an n-type substrate 22 between three spaced, heavily doped p-type regions 24, 26 and 28. A metal control gate 30 is formed over channels A_1 and B_1 and is insulated from the channels by dielectric layers 32 and 33, respectively, of the same thickness. A drain terminal 34 is in ohmic contact with the diffused region 24, and a source terminal 36 is in ohmic contact with diffused region 28. It will be noted that channels A_1 and B_1 have the same width, that is, the plan view dimension normal to the direction of current flow. However, the length, that is, the plan view dimension parallel to current flow, of channel B_1 is approximately twice that of channel A_1 . Therefore, the width-to-length ratio of channel A is approximately twice the width-to-length ratio of channel B, as would be its transconductance.

Another compound-channel MOS device constructed in accordance with the present invention wherein the difference in transconductance is provided by a difference in the width-to-length ratios is indicated generally by the reference numeral 40 in Figures 7 and 8. The device 40 comprises channels A_2 and B_2 formed between heavily doped, p-type diffused regions 42, 44 and 46 in an n-type substrate 48. A common metal control gate 49 is formed over both channels A_2 and B_2 and is electrically insulated from the channels by an insulating layer 50 and layer 51, respectively, of the same thickness. A drain terminal 52 is in ohmic contact with diffused region 42, and a source terminal 54 is in ohmic contact with diffused region 46. In the device 40, the length of channel A_2 is equal to the length of channel B_2 , but the width of channel A_2 is approximately twice the width of channel B_2 so that channel A_2 has a substantially higher transconductance for any given gate bias voltage and source and drain voltages.

As mentioned, the difference in transconductance between channels A and B can also be achieved by varying the thickness of the insulating layer separating the common gate from each of the channels. The lengths of the channels can then be the smallest value that technology permits, and the widths of the channels can be equal. As a result, the intermediate heavily doped p-type diffused region can be eliminated. This combination of factors means that the device can then occupy substantially less area for a given performance. However, the device then has the disadvantage of requiring greater processing complexity in order to achieve the two insulating layers having different thicknesses. The intermediate diffused regions 26 and 44 can also be eliminated to achieve a smaller device, if desired, by making the insulating layer 32 thinner along the junction between the two channels. Then the channel induced by the gate electrode overlying the thinner oxide

will produce an enhanced channel of greater depth which will simulate the diffused region and provide a relatively low resistance path at the junction between the channels.

The devices 20 and 40 may be fabricated using any conventional process for fabricating MOS transistor devices. Although the back gates of the channels are illustrated as common with the source of channel B, in some integrated circuit applications, such as when the device is used as a load for an amplifier, the back gates may not be common with the source.

WHAT WE CLAIM IS:—

1. A compound-channel semiconductor device comprising first and second enhancement-mode channels each having a drain end, a source end and a control gate separated from the respective channel by an insulating layer, the first conductance channel having a greater transconductance than the second channel at a given gate bias, the drain of the first channel being the drain of the device, the source end of the first channel being joined at least electrically to the drain end of the second channel, the source of the second channel being the source of the device, and the control gates of the first and second channel being electrically joined.

2. A device according to claim 1, wherein the first and second channels are both formed on a common substrate.

3. A device according to claims 1 and 2, wherein the said first and second channels are defined by three heavily doped regions of conductivity type opposite that of the substrate.

4. A device according to any of the preceding claims, wherein the width-to-length ratio of the first channel is greater than the width-to-length ratio of the second channel to produce the greater transconductance.

5. A device according to claim 4, wherein the width of the first channel is greater than the width of the second channel to produce the greater transconductance of the first channel.

6. A device according to claim 4, wherein the length of the second channel is greater than the length of the first channel to produce the greater transconductance of the first channel.

7. A device according to claim 1 or 2, wherein the insulating layer separating the control gate of the first channel from that channel is thinner than the insulating layer separating the control gate of the second channel.

8. A device according to claim 1, wherein each of said channels is a discrete device.

9. A compound channel insulated gate semiconductor device substantially as herein described with reference to Figure 1, Figures

5 and 6 or Figures 7 and 8 of the accompanying drawings.

ABEL & IMRAY,
Chartered Patent Agents,
Northumberland House,
303—306 High Holborn,
London, W.C.1.

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