## CLAIMS

1. A semiconductor device comprising:

a first basic block and a second basic block, each comprising a logic circuit; and

a circuit configured to control a connection between the first basic block and the second basic block,

wherein the circuit comprises a first transistor functioning as a switching element and a second transistor configured to control supply of a potential to a gate electrode of the first transistor, and

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

2. The semiconductor device according to claim 1, the circuit configured to control a connection between the first basic block and the second basic block further comprising a third transistor configured to control supply of a fixed potential to one of a source electrode and a drain electrode of the first transistor.

3. The semiconductor device according to claim 1, the circuit configured to control a connection between the first basic block and the second basic block further comprising a capacitor connected to the gate electrode of the first transistor.

4. The semiconductor device according to claim 1, the circuit configured to control a connection between the first basic block and the second basic block further comprising a resistor connected to one of a source electrode and a drain electrode of the first transistor.

5. The semiconductor device according to claim 1, wherein the oxide semiconductor layer comprises an In–Ga–Zn–O-based oxide semiconductor.

6. The semiconductor device according to claim 1, wherein hydrogen concentration in the channel formation region is lower than or equal to $5\times10^{19}/cm^3$.

7. The semiconductor device according to claim 1,

wherein the hydrogen concentration in the oxide semiconductor layer which is measured by secondary ion mass spectrometry is less than or equal to $5 \times 10^{19}/cm^3$,

wherein the carrier density of the oxide semiconductor film measured by Hall effect measurement is less than $1 \times 10^{14}/cm^3$,

wherein the band gap of the oxide semiconductor is greater than or equal to 2 eV, and

wherein off-state current density of the second transistor is lower than or equal to 100 zA/μm.

8. The semiconductor device according to claim 1, wherein the first transistor comprises at least one of silicon, silicon germanium, and germanium which have crystallinity.

9. An electronic apparatus including the semiconductor device according to claim 1.

10. The semiconductor device according to claim 1, wherein the only transistors comprised in the circuit configured to control a connection between the first basic block and the second basic block are the first transistor and the second transistor.

11. A semiconductor device comprising:

basic blocks each comprising a logic circuit; and

programming cells configured to control supply of a power supply potential

to each of the basic blocks,

wherein the programming cells each comprise a first transistor functioning as a switching element and a second transistor configured to control supply of a potential to a gate electrode of the first transistor, and

wherein the second transistors each comprise a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

12. A semiconductor device comprising:

basic blocks each comprising a logic circuit; and

programming cells each configured to control connections between two of the basic blocks,

wherein the programming cells each comprise a first transistor functioning as a switching element and a second transistor configured to control supply of a potential to a gate electrode of the first transistor, and

wherein the second transistors each comprise a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

13. A semiconductor device comprising:

basic blocks each comprising a logic circuit;

first programming cells each configured to control connections between two of the basic blocks; and

second programming cells configured to control supply of a power supply potential to each of the basic blocks,

wherein the first programming cells and the second programming cells each comprise a first transistor functioning as a switching element and a second transistor configured to control supply of a potential to a gate electrode of the first transistor, and

wherein the second transistors each comprise a channel formation region

comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

14. A semiconductor device comprising:

a plurality of logic circuits arranged in a matrix; and

a plurality of switching blocks arranged in a matrix, each of the plurality of switching blocks comprising a plurality of programming cells;

wherein each of the plurality of switching blocks is configured to control connections between at least four of the plurality of logic circuits,

wherein each of the plurality of programming cells comprises a first transistor functioning as a switching element and a second transistor configured to control supply of a potential to a gate electrode of the first transistor, and

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

15. A semiconductor device comprising:

a plurality of logic circuits arranged in a matrix; and

a plurality of switching blocks arranged in a matrix, each of the plurality of switching blocks comprising a plurality of programming cells;

wherein each of the plurality of switching blocks is configured to control power supply to one of the plurality of logic circuits,

wherein each of the plurality of programming cells comprises a first transistor functioning as a switching element and a second transistor configured to control supply of a potential to a gate electrode of the first transistor, and

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

16. The semiconductor device according to claim 14 or claim 15,

wherein an input terminal and an output terminal of each of the logic circuits are connected to one of the switching blocks.

17. The semiconductor device according to any one of claim 11 to claim 15, each programming cell further comprising:

a third transistor configured to control supply of a fixed potential to one of a source electrode and a drain electrode of the first transistor.

18. The semiconductor device according to any one of claim 11 to claim 15, each programming cell further comprising a resistor connected to one of a source electrode and a drain electrode of the first transistor.

19. A semiconductor device comprising:

basic blocks each comprising a logic circuit;

a node configured to be applied with a power supply potential; and

programming cells each comprising:

a first transistor comprising a gate electrode, a source electrode and a drain electrode; and

a second transistor comprising a gate electrode, a source electrode and a drain electrode, one of the source electrode and the drain electrode of the second transistor being configured to be at a same potential as the gate electrode of the first transistor,

wherein the node is connected to one of the basic blocks through the source electrode and the drain electrode of the first transistor of a corresponding one of the programming cells, and

wherein the second transistors each comprise a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

20. A semiconductor device comprising:

basic blocks each comprising a logic circuit; and

programming cells each comprising:

a first transistor comprising a gate electrode, a source electrode and a drain electrode; and

a second transistor comprising a gate electrode, a source electrode and a drain electrode, one of the source electrode and the drain electrode of the second transistor being configured to be at a same potential as the gate electrode of the first transistor,

wherein a first one of the basic blocks is connected to a second one of the basic blocks through the source electrode and the drain electrode of one of the first transistors, and

wherein the second transistors each comprise a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower intrinsic carrier density than silicon.

21. A semiconductor device comprising:

basic blocks each comprising a logic circuit;

a wiring; and

programming cells each comprising:

a first transistor comprising a gate electrode, a source electrode and a drain electrode; and

a second transistor comprising a gate electrode, a source electrode and a drain electrode, one of the source electrode and the drain electrode of the second transistor being connected to the gate electrode of the first transistor,

wherein the wiring is connected to the basic blocks through the source electrodes and the drain electrodes of the first transistors, and

wherein the second transistors each comprise a channel formation region comprising an oxide semiconductor layer having a wider band gap and a lower

intrinsic carrier density than silicon.

22. The semiconductor device according to any one of claim 19 to claim 21, each programming cell further comprising:

a third transistor comprising a gate electrode, a source electrode and a drain electrode, the gate electrode of the third transistor being connected to the gate electrode of the first transistor, and one of the source electrode and the drain electrode of the third transistor being connected to the other of the source electrode and the drain electrode of the first transistor.

23. The semiconductor device according to any one of claim 19 to claim 21, each programming cell further comprising:

a third transistor comprising a gate electrode, a source electrode and a drain electrode, the gate electrode of the third transistor being connected to the gate electrode of the first transistor, and one of the source electrode and the drain electrode of the third transistor being connected to the other of the source electrode and the drain electrode of the first transistor; and

a capacitor comprising a first electrode and a second electrode, the first electrode being connected to the other of the source electrode and the drain electrode of the third transistor, and the second electrode being connected to each of the gate electrode of the third transistor and the gate electrode of the first transistor.

24. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21,

wherein the only transistors comprised in one of the programming cells are the first transistor and the second transistor.

25. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, each programming cell further comprising:

a third transistor connected in series with the first transistor.

26. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, each programming cell further comprising a capacitor connected to the gate electrode of the first transistor.

27. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, wherein the oxide semiconductor layers comprise an In–Ga–Zn–O-based oxide semiconductor.

28. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, wherein hydrogen concentrations in the channel formation regions are lower than or equal to $5\times10^{19}/cm^3$.

29. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21,

wherein the hydrogen concentration in the oxide semiconductor layer which is measured by secondary ion mass spectrometry is less than or equal to $5 \times 10^{19}/cm^3$,

wherein the carrier density of the oxide semiconductor film measured by Hall effect measurement is less than $1 \times 10^{14}/cm^3$,

wherein the band gap of the oxide semiconductor is greater than or equal to 2 eV, and

wherein off-state current densities of the second transistors are lower than or equal to 100 zA/μm.

30. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, wherein, for one of the programming cells, the gate electrode of the first transistor is in a floating state when the second transistor is in an off-state.

31. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, wherein the first transistors each comprise at least one of silicon, silicon germanium, and germanium which have crystallinity.

32. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, wherein the first transistors and the second transistors are formed on a same substrate, the second transistors being formed over an insulating film that covers the first transistors.

33. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, wherein the first transistor and the second transistor are n-type.

34. The semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21, wherein each of the programming cells is configured to supply a fixed potential as an output when the first transistor is in an off-state.

35. A programmable logic device including the semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21.

36. An electronic apparatus including the semiconductor device according to any one of claim 11 to claim 15 and claim 19 to claim 21.