ABSTRACT OF THE DISCLOSURE

METHOD FOR FORMING A LOW CONTACT LEAKAGE AND LOW CONTACT RESISTANCE INTEGRATED CIRCUIT DEVICE ELECTRODE

A method for forming a low contact leakage and low contact resistance integrated circuit device electrode within an integrated circuit, and the low contact leakage and low contact resistance integrated circuit device electrode formed through the method. There is first formed within a semiconductor substrate an integrated circuit device electrode. The integrated circuit device electrode has a width upon the semiconductor substrate of less than the width of a conductor element desired to be formed upon the integrated circuit device electrode plus two times the registration tolerance of a fabrication tool employed in defining the location of the conductor element desired to be formed upon the integrated circuit device electrode. Formed then upon the semiconductor substrate including the integrated circuit device electrode is a blanket metal silicide forming metal layer. The semiconductor substrate is then annealed to partially consume the blanket metal silicide forming metal layer at the location of the integrated circuit device electrode and partially consume the semiconductor substrate at the location of the integrated circuit device electrode while forming a patterned metal silicide layer aligned with a partially consumed integrated circuit device electrode beneath a partially consumed blanket metal silicide forming metal layer. Finally, the blanket partially consumed metal silicide forming metal layer is patterned to form a patterned partially consumed metal silicide forming metal layer. The patterned partially consumed metal silicide forming metal layer is aligned at least partially over the partially consumed integrated circuit device electrode and the patterned metal silicide layer. The patterned partially consumed metal silicide forming metal layer has a width greater than the width of the conductor element desired to be formed upon the integrated circuit device electrode plus two times the registration tolerance of the fabrication tool employed in defining the location of the conductor element desired to be formed upon the integrated circuit device electrode. There may also be formed and aligned upon the patterned partially consumed metal silicide forming metal layer a patterned barrier layer of equivalent width.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)