Method for manufacturing a semiconductor substrate

The invention relates to a method for manufacturing a semiconductor substrate, in particular, a semiconductor-on-insulator (SOI) substrate.

Complex semiconductor substrates may be manufactured by combining two or more layers. One class of such engineered substrates are semiconductor-on-insulator substrates, wherein a top semiconductor layer is formed over a carrier substrate with a dielectric layer in between. For the top semiconductor layer and the carrier substrate, usually silicon is used and the dielectric layer is usually an oxide layer, typically a silicon oxide.

Especially, “fully depleted” SOIs (FDSOI) often take advantage of doped areas inside the carrier substrate with a back bias for tuning the threshold voltage of devices formed on the top semiconductor layer.

For the fabrication of the doped areas below the buried dielectric, ions are usually implanted through the top semiconductor layer and the buried dielectric layer. This method has, however, the drawback that a tail of the implantation profile impacts the initial doping level of the top semiconductor layers, thereby altering the device characteristics and generating a random dopant fluctuation (RDF) which induces threshold voltage variability.

In order to avoid such a dopant contamination and damage of the channel region through the high dose and/or implantation tail, it has been proposed to implant through the top semiconductor layer and the buried dielectric layer deeply into the carrier substrate. This method, however, requires thermal annealing steps which are essential to diffuse the dopant upwards towards the interface between the carrier substrate and the buried dielectric. Thus it does not become possible to obtain the desired dopant level for circuit optimization.

Furthermore, the active dopant level at the interface between the carrier substrate and the buried dielectric layer cannot be very high, typically smaller than 1.0×10^{19} cm^{-3}. This limits the possibility of using implanted doped patterns to generate a buried circuitry.

It is therefore the object of the present invention to provide an improved method for fabricating a semiconductor substrate, in particular, a semiconductor-on-insulator substrate.

This object is achieved with a method according to claim 1.

Accordingly, the method for manufacturing a semiconductor substrate, in particular, a semiconductor-on-insulator (SOI) substrate, comprises the steps of: a) providing a donor substrate and a handle substrate, b) forming a pattern of one or more doped regions in, in particular inside, the handle substrate, and then c) attaching, in particular by bonding, the donor and the handle substrate to obtain a donor-handle compound.

By forming the pattern of one or more doped regions in the handle substrate prior to attaching the donor and the handle substrate, the creation of tails in other layers of the semiconductor substrate can be suppressed and the formation of doped regions with desired dimensions, dopant level and profiles can be enabled. Further, the negative effects of so called resist edge ion implantation deflection can be suppressed or at least reduced to a level which typically does not have any impact on the dopant profiles. This may help in reducing the dimensions of the circuits on the substrate.

Each of the donor substrate and the handle substrate may be a semiconductor substrate, in particular, a silicon substrate.

Prior to attaching the donor and the handle substrate, the handle and/or the donor substrate may be prepared for bonding, e.g. by cleaning, or any suitable surface treatments.

According to an advantageous realisation, the method may further comprise a step d) carried out between steps a) and b) which consists in forming one or more alignment marks in, in particular inside, the handle substrate. Alignment marks will allow the formation of the pattern at predetermined locations of the handle substrate such that the doped regions can be aligned with corresponding regions in other layers of the substrate in particular in the donor substrate or other doped patterns in the handle substrate.

In this context, the term “inside” means that the alignment marks are buried, typically in a depth of less than about 10µm, such that the surface of the handle substrate is essentially unaffected by the alignment marks.

Further advantage of forming the alignment marks and/or implanting the dopant patterns below the handle substrate surface is that the surface remains essentially unaffected such that the bonding quality of the handle substrate is better compared to the prior art. This invention is independent of the lithography technique utilized. It remains

compatible with the most advanced lithography techniques like immersion, EUV, and e-beam lithography.

In particular, the one or more alignment marks may be formed by ion implantation. In this way, the alignment marks essentially do not alter the surface of the handle substrate as compared to alignment marks formed by filled trenches known in the art. The alignment marks or structures used in the prior art have to be typically planarized using thick dielectric layers and the material mix could even lead to stress inside the material. The use of the prior art may also cause formation of voids at the bonding interface. Thus, whereas the prior art marks could not be combined with thin dielectric layers or semiconductor layers, the ion implanted alignment marks are compatible with thinner buried dielectric layers, for example, having a thickness smaller than 200 nm, in particular smaller than 100 nm, as stress can be prevented and no planarization becomes necessary. The handle substrate surface in the inventive method remains better prepared for bonding.

Further preferred, the one or more alignment marks may comprise a non-dopant species, in particular, hydrogen (H), helium (He), argon (Ar), fluorine (F), neon (Ne) and/or xenon (Xe), or a combination of two or more elements. In particular, argon may be used as it is cheap and commonly used to clean up the beam line of implanters, so that the implementation of the method can be easily achieved.

The alignment marks could, according to a variant, also be achieved using a different technique, e.g. focussed laser melting or focussed ion beam melting.

According to a preferred embodiment, Step d) may comprise a thermal annealing step. By the thermal annealing step, the optical contrast between the alignment marks and surrounding substrate material can be enhanced, i.e. defects like the growth of nano- or micro-cavities may be induced. The position and the shape of the alignment marks remain stable. In this way, a predetermined distribution of the nano- or micro-cavities can be created, locally changing the optical properties of the handle substrate. These can be observed in an alignment tool so that a lithography tool can correctly align the subsequent doped patterns in the handle and/or transferred layer of the donor substrate.

Advantageously, step b) may comprise at least one ion implantation step for implanting a dopant, in particular, phosphorous and/or arsenic and/or boron and/or indium, and/or antimony. Dopant implantation targets the formation of n and p doped regions in the

handle substrate. Thus desired regions with n and/or p type dopant concentrations can be formed within the handle substrate.

The at least one ion implantation step may be followed by an annealing step. In particular, the annealing step may be a thermal annealing step. Annealing can bring the dopants up to the surface.

The method of manufacturing a semiconductor substrate may preferably further comprise a step e) carried out between steps a) and b) which consists in forming a screening layer, in particular, a screening oxide, on the handle substrate. By using a screening layer or sacrificial layer, in particular a screening or sacrificial oxide, the variability related to channelling and substrate surface miss-orientation during the ion implantation can be suppressed.

In a further variant, prior to step c), the screening layer may be removed or stripped.

The method may further comprise a step f) carried out between steps a) and c) which consists in forming a predetermined splitting area at a depth h inside the donor substrate and a step g) carried out after step c) which consists in detaching a remainder of the donor substrate from the donor-handle compound wherein detachment occurs at the predetermined splitting area.

Layers, in particular with a thickness in the range of micrometers, can be transferred onto the handle substrate. With the inventive method, thin layers, in particular with a thickness of less than 400 nm, more in particular less than 200 nm, can be transferred. As the surface of the handle substrate remains essentially unaffected with the inventive method, the bonding quality of the handle substrate is better compared to the prior art.

Forming the predetermined splitting area may comprise an ion implantation step. The depth h of the predetermined splitting area may be determined by the energy of the implanted ions. The implanted ions for forming the predetermined splitting area may be hydrogen or rare gas ions (He, Ar, ...).

The method may further comprise a step h) carried out between steps a) and c) which consists of forming a dielectric layer, in particular, an oxide layer, or a combination of stacked layers comprising at least one dielectric layer on the donor substrate, in particular, wherein the dielectric layer has a thickness of less than 200 nm, in particular less than 100 nm. Thereby, the SOI substrate may be obtained with buried doped re-

gions. This SOI substrate can have a thin dielectric and eventually also a thin top semiconductor layer.

The method according to the invention thus enables to obtain doped regions in the handle substrate and at the same time a contamination of the transferred layer with a doping tail like occurring in the prior art can be prevented.

The dielectric layer may be formed by oxidizing the donor substrate which can be achieved by a thermal process. Alternatively, the dielectric layer can be provided by deposition. In a variant, a dielectric layer may be formed on the handle substrate.

The pattern of one or more doped regions may comprise one or more lines and/or one or more islands. A line may particularly be a straight or curved line, wherein the length of the line is significantly larger than the width of the line.

The pattern of one or more doped regions may comprise at least one well region and/or at least one back gate. Thereby the desired dopant patterns and dopant profiles in depth perpendicular to the handle substrate surface can be better created, wherein due to the fact that the dopant pattern is formed prior to bonding, any dimensions can be achieved. Between the well and back gate formation steps, additional annealing steps can be included.

At least one well region and at least one back gate may be formed using the same mask. This will simplify the process.

The method may further comprise a surface treatment step, in particular, comprising a CMP polishing (chemical-mechanical polishing) of the top semiconductor layer after the detachment step of the semiconductor substrate and/or a cleaning step before and/or after the polishing step.

Advantageously, the surface where the detaching occurred may be treated using an annealing step, in particular, a thermal annealing step. In this way, surface irregularities may be smoothed.

According to another aspect, the object is achieved with a method according to claim 14. Accordingly, the invention provides a method for manufacturing a semiconductor substrate, in particular, a semiconductor-on-insulator (SOI) substrate, comprises the steps of: a) providing a donor substrate and a handle substrate, b) forming one or more

alignment marks in, in particular inside, the handle substrate, and then c) attaching, in particular by bonding, the donor and the handle substrate to obtain a donor-handle compound.

Alignment marks will allow the formation of patterns at predetermined locations of the handle substrate and/or in other layers of the substrate in particular in the donor substrate.

In this context, the term “inside” means that the alignment marks are buried, typically in a depth of less than about 10µm, such that the surface of the handle substrate is essentially unaffected by the alignment marks.

By forming the alignment marks in, in particular inside, the handle substrate, i.e. below the handle substrate surface, the surface remains essentially unaffected such that the bonding quality of the handle substrate is better compared to the prior art. This invention is independent of the lithography technique utilized. It remains compatible with the most advanced lithography techniques like immersion, EUV, and e-beam lithography.

In particular, the alignment marks may be formed such that they essentially do not alter the surface of the handle substrate as compared to alignment marks formed by filled trenches known in the art. The alignment marks or structures used in the prior art have to be typically planarized using thick dielectric layers and the material mix could even lead to stress inside the material. The use of the prior art may also cause formation of voids at the bonding interface. Thus, whereas the prior art marks could not be combined with thin dielectric layers or semiconductor layers, the alignment marks according to the invention are compatible with thinner buried dielectric layers, for example, having a thickness smaller than 200 nm, in particular less than 100 nm, as stress can be prevented and no planarization becomes necessary. The handle substrate surface in the inventive method remains better prepared for bonding.

The method, in particular the step of forming one or more alignment marks, may comprise one or more of the features described above.

The invention further provides a semiconductor substrate comprising a donor-handle compound with one or more alignment marks and/or a pattern of one or more doped regions in the handle substrate.

The one or more alignment marks and/or the pattern of one or more doped regions in the handle substrate may comprise one or more of the above-described features obtained during the various process steps. The semiconductor substrate may particularly

correspond to a donor-handle compound as formed in step c) of the above-described methods.

The semiconductor substrate may further comprise a predetermined splitting area at a depth h inside the donor substrate.

The invention further provides a semiconductor-on-insulator substrate, comprising a substrate layer, a semiconductor layer and a dielectric layer, in particular, an oxide layer, between the substrate layer and the semiconductor layer, wherein the substrate layer comprises one or more alignment marks and/or a pattern of one or more doped regions.

The dielectric layer may correspond to a buried oxide layer (BOX). The one or more alignment marks and/or the pattern of one or more doped regions may comprise one or more of the above-mentioned features obtained during the various process steps.

The pattern of one or more doped regions may be designed and/or arranged such that they do not extend into the semiconductor layer and/or the dielectric layer. In this way, the pattern of one or more doped regions does not alter the characteristics of a device formed on the semiconductor layer by generating a random dopant fluctuation (RDF) which will induce a threshold voltage variability. The threshold voltage variability observed in the art in turn negatively impacts the parameters of integrated circuits causing threshold voltage offset and mismatch. Typical corrective action is to oversize some critical circuit modules in order to compensate for this random variability. Thus, by reducing, in particular essentially eliminating RDF in the inventive substrate, a significant surface area gain is enabled for the integrated circuits. This is even further improved by the reduced resist edge ion implantation deflection effect, described above. Hence, the semiconductor-on-insulator substrate may be used to produce more reproducible devices and more compact and robust circuits.

Advantageous embodiments will be described in combination with the enclosed Figures.

Figs. 1a to 1e illustrate a handle substrate at different steps of an exemplary method for manufacturing a semiconductor substrate according to the invention;

Figs. 2a to 2c illustrate a donor substrate at different steps of an exemplary method for manufacturing a semiconductor substrate according to the invention;

Figs. 3a and 3b illustrate steps of an exemplary method for manufacturing a semiconductor substrate according to the invention; and

Figs. 4a and 4b illustrate an exemplary silicon-on-insulator substrate with inventive dopant profile

In Figs. 1a to 1e, the treatment of a handle substrate 101 according to an exemplary method for manufacturing a semiconductor substrate is shown. In Fig. 1a, a handle substrate 101 is provided.

The handle substrate 101 may be any suitable handle substrate, in particular a silicon wafer. The handle substrate may also be a glass or quartz type substrate.

In Fig. 1b, a screening layer 102, in particular, a screening oxide, is formed on a main surface of the handle substrate 101. Depending on the process, this screening layer 102 might not be necessary.

In the next process step, alignment marks 103a, 103b are formed inside the handle substrate 101. This is achieved by performing an ion implanting through the screening layer 102. In this embodiment the implanting species is a non-dopant specie, for example, argon or fluorine, which are species typically available in a fabrication line.

The result of this step is shown in Figure 1c.

The alignment marks 103a and 103b are formed from a non-dopant specie, i.e. the alignment marks 103a and 103b do not dope the substrate 101. Furthermore, due to the ion implantation process, the alignment marks 103a and 103b do not alter the surface of the handle substrate 101. In other words, the alignment marks 103a and 103b correspond to alignment marks which are buried in the handle substrate 101. Furthermore, the alignment marks 103a and 103b, which relate to defects in the handle substrate, do not diffuse thereby generating stable alignment marks in size and position.

By the ion implantation process, it is possible to generate fine and possibly minimal feature implantation regions, where minimal feature corresponds to the smallest geometry that can be defined with a given lithography technology and reproducible and

reliable alignment marks which are compatible with standard lithography but also with immersion and EUV (extreme ultraviolet) lithography requirements. Indeed, the alignment marks are preferably defined by using a mask formed on top of the screening layer 102. The masking layer may e.g. be patterned by lithography techniques. The implantation step can then be carried out by a full wafer area implantation apparatus.

As a variant of this embodiment, other suitable processes to form the alignment marks inside the handle substrate could be applied, e.g. focussed laser or focussed ion beam techniques.

Modern lithography tools are equipped with alignment tools that can identify the alignment marks, like infra red (IR) alignment lasers which are suited for identifying the buried alignment marks in the handle wafer with nanometric precision.

In Fig. 1d, additionally, a pattern of doped regions 104a, 104b, 104c and 104d is shown. This pattern of doped regions 104a to d has been formed using one or more ion implantation steps. The doped regions may be implanted at different depths. Doped regions 104a and 104d, for example, are implanted at different depths, while doped regions 104b and 104c are partly overlapping.

The doped regions can correspond to n- and/or p-wells and/or n- and/or p- back gates.

The doped region 104a may correspond to an n-well comprising phosphorous as a dopant. The concentration of the dopant may be between 10^{16} and 10^{18} cm^{-3}. There are several options to form such a doped region, for example implantation and diffusion further into the handle substrate but also upwards towards its surface by an annealing step.

Doped region 104b may correspond to a p-well comprising boron as a dopant specie. The concentration of the dopant may lie between 5.0×10^{16} and 5.0×10^{18} cm^{-3}. There are several options to form such a doped region, for example implantation and diffusion further into the handle substrate but also upwards towards its surface by an annealing step.

Doped region 104c may correspond to an N^+ gate, particularly comprising arsenic, and doped region 104d may correspond to a P^+ gate, in particular, comprising boron. Typical process conditions for gate regions are for the N-gate: As doping with an energy in the range of 5 - 50 keV and doses between $5x10^{14}cm^{-2}$ and $5 x10^{15}cm^{-2}$ and for the P-gate:

B doping with an energy in the range of 5 - 50 keV with doses between 5 $x10^{14}cm^{-2}$ and 5 $x10^{15}cm^{-2}$.

Doped regions 104a and 104b may correspond to well regions. Typical process conditions for the well regions are energies in the range of 50 – 100 keV and doses between $5x10^{12}$ cm^{-2} and $1x10^{14}$ cm^{-2}.

After the implantation steps of the buried alignment marks 103a and 103b and the pattern of doped regions 104a to d, a next step consists in removing or stripping the screening oxide 102 from the handle substrate 101. The processed handle substrate without the screening oxide 102 is shown in Fig. 1e.

In Fig. 1e, the pattern of doped regions 104a to d of Fig. 1d has been processed using annealing steps. In this way, diffusion further into the handle substrate 101 but also upwards towards its surface has been achieved.

The pattern of Figure 1e is only for illustrative purposes. Of course, any other arrangement of the various regions can be achieved depending on process conditions.

In Figs. 2a to 2c, a treatment of a donor substrate according to an exemplary method for manufacturing a semiconductor substrate according to the invention is shown. First, a donor substrate 205 is provided in Fig. 2a. The donor substrate 205 can be a semiconductor substrate, in particular one out of a silicon (Si), a silicon carbide, a silicon germanium, a gallium nitride or a germanium substrate.

A dielectric layer 206 is then provided on the donor substrate 205 (see Fig. 2b). The dielectric layer 206 may be formed either by a thermal process or by deposition. For example, the dielectric layer 206 may be at least one out of silicon dioxide, silicon nitride, silicon oxynitride or Al_2O_3, etc. or a combination of stacked layers comprising at least one layer at least one out of silicon dioxide, silicon nitride, silicon oxynitride or Al_2O_3, etc.

According to a variant, the step as illustrated in Figure 2b, may also be omitted, e.g. in case of direct silicon bonding without intervening dielectric layer.

In Fig. 2c, illustrates the result of the next process step consisting in forming a predetermined splitting area 207 inside the donor substrate 205. The predetermined splitting area 207 is formed by an ion implantation step, during which ions like hydrogen or rare

gas ions (helium, argon, etc.) are implanted into the donor substrate 205. The depth h of the predetermined splitting area can be determined by the energy of the implanted ions.

In Figs. 3a and 3b, further steps of the exemplary method for manufacturing a semiconductor substrate according to the invention are shown.

Fig. 3a shows a donor-handle compound 308 obtained by attaching, in particular by bonding, the donor substrate 305 and the handle substrate 301. In particular, the donor-handle compound 308 of Fig. 3a may be formed by attaching a handle substrate from Fig. 1e and a donor substrate from Fig. 2c.

Upon a mechanical and/or thermal treatment, a detachment of a semiconductor layer 310 together with a buried dielectric layer 309 occurs at the predetermined splitting area 307 so that the two layers are transferred onto the handle substrate 301 to obtain the silicon-on-insulator structure as shown in Fig. 3b with buried alignment marks 303a, 303b and doped regions 304a to 304d.

Actually, during a thermal treatment carried out during the detachment step microcavities resulting in the formation of microsplittings or microcracks are not only achieved at the predetermined detachment area 307 leading to the complete detachment but also in the area of the alignment marks. The changed crystallographic properties in these regions can then be exploited to observe the alignment marks during subsequent lithography fabrication steps. As an alternative each ion implantation step may be followed by a dedicated thermal annealing.

In Figure 4a the exemplary semiconductor-on-insulator substrate of Fig. 3b is again shown. A semiconductor layer 410 is provided over a handle substrate 401 with a buried dielectric layer 409 in between. In the handle substrate 401 buried alignment marks 403a, 403b and doped regions 404a to 404d are shown.

In Fig. 4b, the respective dopant concentration profile is illustrated as the solid line 411. It can be seen that the maximum of the dopant concentration, e.g. a gate region is near the interface of the handle substrate 401 and the buried dielectric layer 409. Thanks to implanting prior to bonding, the semiconductor layer 410 is not affected by the high doping concentration in the handle substrate. Below the gate region a second region with a lower dopant concentration, e.g. a well region, can be observed.

For comparison, a typical dopant profile according to the prior art is shown as a dashed line 412. It can be seen that in the profile according to the prior art also a dopant concentration is present in the semiconductor layer 410. This non-zero concentration in the semiconductor layer 410 stems from the implantation tail caused by the implanting through the top semiconductor layer and subsequent anneal steps. At the same time, the maximum dopant concentration at the interface between handle substrate 401 and the buried dielectric layer 409 is reduced compared to the concentration which can be achieved by the inventive method.

In the following, practical examples according to the invention will be described.

According to a first example, argon is used to form buried alignment marks in a handle substrate. The energy for the ion implantation step is between 50 and 250 keV with a dose range of 1 $x10^{14}$ to 5 $x10^{15}$ cm^{-2}. The ion implantation is performed through a sacrificial oxide, which is removed after implantation of all the required implants. Argon is particularly advantageous as it is cheap and available in industrial implanters.

According to a second example, fluorine is used for the buried alignment marks. The energy range may be between 25 and 150 keV at a dose range of 1 $x10^{15}$ to 1 $x10^{16}$ cm^{-2}. Boron trifluoride (BF_3) gas may be used to obtain atomic boron for doping purposes.

According to a 3rd to 5th example, fluorine, neon or xenon may be used for the generation of alignment marks. It is desired to keep the same level and morphology of structural damage as in the case of argon. For example, fluorine may be implanted at 60 keV and a dose of 1 $x10^{16}$ cm^{-2} followed by a thermal annealing step with 700° C for one hour and a 1100° C spike anneal.

After the generation of the buried alignment marks, a P-well and an N-well may be formed using ion implantation using following generic recipes.

P-Well: - For example Boron implantation and anneal. The p well formation can be achieved with just one single implant plus diffusion. But if necessary high energy implants multiple doses and implantation energies can be utilized followed by an annealing step to form the p well region.

N-Well: - for example Phosphorus and/or arsenic, implantation and anneal. The n well formation can be achieved with just one single implant plus diffusion. But if necessary

high energy implants multiple doses and implantation energies can be utilized followed by an annealing step to form the n well region

Buried gates may be formed using the following generic recipes.

N-gate: Arsenic or phosphorus, followed by an activation anneal.

P-gate: Boron or Indium, followed by an activation anneal.

A possible process flow of an exemplary method for manufacturing a semiconductor substrate according to the invention may thus comprise the following subsequent steps:

1) Oxidation or deposition of a screening oxide on handle substrate;

2) Implantation and formation of alignment marks;

3) Implantation of a deep n-well (concentration 10^{16} – 10^{18} at/cm^{-3}), dopant specie e.g. phosphorus;

4) Anneal;

5) Implantation of a p-well (concentration $5x10^{16}$ – $5x10^{18}$ at/cm^{-3}), dopant specie e.g. boron;

6) Anneal;

7) Implantation of the N+ gate, e.g. with arsenic;

8) Anneal;

9) Implantation of the P+ gate, e.g. with boron;

10) Anneal;

11) Strip the screening oxide; and

12) Prepare for bonding with donor substrate.

Alternatively, the well and the respective gate implant both can be done together using the same mask.

By providing alignment marks and dopant regions prior to bonding inside the handle substrate, dopant concentration tails inside the transferred layer 310 and thus in device layers can be prevented and the dopant profiles can be tailored as necessary.

In the above described embodiments and examples, alternatively, only the alignment marks may be provided in the handle substrate. In other words, the pattern of one or more doped regions in the handle substrate may be omitted. The alignment marks may be used for alignment purposes during subsequent process steps affecting the transferred semiconductor and buried dielectric layer. By forming the alignment marks in, in particular inside, the handle substrate, i.e. below the handle substrate surface, the surface remains essentially unaffected such that the bonding quality of the handle substrate is better compared to the prior art.

Although the previously discussed embodiments and examples of the present invention have been described separately, it is to be understood that some or all of the above-described features can also be combined in different ways. The discussed embodiments are not intended as limitations but serve as examples illustrating features and advantages of the invention.

Claims

1. Method for manufacturing a semiconductor substrate, in particular a semiconductor-on-insulator substrate, comprising the steps of:

   a) providing a donor substrate (205; 305) and a handle substrate (101; 201; 301; 401);

   b) forming a pattern of one or more doped regions (104a-d; 304a-d; 404a-d) in, in particular inside, the handle substrate (101; 201; 301; 401); and then

   c) attaching, in particular by bonding, the donor (205; 305) and the handle (101; 201; 301; 401) substrate to obtain a donor-handle compound (308).

2. Method according to claim 1, further comprising a step d) carried out between steps a) and b) which consists in forming one or more alignment marks (103a-b; 303a-b; 403a-b) in, in particular inside, the handle substrate (101; 201; 301; 401).

3. Method according to claim 2, wherein the one or more alignment marks (103a-b; 303a-b; 403a-b) are formed by ion implantation.

4. Method according to claim 2 or 3, wherein the one or more alignment marks (103a-b; 303a-b; 403a-b) comprise a non-dopant species, in particular, H, He, Ar, F, Ne and/or Xe.

5. Method according to one of the claims 2 – 4, wherein step d) comprises a thermal annealing step.

6. Method according to one of the preceding claims, wherein step b) comprises at least one ion implantation step for implanting a dopant, in particular, phosphorus and/or arsenic and/or boron.

7. Method according to claim 6, wherein the at least one ion implantation step is followed by an annealing step.

8. Method according to one of the preceding claims, further comprising a step e) carried out between steps a) and b) which consists in forming a screening layer (102), in particular a screening oxide, on the handle substrate (101; 201; 301; 401).

9. Method according to one of the preceding claims, further comprising a step f) carried out between steps a) and c) which consists in forming a predetermined splitting area (207; 307) at a depth h inside the donor substrate (205; 305) and a step g) carried out after step c) which consists in detaching a remainder of the donor substrate (205; 305) from the donor-handle compound, wherein detachment occurs at the predetermined splitting area (207; 307).

10. Method according to one of the preceding claims, further comprising a step h) carried out between steps a) and c) which consists in forming a dielectric layer (206; 306), in particular an oxide layer, or a combination of stacked layers comprising at least one dielectric layer on the donor substrate (205; 305), in particular, wherein the dielectric layer (206; 306) has a thickness of less than 200 nm, in particular less than 100 nm.

11. Method according to one of the preceding claims, wherein the pattern of one or more doped regions (104a-d; 304a-d; 404a-d) comprises one or more lines and/or one or more islands.

12. Method according to one of the preceding claims, wherein the pattern of one or more doped regions (104a-d; 304a-d; 404a-d) comprises at least one well region and/or at least one back gate.

13. Method according to claim 12, wherein at least one well region and at least one back gate are formed using the same mask.

14. Method for manufacturing a semiconductor substrate, in particular, a semiconductor-on-insulator (SOI) substrate, comprises the steps of:

a) providing a donor substrate and a handle substrate;

b) forming one or more alignment marks in, in particular inside, the handle substrate; and then

c) attaching, in particular by bonding, the donor and the handle substrate to obtain a donor-handle compound.

15. Semiconductor substrate comprising a donor-handle compound (308) with one or more alignment marks (103a-b; 303a-b; 403a-b) and/or a pattern of one or more doped regions (104a-d; 304a-d; 404a-d) in the handle substrate (101; 201; 301; 401).

16. Semiconductor substrate according to claim 15, further comprising a predetermined splitting area (207; 307) at a depth h inside the donor substrate (205; 305).

17. Semiconductor-on-insulator substrate, comprising a substrate layer (301; 401), a semiconductor layer (310; 410) and a dielectric layer (309; 409), in particular an oxide layer, between the substrate layer (301; 401) and the semiconductor layer (310; 410), wherein the substrate layer (301; 401) comprises one or more alignment marks (303a-b; 403a-b) and/or a pattern of one or more doped regions (304a-d; 404a-d).

18. Semiconductor-on-insulator substrate according to claim 17, wherein the pattern of one or more doped regions (304a-d; 404a-d) does not extend into the semiconductor layer (310; 410) and/or the dielectric layer (309; 409).