CLAIMS

1. A semiconductor structure, comprising:

a substrate;

a first gate structure and a second gate structure that are located on a surface of the substrate and have a same thickness; and

a first doped area and a second doped area that are located in the substrate and are located on two sides of the first gate structure respectively, wherein the first gate structure forms a selection transistor with the first doped area and the second doped area;

an orthographic projection of the second gate structure on the substrate is at least partially overlapped with the second doped area; the second gate structure and the second doped area form an antifuse bit structure; and a breakdown state and a non-breakdown state of the antifuse bit structure are configured to represent different stored data respectively;

wherein the semiconductor structure further comprises:

a first metal line, wherein the first metal line is located above the first gate structure and the second gate structure, and is connected with the first doped area through a first connection structure; and

a second metal line, wherein the second metal line is located between the first gate structure and the first metal line, and is connected with the substrate through a second connection structure.

2. The semiconductor structure of claim 1, wherein the first gate structure comprises a first gate electrode and a first gate dielectric layer located below the first gate electrode; the second gate structure comprises a second gate electrode and a second gate dielectric layer located below the second gate electrode; and

the first gate dielectric layer and the second gate dielectric layer have a same thickness, and are of a thin gate oxide structure.

3. The semiconductor structure of claim 1, further comprising:

an isolating structure, located in the substrate between two adjacent antifuse bit structures, wherein at least a portion of the second connection structure is located above the isolating structure.

4. The semiconductor structure of claim 3, further comprising:

a third doped area, located in the substrate on two sides of the isolating structure, wherein the second connection structure is connected with the substrate through the third doped area.

5. The semiconductor structure of claim 1, further comprising:

a word line located above the first gate structure, wherein the word line is connected with a plurality of first gate structures located in an extension direction of the word line;

a third metal line located above the second gate structure, wherein an extension direction of the third metal line is parallel to an extension direction of the word line, and the third metal line is connected with a plurality of second gate structures located in the extension direction of the third metal line.

6. The semiconductor structure of claim 1, wherein two adjacent selection transistors are symmetrically disposed and share a same first doped area.

7. A method for operating a memory, the memory comprising the semiconductor structure of any one of the claims 1-6, and the method comprising:

according to data to be written in, carrying out write-in operation on the memory, wherein the write-in operation comprises:

breaking down a target antifuse bit structure among antifuse bit structures of the memory, to switch the target antifuse bit structure into a breakdown state from a non-breakdown state; and

keeping a non-target antifuse bit structure in the non-breakdown state, wherein the non-target antifuse bit structure is an antifuse bit structure other than the target antifuse bit

structure.

8. The method of claim 7, wherein the write-in operation further comprises:

applying a first voltage to the substrate to keep the non-breakdown state of the selection transistor.

9. The method of claim 7, wherein breaking down the target antifuse bit structure among the antifuse bit structures of the memory to switch the target antifuse bit structure into the breakdown state from the non-breakdown state comprises:

applying a second voltage to a first gate electrode of a selection transistor connected with the target antifuse bit structure so as to switch on the selection transistor connected with the target antifuse bit structure;

applying a third voltage to a first metal line connected with the selection transistor connected with the target antifuse bit structure, wherein a difference between the third voltage and the second voltage is smaller than a breakdown voltage of the first gate dielectric layer; and

applying a fourth voltage to a second gate electrode of the target antifuse bit structure, to switch the target antifuse bit structure into the breakdown state from the non-breakdown state, wherein a voltage difference between the third voltage and the fourth voltage is greater than or equal to a breakdown voltage of the second gate dielectric layer.

10. The method of claim 7, wherein keeping the non-target antifuse bit structure in the non-breakdown state comprises:

applying a second voltage to a first gate electrode of a selection transistor connected with the non-target antifuse bit structure so as to switch on the selection transistor connected with the non-target antifuse bit structure;

applying a first voltage to a first metal line connected with the selection transistor connected with the non-target antifuse bit structure, wherein a difference between the first voltage and the second voltage is smaller than a breakdown voltage of the first gate dielectric layer; and

applying a fourth voltage to a second gate electrode of the non-target antifuse bit structure, to keep the non-target antifuse bit structure in the non-breakdown state, wherein a voltage difference between the first voltage and the fourth voltage is smaller than a breakdown voltage of the second gate dielectric layer.

11. The method of claim 7, wherein keeping the non-target antifuse bit structure in the non-breakdown state comprises:

applying a cut-off voltage to a first gate electrode of a selection transistor connected with the non-target antifuse bit structure so as to cut off the selection transistor connected with the non-target antifuse bit structure;

applying a third voltage to a first metal line connected with the selection transistor connected with the non-target antifuse bit structure, wherein a difference between the third voltage and the cut-off voltage is smaller than a breakdown voltage of the first gate dielectric layer; and

applying a first voltage to a second gate electrode of the non-target antifuse bit structure, to keep the non-target antifuse bit structure in the non-breakdown state, wherein a voltage difference between the third voltage and the first voltage is smaller a breakdown voltage of the second gate dielectric layer.

12. The method of claim 7, further comprising:

carrying out a read operation on the memory, wherein the read operation comprises:

grounding the substrate;

applying a first read voltage to a first gate electrode of a selection transistor connected with one of the antifuse bit structures so as to switch on the selection transistor connected with the one of the antifuse bit structures;

applying a second read voltage to a first metal line connected with the selection transistor connected with the one of the antifuse bit structures; and

detecting a current on the first metal line.

13. A memory, comprising:

a memory array, the memory array comprising the semiconductor structure of any one of the claims 1-6; and

a peripheral circuit coupled to the memory array.