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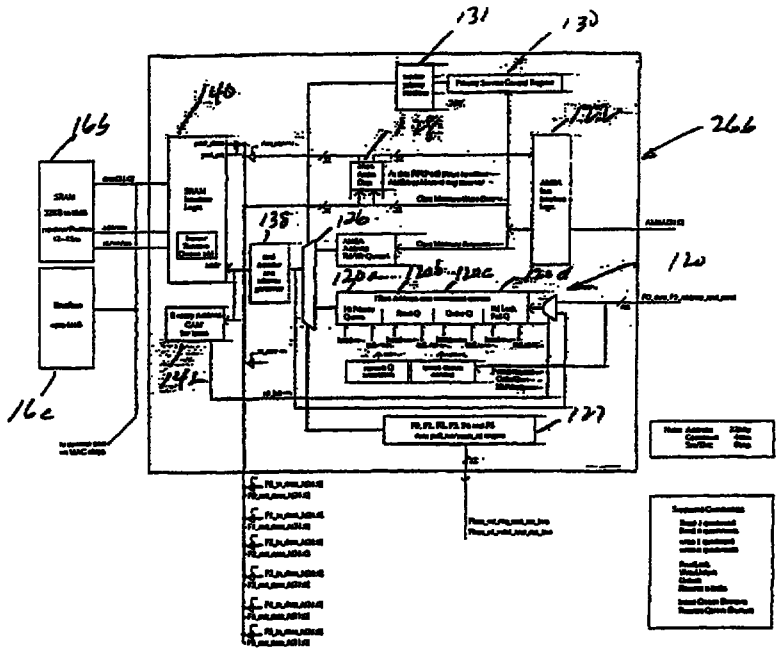
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(54) Title: SRAM CONTROLLER FOR PARALLEL PROCESSOR ARCHITECTURE



(57) Abstract: A controller for a random access memory includes an address and command queue that holds memory references from a plurality of microcontrol functional units. The address and command queue includes a read queue that stores read memory references. The controller also includes a first read/write queue that holds memory references from a core processor and control logic including an arbiter that detects the fullness of each of the queues and a status of completion of outstanding memory references to select a memory reference from one of the queues.

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