CLAIMS

What is claimed is:

1. An apparatus comprising:

switch controller circuitry to control a conduction state of a high side switch and a low side switch in a DC to DC converter which includes an inductor; and

zero crossing logic circuitry comprising phase comparator circuitry, a first clocking circuitry and a second clocking circuitry, each clocking circuitry comprising one or more delay elements,

the zero crossing logic circuitry to monitor a switch node voltage, Vsw, and to determine whether Vsw is greater than a reference, Vref,

the switch controller circuitry to turn off the low side switch if Vsw is greater than Vref while the low side switch is turned on, Vsw greater than Vref corresponding to a negative inductor current through the inductor,

wherein the first clocking circuitry is to receive the switch node voltage and to provide a first clocked signal output and the second clocking circuitry is to receive the reference and to provide a second clocked signal output, the first clocked signal corresponding to Vsw and the second clocked signal corresponding to the reference, and

wherein the phase comparator circuitry is to receive the first clocked signal and the second clocked signal and to provide a digital output that has a first value if Vsw is greater than Vref and a second value otherwise.

2. The apparatus of claim 1, wherein each clocking circuitry corresponds to a ground modulated delay line.

3. The apparatus of claim 1, wherein each clocking circuitry corresponds to a gate modulated delay line.

4. The apparatus of claim 1, wherein the phase comparator circuitry comprises a D flip flop to receive the first clocked signal and the second clocked signal and to provide the digital output that has the first value if Vsw is greater than Vref and the second value otherwise.

5. The apparatus of claim 1, wherein the zero crossing logic circuitry further comprises offset circuitry to adjust a threshold associated with phase comparator circuitry.

6. The apparatus of claim 1, further comprising a freewheeling switch, the switch controller circuitry to turn on the freewheeling switch when a high side switch is off and the low side switch is being turned off.

7. The apparatus of claim 2, wherein the first clocking circuitry and the second clocking circuitry each comprises a delay oscillator.

8. The apparatus of claim 1, further comprising an oscillator to provide a clock input to the first clocking circuitry and the second clocking circuitry, the oscillator comprising a plurality of delay elements.

9. A method comprising:

monitoring, by zero crossing logic circuitry, switch node voltage, Vsw;

determining, by the zero crossing logic circuitry, whether Vsw is greater than a reference, Vref, the zero crossing logic circuitry comprising phase comparator circuitry, a first clocking circuitry and a second clocking circuitry, each clocking circuitry comprising one or more delay elements; and

turning, by switch controller circuitry, off a low side switch if Vsw is greater than Vref while the low side switch is turned on, Vsw greater than Vref corresponding to a negative inductor current through an inductor wherein a DC to DC converter comprises the high side switch, the low side switch and the inductor,

wherein the method further comprising:

receiving, by the first clocking circuitry, the switch node voltage and providing, by the first clocking circuitry, a first clocked signal output; and

receiving, by the second clocking circuitry, the reference and providing, by the second clocking circuitry, a second clocked signal output comprising one or more delay elements, the first clocked signal corresponding to Vsw and the second clocked signal corresponding to Vref through the inductor,

wherein the method further comprising:

receiving by phase comparator circuitry the first clocked signal and the second clocked signal and providing, by the phase comparator circuitry, a digital output that has a first value if Vsw is greater than Vref and a second value otherwise.

10. The method of claim 9, wherein each clocking circuitry corresponds to a ground modulated delay line.

11. The method of claim 9, wherein each clocking circuitry corresponds to a gate modulated delay line.

12. The method of claim 9, further comprising adjusting, by offset circuitry, a threshold associated with the phase comparator circuitry.

13. The method of claim 9, further comprising turning on, by the switch controller circuitry to turn, a freewheeling switch when a high side switch is off and the low side switch is being turned off.

14. The method of claim 9, further comprising providing, by an oscillator, a clock input to the first clocking circuitry and the second clocking circuitry, the oscillator comprising a plurality of delay elements.

15. A system comprising:

DC to DC converter circuitry;

switch controller circuitry to control a conduction state of a high side switch and a low side switch in a DC to DC converter which includes an inductor; and

zero crossing logic circuitry comprising phase comparator circuitry, a first clocking circuitry and a second clocking circuitry, each clocking circuitry comprising one or more delay elements,

the zero crossing logic circuitry to monitor a switch node voltage, Vsw, and to determine whether Vsw is greater than a reference, Vref,

the switch controller circuitry to turn off the low side switch if Vsw is greater than Vref while the low side switch is turned on, Vsw greater than Vref corresponding to a negative inductor current,

wherein the first clocking circuitry is to receive the switch node voltage and to provide a first clocked signal output and the second clocking circuitry is to receive the reference and to provide a second clocked signal output, the first clocked signal corresponding to Vsw and the second clocked signal corresponding to the reference, and

wherein the phase comparator circuitry is to receive the first clocked signal and the second clocked signal and to provide a digital output that has a first value if Vsw is greater than Vref and a second value otherwise.

16. The system of claim 15, wherein each clocking circuitry corresponds to a ground modulated delay line.

17. The system of claim 15, wherein each clocking circuitry corresponds to a gate modulated delay line.

18. The system of claim 15, wherein the phase comparator circuitry comprises a D flip flop to receive the first clocked signal and the second clocked signal and to provide the digital output that has the first value if Vsw is greater than Vref and the second value otherwise.

19. The system of claim 15, wherein the zero crossing logic circuitry further comprises offset circuitry to adjust a threshold associated with the phase comparator circuitry.

20. The system of claim 15, further comprising a freewheeling switch, the switch controller circuitry to turn on the freewheeling switch when a high side switch is off and the low side switch is being turned off.

21. The system of claim 15, further comprising an oscillator to provide a clock input to the first clocking circuitry and the second clocking circuitry, the oscillator comprising a plurality of delay elements.