

CLAIMS:

1. A method, comprising:

forming a build-up layer on an adhesion layer of a carrier, wherein the build-up layer has a topmost surface and a bottommost surface;

pressing more than one semiconductor die into the build-up layer, wherein each semiconductor die has a topmost surface and a bottommost surface, wherein each semiconductor die having been previously functionally tested and having wide pads to facilitate the testing, wherein, at least some of the wide pads on a same die are spaced apart a minimal distance permitted by said die's manufacturing process, wherein the bottommost surface of the build-up layer is below the topmost surface of each die, and wherein each wide pad is recessed into the die to have the topmost surface lower than the topmost surface of the die;

forming a mold over the more than one semiconductor die;

detaching the build-up layer from the carrier;

removing the build-up layer over the at least some of the wide pads to form via openings over the at least some of the wide pads;

forming a metallization layer on the build-up layer, the metallization layer substantially filling the via openings; and

patterning the metallization to form lands over the filled via openings and more than one wire between respective lands of the at least some of the wide pads.

2. The method of claim 1 further comprising raising the atmospheric pressure around the semiconductor die and build-up layer after the pressing to better fill voids in recessed regions on a die's surface where the die's pads are located.

3. The method of claim 1 further comprising hardening the build-up layer after the forming of the mold.

4. The method of claim 1 wherein the wide pads are each approximately 40 μm across.
5. The method of claim 1 further comprising forming solder balls or C4 balls on the lands.
6. The method of claim 1 wherein the removing of the build-up layer includes use of a laser.
7. An apparatus, comprising:

a build-up layer having a topmost surface, a bottommost surface, and a pad side of multiple die pressed into a bottom side of the build-up layer, wherein each die has a topmost surface and a bottommost surface, wherein the multiple die having wide pads to facilitate on wafer testing of the multiple die, the wide pads spaced a minimum distance permitted by a manufacturing process used to manufacture their respective die, the build-up layer being removed above the wide pads, wherein the bottommost surface of the build-up layer is below the topmost surface of each die, and wherein each wide pad is recessed into the die to have the topmost surface lower than the topmost surface of the die;

metallization on a top side of the build-up layer and substantially filling regions above the wide pads, the metallization including lands above the wide pads and multiple wires between the wide pads.
8. The apparatus of claim 7 wherein the wide pads exhibit scarring from testing of the die prior to their being packaged with the build-up layer and metallization.
9. The apparatus of claim 7 wherein a bottom region of the metallization in contact with the wide pads has a width sufficient to withstand a maximum rated current flow through said wide pads.

10. The apparatus of claim 9 wherein a thickness of the build-up layer provides for said width in view of tapering along sidewalls of said build-up layer around said regions.
11. The apparatus of claim 7 wherein said build-up layer is selected from the group consisting of: polyimide; epoxy; acrylic; a low k material; silicone; PBO.
12. The apparatus of claim 7 further comprising dielectric formed over the buildup layer and the metallization.
13. The apparatus of claim 12 further comprising openings formed in the dielectric above the lands and solder balls or C4 balls formed on the lands.
14. A system, comprising:
 - a planar board,
 - a multi-chip module affixed to the planar board, the multi-chip module comprising:
 - a build-up layer having a pad side of multiple die pressed into a bottom side of the buildup layer, wherein each die has a topmost surface and a bottommost surface, wherein the multiple die having wide pads to facilitate on wafer testing of the multiple die, the wide pads spaced a minimum distance permitted by a manufacturing process used to manufacture their respective die, the buildup layer being removed above the wide pads, wherein the bottommost surface of the build-up layer is below the topmost surface of each die, and wherein each wide pad is recessed into the die to have the topmost surface lower than the topmost surface of the die;
 - metallization on a top side of the build-up layer and substantially filling regions above the wide pads, the metallization including lands above the wide pads and multiple wires between the wide pads.
15. The system of claim 14 wherein the wide pads exhibit scarring from testing of the die prior to their being packaged with the build-up layer and metallization.

16. The system of claim 14 wherein the wide pads exhibit scarring from testing of the die prior to their being packaged with the build-up layer and metallization.
17. The system of claim 14 wherein a bottom region of the metallization in contact with the wide pads has a width sufficient to withstand a maximum rated current flow through said wide pads.
18. The system of claim 14 wherein said system is a computing system.
19. The system of claim 18 wherein said computing system is any of: an intelligent device; a smartphone; a tablet computer; a laptop computer; a desktop computer; a server computer;
20. The apparatus of claim 14 wherein said system is a networking system.
21. A method, comprising:
forming a build-up layer on an adhesion layer of a carrier;
pressing more than one semiconductor die into the build-up layer, each semiconductor die having been previously functionally tested and having wide pads to facilitate the testing, wherein, at least some of the wide pads on a same die are spaced apart a minimal distance permitted by said die's manufacturing process, wherein the bottommost surface of the build-up layer is below the topmost surface of each die, and wherein each wide pad is recessed into the die to have the topmost surface lower than the topmost surface of the die;
forming a mold over the more than one semiconductor die;
detaching the build-up layer from the carrier;
removing the build-up layer over the at least some of the wide pads to form via openings over the at least some of the wide pads;
forming a metallization layer on the build-up layer, the metallization layer substantially filling the via openings; and
patterning the metallization to form lands over the filled via openings and more than one wire between respective lands of the at least some of the wide pads, wherein at least one or more wires are spaciouly formed between a land of a first die and another land of a second die.