METHODS FOR MAKING NEARLY PLANAR DIELECTRIC FILMS IN INTEGRATED CIRCUITS

Related Application

This application is a continuation of U.S. Provisional Application 60/187,658, which was filed on March 7, 2000 and which is incorporated herein by reference.

Technical Field

The present invention concerns methods of making integrated circuits, particularly methods of making metal masks and dielectric, or insulative, films.

Background of the Invention

Integrated circuits, the key components in thousands of electronic and computer products, are interconnected networks of electrical components fabricated on a common foundation, or substrate. Fabricators typically build the circuits layer by layer, using techniques, such as doping, masking, and etching, to form thousands and even millions of microscopic resistors, transistors, and other electrical components on a silicon substrate, known as a wafer. The components are then wired, or interconnected, together to define a specific electric circuit, such as a computer memory.

One important concern during fabrication is flatness, or planarity, of various layers of the integrated circuit. For example, planarity significantly affects the accuracy of a photo-imaging process, known as photomasking or photolithography, which entails focusing light on light-sensitive materials to define specific patterns or structures in a layer of an integrated circuit. In this process, the presence of hills and valleys in a layer forces various regions of the layer out of focus, causing photo-imaged features to be smaller or larger than intended. Moreover, hills and valleys can reflect light undesirably onto other regions of a layer and add undesirable features, such as notches, to desired features. These problems can be largely avoided if the layer is sufficiently planar.

One process for making surfaces flat or planar is known as chemical-mechanical planarization or polishing. Chemical-mechanical planarization

typically entails applying a fluid containing abrasive particles to a surface of an integrated circuit, and polishing the surface with a rotating polishing head. The process is used frequently to planarize the insulative, or dielectric, layers that lie between layers of metal wiring in integrated circuits. These insulative layers, which typically consist of silicon dioxide, are sometimes called intermetal dielectric layers. In conventional integrated-circuit fabrication, planarization of these layers is necessary because each insulative layer tends to follow the hills and valleys of the underlying metal wiring, similar to the way a bed sheet follows the contours of whatever it covers. Thus, fabricators generally deposit an insulative layer much thicker than necessary to cover the metal wiring and then planarize the insulative layer to remove the hills and valleys.

Unfortunately, conventional methods of forming these intermetal dielectric layers suffer from at least two problems. First, the process of chemical-mechanical planarization is not only relatively costly but also quite time consuming. And second, the thickness of these layers generally varies considerably from point to point because of underlying wiring. Occasionally, the thickness variation leaves metal wiring under a layer too close to metal wiring on the layer, encouraging shorting or crosstalking. Crosstalk, a phenomenon that also occurs in telephone systems, occurs when signals from one wire are undesirable transferred or communicated to another nearby wire.

Accordingly, the art needs fabrication methods that reduce the need to planarize intermetal dielectric layers, that reduce thickness variation in these layers, and that improve their electrical properties generally.

Summary of the Invention

To address these and other needs, the inventor devised various methods of making dielectric layers on metal layers, which reduce the need for chemical-mechanical planarization procedure. Specifically, a first exemplary method of the invention forms a metal layer with a predetermined maximum feature spacing and then uses a TEOS-based (tetraethyl-orthosilicate-based) oxide deposition procedure to form an oxide film having nearly planar or quasi-planar characteristics. The exemplary method executes a CVD (chemical vapor deposition) TEOS oxide procedure to form an oxide layer on a metal layer having a maximum feature spacing of 0.2-0.5 microns.

A second exemplary method includes voids within the oxide, or more generally insulative, film to improve its effective dielectric constant and thus improve its ability to prevent shorting and crosstalk between metal wiring. Specifically, the exemplary method uses a TEOS process at a non-conformal rate sufficient to encourage the formation of voids, and then uses the TEOS process at a conformal rate of deposition to seal the voids. More generally, however, the invention uses a non-conformal deposition procedure to encourage formation of voids and then a more conformal deposition to seal the voids.

A third exemplary method increases the metal-fill density of metal patterns to facilitate formation of intermetal dielectric layers having more uniform thicknesses. The third exemplary method adds floating metal to open areas in a metal layout and then extends non-floating metal dimensions according to an iterative procedure that entails filling in notches, and corners and moving selected edges of the layout.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of a partial integrated-circuit assembly 10 including a substrate 12 and metal wires 14a, 14b, and 14c;

Figure 2 is a cross-sectional view of the Figure 1 integrated-circuit assembly after formation of a substantially planar insulative layer 16, including a portion 16a with voids and a portion 16b without voids;

Figure 3 is a cross-sectional view of the Figure 2 assembly after a facet etch to improve the planarity of layer 16;

Figure 4 is a cross-sectional view of the Figure 3 assembly after formation of metal wires 18a and 18b, and substantially planar insulative layer 20, including a portion 20a with voids and a portion 20b without voids;

Figure 5 is a cross-sectional view of a partial integrated-circuit assembly 21 including a substrate 22 and metal wires 24a, 24b, and 24c;

Figure 6 is a cross-sectional view of the Figure 5 assembly after formation of an oxide spacer 26 and a substantially planar insulative layer 28, including a portion 28a with voids and a portion 28b without voids;

Figure 7 is a cross-sectional view of the Figure 6 assembly after a facet etch to improve the planarity of layer 28;

Figure 8 is a cross-sectional view of the Figure 7 assembly after formation of metal wires 30a and 30b, and substantially planar insulative layer 34, including a portion 34a with voids and a portion 34b without voids;

Figure 9 is a cross-sectional view of a partial integrated-circuit assembly 35 including a substrate 36 and metal wires 36a, 36b, and 36c;

Figure 10 is a cross-sectional view of the Figure 9 assembly after formation of an oxide spacer 40 and a substantially planar insulative layer 42;

Figure 11 is a flow chart illustrating an exemplary method of modifying a metal layout to facilitate fabrication of intermetal dielectric layers with more uniform thickness;

Figure 12 is a partial top view of a metal layout showing how the exemplary method of Figure 11 adds metal to open areas in a metal layout;

Figure 13 is a partial top view of a metal layout showing how the exemplary method of Figure 11 fills notches in a metal layout;

Figure 14 is a partial top view of a metal layout showing how the exemplary method of Figure 11 fills corners in a metal layout;

Figure 15 is a partial view of a metal layout showing how the exemplary method of Figure 11 fills in between opposing edges of live metal regions in a metal layout;

Figure 16 is a partial view of a metal layout showing how the exemplary method of Figure 11 moves edges;

Figure 17 is a block diagram of an exemplary computer system 42 for hosting and executing a software implementation of the exemplary pattern-filling method of Figure 11; and

Figure 18 is a simplified schematic diagram of an exemplary integrated memory circuit 50 that incorporates one or more nearly planar intermetal dielectric layers and/ or metal layers made in accord with exemplary methods of the invention.

Description of the Preferred Embodiments

The following detailed description, which references and incorporates the above-identified Figures, describes and illustrates specific embodiments of the invention. These embodiments, offered not to limit but only to exemplify and teach the invention, are shown and described in sufficient detail to enable those

skilled in the art to implement or practice the invention. Thus, where appropriate to avoid obscuring the invention, the description may omit certain information known to those of skill in the art.

First Exemplary Method of Forming Nearly Planar Dielectric Films

Figures 1-4 show a number of exemplary integrated-circuit assemblies, which taken collectively and sequentially, illustrate an exemplary method of making nearly planar or quasi planar dielectric films, or layers, within the scope of the present invention. As used herein, a quasi planar film is globally planar with local nonplanarities having slopes less than or equal to 45 degrees and depths less than the thickness of the next metal layer to be deposited. The local nonplanarities typically occur over the gaps between underlying metal features.

The method, as shown in Figure 1, a cross-sectional view, begins with formation of an integrated-circuit assembly or structure 10, which can exist within any integrated circuit, for example, an integrated memory circuit. Assembly 10 includes a substrate 12. The term "substrate," as used herein, encompasses a semiconductor wafer as well as structures having one or more insulative, semi-insulative, conductive, or semiconductive layers and materials. Thus, for example, the term embraces silicon-on-insulator, silicon-on-sapphire, and other advanced structures.

Substrate 12 includes three representative wires or conductive structures 14a, 14b, and 14c, with a maximum (or average) feature spacing 14s. In the exemplary embodiment, wires 14a-14c are approximately 3000-6000 angstroms thick and comprise metals, such as aluminum, gold, or silver, and nonmetals, such as heavily doped polysilicon. Spacing 14s, in the exemplary embodiment, is 0.3 microns.

Wires 14a-14c can be formed using any number of methods, for example, photolithography and dry etching. To avoid increasing feature spacing during dry etching, the exemplary embodiment forms a lateral-etch-resistant layer, that is, a layer resistant to lateral etching, on a metal layer before etching. Examples of suitable layers include a TEOS, oxide-nitride layer. Alternatively, one can add extensive serif features to the metal mask layout to avoid large open areas, especially to reduce the diagonal distance between features.

Figure 2 shows that the exemplary method next entails forming an insulative layer 16 over substrate 12 and wires 14a-14b. Layer 16 has a thickness 16t of, for example, 6000 angstroms, and includes two layers or sublayers 16a and 16b. Sublayer 16a includes a number of voids, particularly voids 17 between wires 14a and 14b, and between wires 14b and 14c, to increase its dielectric constant. Sublayer 16b is either substantially voidless or includes a substantially fewer number of voids than sublayer 16a. The presence of voids in sublayer 16a reduces lateral electrical coupling between adjacent metal features, for example, between wires 14a and 14b and between wires 14a-14c and any overlying conductive structures.

The exemplary method forms layer 16 using a combination of a non-conformal and conformal oxide depositions. In particular, it uses a CVD TEOS (chemical vapor deposition tetraethyl-orthosilicate) or PECVD TEOS (plasma-enhanced CVD TEOS) oxide deposition process at a non-conformal deposition rate to form void-filled sublayer 16a voids and then lowers the TEOS deposition rate to, a conformal rate to form substantially voidless sublayer 16b.

Figure 3 shows that after forming sublayer 16b, which includes some level of nonplanarity, the exemplary method facet etches the sublayer at an angle of about 45 degrees to improve its global planarity. (That layer 16b has undergone further processing is highlighted by its new reference numeral 16b'.) The facet etch reduces or smooths any sharp trenches in regions overlying gaps between metal features, such as wires 14a-14c. As used herein, the term "facet etch" refers to any etch process that etches substantially faster in the horizontal direction than in the vertical direction. Thus, for example, the term includes an angled sputter etch or reactive- ion etch.

To optimize the slopes of any vias, one can perform the facet etch before via printing. More specifically, one can facet etch after etching any necessary vias and stripping photoresist to produce vias having greater slope and smoothness.

Figure 4 shows the results of forming a second metallization level according to the procedure outlined in Figures 1-3. In brief, this entails forming conductive structures 18a and 18b on insulative sublayer 16b' and forming an insulative layer 20 on sublayer 16b' and conductive structures 18a and 18b.

Insulative layer 20, like insulative layer 16, includes void-filled sublayer 20a and substantially void-free sublayer 20b'. Sublayer 20a includes one or more voids 19 between conductive structures 18a and 18b. Sublayer 20b' was facet etch to improve its planarity. Layer 20 has a thickness 20t, of for example 3000-6000 angstroms.

Second Exemplary Method of Forming Nearly Planar Dielectric Films

Figures 5-8 show a number of exemplary integrated-circuit assemblies, which taken collectively and sequentially, illustrate a second exemplary method of making nearly planar or quasi planar dielectric layers within the scope of the present invention. The second method is particularly applicable to maximum metal feature spacing greater than about 0.3 microns or oxide thickness less than 6000 angstroms to allow for shallow via formation, that is, via depths less than about 4000 angstroms.

More particularly, Figure 5 shows that the method begins with formation of an integrated-circuit assembly or structure 21, which, like assembly 10 in Figure 1, can exist within any integrated circuit. Assembly 10 includes a substrate 22 which supports three representative wires or conductive structures 24a, 24b, and 24c, with a desired feature spacing 24s. In the exemplary embodiment, spacing 24s is greater than 0.3 microns. Some embodiments set a minimum spacing of 0.17 microns. However, the present invention is not limited to any particular spacing.

Figure 6 shows that the exemplary method next entails forming an insulative spacer 26 and an insulative layer 28. Insulative spacers 26, which consists of silicon dioxide for example, lies over portions of substrate 22 adjacent wires 24a-24c to reduce the effective separation of wires 24a-24c. The exemplary method uses a TEOS oxide deposition and subsequent etching to form spacers 26. Insulative layer 28 has a thickness 28t of, for example, 4000 angstroms, and includes two sublayers 28a and 28b, analogous to sublayers 16a and 16b in the first embodiment. Specifically, sublayer 28a includes a number of voids 27 between the wires to increase its dielectric constant, and sublayer 28b is either substantially voidless or includes a substantially fewer number of voids than sublayer 28a. A two-stage TEOS oxide deposition process, similar to that used in the first embodiment, is used to form layer 28.

Figure 7 shows that after forming sublayer 28b, which includes some level of nonplanarity, the exemplary method facet etches the sublayer at an angle of about 45 degrees to improve its global planarity.

Figure 8 shows the results of forming a second metallization level according to the procedure outlined in Figures 5-7. This entails forming conductive structures 30a and 30b on insulative sublayer 28b' and forming an insulative spacer 32 and an insulative layer 34, which, like insulative layer 28, includes void-filled sublayer 34a and substantially void-free sublayer 34b'. Sublayer 34a includes voids 31 between conductive structures 30a and 30b, and sublayer 34b' is facet etched to improve its planarity.

Third Exemplary Method of Forming Nearly Planar Dielectric Films

Figures 9 and 10 show a number of exemplary integrated-circuit assemblies, which taken collectively and sequentially, illustrate a third exemplary method of making nearly planar or quasi planar dielectric layers within the scope of the present invention. In contrast to the first and second embodiment, the third exemplary embodiment is intended for forming insulative films on metal layers with maximum feature spacing up to about 0.5 microns.

Figure 9 shows that the method begins with formation of an integrated-circuit assembly or structure 35, which like assembly 10 in Figure 1 and assembly 21 in Figure 5, can exist within any integrated circuit. Assembly 35 includes a substrate 36 which supports three representative wires or conductive structures 38a, 38b, and 38c, with a desired feature spacing 38s of about 0.5 microns.

Figure 10 shows the results of forming an oxide spacers 40 and an insulative layer 42. The exemplary embodiment forms one or more oxide spacers 40 which is about 1000 angstroms wide, and thus reduces the effective spacing between conductors 38a-38c by 2000 angstroms. Forming insulative layer 42 entails executing a flow-fill procedure, such as TRIKON-200 by Trikon Technologies, Inc. To obtain global and local planarity, one can reduce the maximum feature space by using oxide/TEOS spacer as taught in the second exemplary method, or by enlarging the metal feature, or by adding floating metal between the metal features.

Exemplary Method of Promoting Uniform Thickness of Intermetal Dielectric Layers

To facilitate the formation of more uniformly thick inter-metal dielectric layers, such as those described above, the inventor developed specific methods of (and related computer software) for increasing the pattern density of metal layouts. The methods and associated software take a given metal layout and modify, or fill, open areas of the layout to increase pattern density and thus promote uniform thickness or reduce thickness variation across dielectric layers formed on metal layers based on the layouts. These methods and software can thus be used, for example, to facilitate formation of the conductive structures shown in Figures 1, 5, and 9.

The exemplary method generally entails iteratively measuring a given layout, adding floating metal to fill large open areas in the layout, and extending or filling out existing metal areas to meet maximum feature spacing, or gap, criteria. Figure 11 shows a flow chart of the exemplary method, which is suitable for implementation as a computer-executable program.

Specifically, the flow chart includes a number of process or decision blocks 110, 120, 130, and 140. The exemplary method begins at process block 110 which entails measuring a given layout. This entails determining open (unmetallized or nonconductive) areas large enough to be filled with floating metal and identifying live metal areas that require additional metal to obtain desired spacing. Floating metal is metal that is not coupled to a signal path or component, whereas live metal is metal that is coupled to a signal path or component.

After executing block 110, the exemplary method proceeds to block 120 which entails adding floating metal to any large areas identified in block 110.

To illustrate, Figure 12 shows a hypothetical layout having a live metal region 200 with open area 210. In general, if dimension A is greater than the sum of dimension S1, dimension S2, and L (the maximum feature spacing criteria), the exemplary method adds floating metal, such as floating metal region 220.

After adding floating metal, the exemplary method adds live metal as indicated in block 120 of Figure 11. Figure 12 is again instructive of the

exemplary method. If dimension B is less than the sum of dimension S1, dimension S2, and L, the exemplary method adds metal as indicated by added active metal region 230.

process block 104 which entails filling in notches in the layout.

More particularly, the exemplary method follows an iterative process for adding live (or non-floating) metal, as indicated by blocks 130a-130g.

Block 130a entails filling notches in the current live metal. Figure 13 shows a live metal region 300 of a hypothetical metal layout having a notch 310. Included within notch 310 are a series of iteratively added live metal regions 320-325. The amount of metal added at each iteration can be selected using a minimum surface area criteria or computed dynamically each iteration. The exemplary embodiment repeatedly adds metal to the notch until it is filled, before advancing to block 310b. However, other embodiments can advance to block 310b before the notch is filled, relying on subsequent trips or iterations through the first loop in the flowchart to complete filling of the notch.

Block 130b entails filling in corners in the current live metal, meaning the live metal after filling notches. Figure 14 illustrates a live metal region 400 having a corner 410 and added L-shaped live metal regions 420-423 and a rectangular live metal region 424. (Other embodiments add other shapes of live metal regions.) The amount of metal added at each iteration can be selected using a minimum surface area or single-dimensional criteria or computed dynamically each iteration. The exemplary embodiment repeatedly adds metal to the corner until it is filled, before advancing to block 130c. However, other embodiments can advance to block 310b before the notch is filled, relying on subsequent trips through the inner loop to complete filling of the notch.

Block 130c entails filling in between opposing edges of adjacent live metal regions to achieve a desired spacing, such as a maximum desired spacing L. Figure 15 shows live metal regions 510 and 520, which have respective opposing edges 510a and 520a. The exemplary method entails adding live metal regions, such as live metal regions 521-523, one edge such as edge 520a to achieved the maximum desired spacing L. However, other embodiments add live metal to both of the opposing edges to achieve the desired spacing. Still other embodiments look at the lengths of the opposing edges and use one or both

of the lengths to determine one or more dimensions of the added live metal regions.

After filling in between opposing edges of existing live metal regions, the exemplary method advances to decision block 130d in Figure 11. This block entails determining whether more live metal can be added. More precisely, this entails measuring the layout as modified by the live metal already added and determining whether there are any adjacent regions that violate the desired maximum spacing criteria. (Note that some exemplary embodiments include more than one maximum spacing criteria to account for areas where capacitive effects or crosstalk issues are of greater importance than others.) If the determination indicates that more metal can be added execution proceeds back to block 130a to fill in remaining notches, and so forth. If the determination indicates that no more live metal can be added to satisfy the maximum spacing criteria, execution to proceeds to block 130e in Figure 11.

Block 130e entails moving (or redefining) one or more edges (or portions of edges) of live metal regions in the modified layout specification. To illustrate, Figure 16 shows live metal regions 610 and 620, which have respective edges 610a and 620a. It also shows the addition of live metal region 630 to edge 620a, which effectively extends the edge. Similarly, edge 620a has been extended with the iterative addition of live metal regions 631 and 632. The additions can be made iteratively using a dynamic or static step size, or all it once by computing the size of an optimal addition to each edge. Exemplary execution then proceeds to decision block 130f.

In decision block 130f, the exemplary method decides again whether more metal can be added to the layout. If more metal can be added, the exemplary method repeats execution of process blocks 104-122. However, if no metal can be added, the method proceeds to process block 140 to output the modified layout for use in a fabrication process.

Although not show explicitly in the exemplary flow chart in Figure 11, the exemplary method performs data compaction to minimize or reduce the amount of layout data carried forward from iteration to iteration. Data compaction reduces the number of cells which define the circuit associated with the metal layout and the computing power necessary to create the metal layout.

The exemplary compaction scheme flattens all array placement into single instance placements. For example, a single array placement of a cell incorporating a 3x4 matrix flattens to 12 instances of a single cell. It also flattens specific cells, such as array core cells, vias, or contacts, based on layout or user settings. Additionally, it flattens cells which contain less than a predetermined number of shapes regardless of any other effects. For example, one can flatten cells having less than 10, 20, or 40 shapes. Lastly, the exemplary compaction scheme attempts to merge shapes to minimize overlapping shapes and redundant data.

The appropriate or optimum degree of flattening depends largely on the processing power and memory capabilities of the computer executing the exemplary method. Faster computers with more core memory and swap space can handle larger number of shapes per cell and thus have less need for flattening than slower computers with less core memory and swap space. In the extreme, a complete circuit layout can be flattened into one cell.

If a given layout design is not a single flat list of shapes but includes two or more cells placed into each other as instances, additional precaution should be taken to reduce the risk of introducing unintended shorts into the layout during the pattern- fill process. In the exemplary embodiment, this entails managing the hierarchy of cells.

The exemplary embodiment implements a hierarchy management process which recognizes that each cell has an associated fill area that will not change throughout the metal-fill process. The exemplary management process entails executing the following steps from the bottom up until all cell dependencies are resolved. For each instance in each cell, the process creates a temporary unique copy of the cell associated with a given instance. After this, the process copies metal from other cells into the cell being examined if it falls into the fill area. The process then copies metal from other cell into the cell if the metal falls into a ring around the fill area. Next, the process identifies, extracts, and marks conflict areas.

This exemplary pattern-filling method and other simpler or more complex methods embodying one or more filling techniques of the exemplary embodiment can be used in combination with the methods of making nearly

planar intermetal dielectric layers described using Figures 1-10. More precisely, one can use a pattern-filling method according to the invention to define a layout for a particular metal layer, form a metal layer based on the layout, and then form a nearly planar intermetal dielectric layer according to the invention on the metal layer. The combination of these methods promises to yield not only a nearly planar dielectric layer that reduces or avoids the need for chemical-mechanical planarization, but also a dielectric layer with less thickness deviation because of the adjusted pattern fill density of the underlying metal layer.

Exemplary Computer System Incorporating Pattern-Filling Method

Figure 17 shows an exemplary computer system or workstation 42 for hosting and executing a software implementation of the exemplary pattern-filling method. The most pertinent features of system 42 include a processor 44, a local memory 45 and a data-storage device 46. Additionally, system 42 includes display devices 47 and user-interface devices 48. Some embodiments use distributed processors or parallel processors, and other embodiments use one or more of the following data-storage devices: a read-only memory (ROM), a random-access-memory (RAM), an electrically-erasable and programmable-read-only memory (EEPROM), an optical disk, or a floppy disk. Exemplary display devices include a color monitor, and exemplary user-interface devices include a keyboard, mouse, joystick, or microphone. Thus, the invention is not limited to any genus or species of computerized platforms.

Data-storage device 46 includes layout-development software 46a, pattern-filling software 46b, an exemplary input metal layout 46c, and an exemplary output metal layout 46d. (Software 46a and 46b can be installed on system 42 separately or in combination through a network-download or through a computer-readable medium, such as an optical or magnetic disc, or through other software transfer methods.) Exemplary storage devices include hard disk drives, optical disk drives, or floppy disk drives. In the exemplary embodiment, software 46b is an add-on tool to layout-development software 46a and layout 46c was developed using software 46a. However, in other embodiments, software 46b operates as a separate application program and layout 46c was developed by non-resident layout-development software. General examples of suitable layout-development software are available from Cadence and Mentor

Graphics.. Thus, the invention is not limited to any particular genus or species of layout-development software.

Exemplary Integrated Memory Circuit

Figure 18 shows an exemplary integrated memory circuit 50 that incorporates one or more nearly planar intermetal dielectric layers and/or metal layers within the scope of the present invention. One more memory circuits resembling circuit 50 can be used in a variety of computer or computerized systems, such as system 42 of Figure 17.

Memory circuit 50, which operates according to well-known and understood principles, is generally coupled to a processor (not shown) to form a computer system. More particularly, circuit 50 includes a memory array 52, which comprises a number of memory cells 53a, 53b, 53c, and 53d; a column address decoder 54, and a row address decoder 55; bit lines 56a and 56b; word lines 57a and 57b; and voltage-sense-amplifier circuit 58 coupled in conventional fashion to bit lines 56a and 56b. (For clarity, Figure 18 omits many conventional elements of a memory circuit.)

Conclusion

In furtherance of the art, the inventor has presented several methods for making nearly planar intermetal dielectric layers without the use of chemical-mechanical planarization. Additionally, the inventor has presented a method of modifying metal layouts to facilitate formation of dielectric films with more uniform thickness. These methods of modifying metal layouts and making dielectric layers can be used in sequence to yield nearly planar intermetal dielectric layers with more uniform thickness.

The embodiments described above are intended only to illustrate and teach one or more ways of practicing or implementing the present invention, not to restrict its breadth or scope. The actual scope of the invention, which embraces all ways of practicing or implementing the invention, is defined only by the following claims and their equivalents.

Claims

1. A method of forming a nearly planar dielectric film on a metal layer, comprising:

forming a metal layer having a predetermined maximum feature spacing;

forming an oxide layer on the metal layer using a TEOS-based procedure;

facet-etching the oxide layer; and

reflowing at least a portion of the oxide layer.

2. The method of claim 1, wherein forming the metal layer comprises forming metal layer with a maximum feature spacing of 0.3 microns.

3. The method of claim 1, wherein forming the metal layer comprises forming metal runners and wherein forming the oxide layer forms oxide on one or more sidewalls of the metal runners.

4. The method of claim 1, wherein forming the oxide layer comprises forming a portion of the oxide layer using a TEOS-based procedure at a first deposition rate and forming a portion of the oxide layer using a TEOS-based procedure at a second deposition rate which is less than the first deposition rate.

5. The method of claim 1, wherein forming the oxide layer comprises forming a portion of the oxide layer using a TEOS-based procedure at a first deposition rate having a tendency to form voids and forming a portion of the oxide layer using a TEOS-based procedure at a second deposition rate having a tendency to form substantially no voids or fewer voids than the first deposition rate.

6. The method of claim 1, further comprising facet etching the oxide layer to reduce severity of any trenches in oxide layer overlying gaps between metal features in the metal layer.

7. A method of forming a nearly planar dielectric film on a metal layer, comprising:

forming a metal layer having a predetermined maximum feature spacing of no more than about 0.3 microns;

forming a first oxide layer using a TEOS-based procedure at a first deposition rate on the metal layer;

forming a second oxide layer on the first oxide layer using a TEOS-based procedure at a second deposition rate which is less than the first deposition rate; and

facet etching the second oxide layer.

8. The method of claim 7, further comprising:

depositing a film resistant to lateral etching on the metal layer.

9. The method of claim 8, further comprising:

forming two or more oxide spacers on two or more metal features of the metal layer to provide an effective space less than about the predetermined maximum feature spacing between two or more oxide spacers.

10. The method of claim 7, wherein the first deposition rate has a tendency to form voids and the second deposition rate has lesser tendency to form voids than the first deposition rate.

11. The method of claim 7, further comprising facet etching the second oxide layer to reduce severity of any trenches in the second oxide layer that overly gaps between metal features in the metal layer.

12. A method of making nearly planar dielectric films on a metal layer, where maximum feature spacing cannot be reduced because of lateral electrical coupling concerns, the method comprising:

forming a metal pattern with maximum feature spacing of about five microns;

forming an oxide spacer on one or more metal features of the metal layer to provide an effective space less than about five microns; and

executing a FLOW-FILL procedure to form a substantially void-free oxide layer on the metal layer and the oxide spacer.

13. The method of claim 12, wherein forming the metal pattern includes forming a metal layer; depositing a film resistant to lateral etching on the metal layer; and etching the metal layer to form the metal pattern.

14. The method of claim 13, wherein the film resistant to lateral etching is a TEOS, oxide-nitride film.

15. The method of claim 12, wherein forming the metal pattern includes forming a pattern including extensive serif features to avoid large open areas.

16. A method of making a dielectric layer, comprising:

depositing a dielectric material at a first deposition rate having a tendency to form voids; and

depositing a dielectric material on the deposited dielectric material at a second deposition rate having a tendency to form substantially no voids or fewer voids than the first deposition rate.

17. The method of claim 16, wherein depositing a dielectric material at the first and at the second deposition rate includes depositing a dielectric material using a TEOS-based procedure.

18. A method of increasing pattern-fill density of a metal layout, comprising:

identifying and filling in open areas of the metal layout with floating metal;

identifying and filling in notches of the metal layout; and

identifying and filling in corners of the metal layout.

19. The method of claim 18, wherein the recited steps are performed in the order recited.

20. The method of claim 18, further comprising:

identifying and filling in between opposing edges of live metal regions of the metal layout.

21. A method of increasing pattern-fill density of a hierarchical metal layout pattern definition, comprising:

identifying and filling in one or more notches, inner lines, and corners of the metal layout to define a first derivative metal layout pattern definition;

determining whether the first derivative metal layout pattern definition has a predetermined pattern fill density;

identifying and filling in one or more notches and corners of the metal layout to define a second derivative metal layout pattern definition;

determining whether the second derivative metal layout pattern definition has the predetermined pattern fill density; and

redefining one or more edges of the second derivative metal layout in response to determining that the second derivative metal layout does not have the predetermined pattern fill density.

22. A computer-readable medium comprising instructions for executing the method of claims 18, 19, 20 or 21.

23. An integrated circuit comprising at least a portion resulting from execution of the method of claims 1-17.

24. A system comprising:

a processor; and

at least one integrated memory circuit comprising at least a portion resulting from execution of the method of claims 1-17.

25. The system of claim 24, wherein the processor is a digital signal processor.

26. A method of forming a nearly planar dielectric film on a metal layer, comprising:

forming a metal layer having a predetermined feature spacing of no more than about 0.3 microns;

forming a first oxide layer using a TEOS-based procedure at a first deposition rate on the metal layer;

forming a second oxide layer on the first oxide layer using a TEOS-based procedure at a second deposition rate which is less than the first deposition rate;

facet etching the second oxide layer; and

reflowing at least a portion of at least one of the oxide layers.

27. The method of claim 26, wherein further a film resistant to lateral etching is deposited on the metal layer.

28. The method of claim 26, wherein further at least two oxide spacers are formed on lateral surfaces of at least some of the features of the metal layer.

29. A method of making nearly planar dielectric films on a metal layer, where feature spacing cannot be reduced because of lateral electrical coupling concerns, the method comprising:

forming a metal pattern with maximum feature spacing of about five microns;

forming an oxide spacer on one or more metal features of the metal layer to provide an effective space less than about five microns;

executing a FLOW-FILL procedure to form a substantially void-free oxide layer on the metal layer and the oxide spacer; and

reflowing at least a portion of the oxide layer.

30. The method of claim 29, wherein further forming a metal pattern includes forming a metal layer, depositing a film resistant to lateral etching on the metal layer, and etching the metal layer to form the metal pattern.

31. A method of increasing pattern-fill density in a metal layout pattern, comprising:

defining a primary metal layout pattern and measuring a pattern-fill density of the primary metal layout pattern;

determining if the pattern-fill density of the primary metal layout pattern is at least equal to a predetermined pattern-fill density value;

in response to determining that the metal layout pattern does not at least equal the predetermined pattern-fill density value identifying and filling in open areas of the metal layout pattern exceeding a first predetermined width value with areas of floating metal;

identifying and filling in notches in the metal layout pattern that have less the first predetermined width value, but more than twice a minimum feature size with live areas of metal;

identifying and filling in spaces between opposing edges of live metal regions in the metal layout pattern that have less the first predetermined width value, but more than twice a minimum feature size with live areas of metal;

defining a secondary metal layout pattern and measuring a pattern-fill density of the secondary metal layout pattern;

determining if the pattern-fill density of the secondary metal layout pattern is at least equal to the predetermined pattern-fill density value; and

in response to determining that the secondary metal layout pattern does not at least equal the predetermined pattern-fill density value repeating the

identifying and filling until the predetermined pattern-fill density value is achieved, or until a predetermined number of repetitions has occurred.