ABSTRACT

MULTIPLE PROGRAMMABLE INTERRUPT CONTROLLERS IN A MULTI-PROCESSOR SYSTEM

A multi-processor system that supports multiple programmable interrupt controllers (PIC). An advanced programmable interrupt controller (APIC) provides interface between the processors and the PICs. The APIC provides interface between processors and other I/O devices also. The APIC sends an interrupt request data packet with a first field set to a processor identification number, a second field set to a type of the device that sent interrupt request and a third field. The third field is set to an interrupt vector if the device sending the interrupt request to the APIC is a device other than PIC. The third field is set to a predetermined identification number of the PIC if the interrupt request is from the PIC. A processor, to which the interrupt is directed to, receives the packet. If the interrupt request is from a PIC, the processor uses the third field to identify which of the multiple PICs caused the interrupt. If the interrupt is from a device, other than a PIC, the processor uses the third field to determine an interrupt vector corresponding to the device.

Figure 1