ABSTRACT

NON-ETCH BACK SOG PROCESS USING A METAL VIA STUD

A process has been developed in which planar, multilevel metallizations, are used to fabricate semiconductor devices. The process features initially forming tall, narrow metal via stud structures, and filling the spaces between the metal via stud structures with a planarizing layer of a composite dielectric, which includes a spin on glass layer. The composite dielectric was deposited by initially using a non-porous, silicon oxide layer, followed by the planarizing spin on glass layer. Therefore metal via fills will interface the non-porous, silicon oxide layer.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)