

Claims

What is claimed is:

1. An apparatus comprising:
 - a semiconductor pillar operable to conduct a current;
 - a charge trap region separated from the semiconductor pillar by a tunnel region;
 - a dielectric blocking region adjacent to the charge trap region;
 - a gate adjacent to the dielectric blocking region and operable to control storage of charge in the charge storage region; and
 - a dielectric barrier between the dielectric blocking region and the gate, the dielectric barrier comprising a material different from a material of the dielectric blocking region, the material of the dielectric barrier having a dielectric constant greater than that of aluminum oxide.
2. The apparatus of claim 1, wherein the material of the dielectric barrier has a dielectric constant (κ) in a range of $12 < \kappa < 40$.
3. The apparatus of claim 1, wherein the material of the dielectric barrier has an electron affinity lower than that aluminum oxide.
4. The apparatus of claim 3, wherein the material dielectric barrier has an electron affinity in a range of $1.5 \text{ eV} < \chi < 2.5 \text{ eV}$.
5. The apparatus of claim 1, wherein the material of the dielectric barrier includes one or more of hafnium oxide, zirconium oxide, or a mixture of hafnium oxide and/or zirconium oxide with one or more of aluminum oxide, silicon oxide, titanium oxide, gadolinium oxide, niobium oxide, or tantalum oxide.
6. The apparatus of claim 1, wherein the charge trap region includes a dielectric silicon nitride.

7. The apparatus of claim 1, wherein the gate includes conductive titanium nitride.
8. The apparatus of claim 7, wherein the gate includes tungsten on and contacting the conductive titanium nitride.
9. A memory device comprising:
a string of memory cells including:
a vertical pillar of semiconductor material; and
a number of charge storage devices arranged along the vertical pillar, each charge storage device of the number of charge storage devices including
a charge trap region separated from the vertical pillar of the vertical string by a tunnel region;
a dielectric blocking region adjacent to the charge trap region;
a gate adjacent to the dielectric blocking region and operable to control storage of charge in the charge storage region; and
a dielectric barrier between the dielectric blocking region and the gate, a material of the dielectric barrier being different from a material of the dielectric blocking region, the material of the dielectric barrier having a dielectric constant greater than that of aluminum oxide.
10. The memory device of claim 9, wherein the material of the dielectric barrier includes hafnium oxide.
11. The memory device of claim 9, wherein the material of the dielectric barrier includes zirconium oxide.
12. The memory device of claim 9, wherein the material of the dielectric barrier includes a mixture of hafnium oxide with one or more of aluminum

oxide, silicon oxide, titanium oxide, gadolinium oxide, niobium oxide, or tantalum oxide.

13. The memory device of claim 9, wherein the material of the dielectric barrier includes a mixture of zirconium oxide with one or more of aluminum oxide, silicon oxide, titanium oxide, gadolinium oxide, niobium oxide, or tantalum oxide.

14. The memory device of claim 9, wherein the dielectric barrier has a thickness in a range from about 15 angstroms to about 50 angstroms from the dielectric blocking region to the gate.

15. The memory device of claim 9, wherein the tunnel region is a three region tunnel barrier.

16. The memory device of claim 15, wherein the three region tunnel barrier is a region of dielectric oxide, a region of dielectric nitride disposed on the dielectric oxide, and another region of dielectric oxide disposed on the region of dielectric nitride.

17. The memory device of claim 9, wherein the tunnel region is a two region tunnel barrier.

18. The memory device of claim 9, wherein the tunnel region is a one region tunnel barrier.

19. The memory device of claim 9, wherein the gate is a metal gate.

20. The memory device of claim 9, wherein the pillar of semiconductor material comprises poly silicon.

21. A memory device comprising:
a string of memory cells including:

a vertical pillar of semiconductor material; and
a number of charge storage devices arranged along the vertical pillar, each
charge storage device of the number of charge storage devices
including
a charge trap region separated from the vertical pillar of
the vertical string by a tunnel region;
a dielectric blocking region adjacent to the charge trap
region;
a gate adjacent to the dielectric blocking region and
operable to control storage of charge in the charge storage
region; and
a dielectric barrier between the dielectric blocking region
and the gate, a material of the dielectric barrier being
different from a material of the dielectric blocking region,
the material of the dielectric barrier having an electron
affinity lower than 2.8 eV.

22. The memory device of claim 21, wherein the material of the dielectric barrier has a dielectric constant (κ) in a range of $12 < \kappa < 40$.

23. The memory device of claim 21, wherein the material dielectric barrier has an electron affinity in a range of $1.5 \text{ eV} < \chi < 2.5 \text{ eV}$.

24. The memory device of claim 21, wherein the tunnel region includes a region of a first dielectric oxide, a region of dielectric nitride disposed on the dielectric oxide, and a region of a second dielectric oxide disposed on the region of dielectric nitride.

25. A method comprising:
forming a blocking dielectric region along a wall of an open area in a material stack;
forming a charge trap region on and contacting the blocking dielectric

region;

forming a tunnel region on and contacting the charge trap region;

forming semiconductor material on and contacting the tunnel region,

the semiconductor material operable as a channel to conduct a

current;

removing a portion of the material stack exposing a portion of the

dielectric blocking region;

forming a dielectric barrier on and contacting the exposed portion of the dielectric blocking region on a side of the dielectric blocking region opposite the charge trap region, a material of the dielectric barrier being different from a material of the dielectric blocking region, the material of the dielectric barrier having a dielectric constant greater than that of aluminum oxide; and

forming a gate on and contacting the dielectric barrier, the gate separated from the dielectric blocking region by the dielectric barrier.

26. The method of claim 25, wherein forming the dielectric barrier includes depositing hafnium oxide.

27. The method of claim 25, wherein forming the dielectric barrier includes depositing zirconium oxide.

28. The method of claim 25, wherein forming the dielectric barrier includes depositing a mixture of hafnium oxide with aluminum oxide.

29. The method of claim 25, wherein forming the dielectric barrier includes depositing a mixture of zirconium oxide with aluminum oxide.

30. The method of claim 25, wherein forming the dielectric barrier includes depositing a mixture of hafnium oxide with one or more of silicon oxide, titanium oxide, gadolinium oxide, niobium oxide, or tantalum oxide.

31. The method of claim 25, wherein forming the dielectric barrier includes depositing a mixture of zirconium oxide with one or more of silicon oxide,

titanium oxide, gadolinium oxide, niobium oxide, or tantalum oxide.

32. The method of claim 25, wherein forming the gate includes forming a conductive titanium nitride region on and contacting the dielectric barrier and forming tungsten on and contacting the conductive titanium nitride.

33. A method comprising:

forming a dielectric barrier on and contacting a wall of an open area in a material stack;

forming a blocking dielectric region on and contacting the dielectric barrier, a material of the dielectric barrier being different from a material of the dielectric blocking region;

forming a charge trap region on and contacting the blocking dielectric region;

forming a tunnel region on and contacting the charge trap region;

forming semiconductor material on and contacting the tunnel region, the

semiconductor material operable as a channel to conduct a

current; and

forming a gate on and contacting the dielectric barrier, the gate separated from the dielectric blocking region by the dielectric barrier.

34. The method of claim 33, wherein the material of the dielectric barrier has a dielectric constant greater than that of aluminum oxide.

35. The method of claim 33, wherein forming the dielectric barrier includes depositing aluminum oxide.

36. The method of claim 33, wherein forming the dielectric barrier includes depositing hafnium oxide.

37. The method of claim 33, wherein forming the dielectric barrier includes depositing zirconium oxide.

38. The method of claim 33, wherein forming the dielectric barrier includes depositing a mixture of hafnium oxide with one or more of aluminum oxide, silicon oxide, titanium oxide, gadolinium oxide, niobium oxide, or tantalum oxide.
39. The method of claim 33, wherein forming the dielectric barrier includes depositing a mixture of zirconium oxide with one or more of aluminum oxide, silicon oxide, titanium oxide, gadolinium oxide, niobium oxide, or tantalum oxide.
40. The method of claim 33, wherein forming the dielectric barrier includes forming material of the dielectric barrier having a dielectric constant (κ) in a range of $12 < \kappa < 40$.
41. The method of claim 33, wherein forming the dielectric barrier includes forming material of the dielectric barrier having an electron affinity in a range of $1.5 \text{ eV} < \chi < 2.5 \text{ eV}$.
42. The method of claim 33, wherein the method includes:
forming the open area as an open pillar in the material stack, the material stack including alternating isolation dielectrics and sacrificial regions for conductive regions;
removing portions of the sacrificial regions, exposing portions of the dielectric barrier; and
forming multiple gates on and contacting the exposed portions of the dielectric barrier, wherein multiple charge trap structures are formed in the material stack.
43. The method of claim 42, wherein the dielectric barrier, the blocking dielectric region, the charge trap region, the tunnel region, and the semiconductor material are formed as continuous regions between and through the multiple charge trap structures.

44. The method of claim 42, wherein forming the semiconductor material includes forming a doped hollow pillar of the semiconductor material in the open pillar.