

CLAIMS

1. An apparatus comprising:
 - a memory array having a plurality of memory cells;
 - memory access circuits coupled to the memory array and configured to perform write operations responsive to control signals;
 - control logic coupled to the memory access circuits and configured to apply a set of write parameters based, at least in part, on a number of write operations performed by the memory access circuits and further configured to provide control signals to the memory access circuits to perform write operations on the plurality of memory cells according to the set of write parameters; and
 - a parameter table defining a plurality of write cycle bins, wherein the parameter table includes a minimum number of write operations and a maximum number of write operations for each of the plurality of write cycle bins, wherein a first range defining a first write cycle bin at least partially overlaps a second range defining a second write cycle bin.
2. The apparatus of claim 1, wherein the control logic is configured to compare the number of write operations performed by the memory access circuits to the plurality of write cycle bins to select the set of write parameters.
3. The apparatus of claim 2, wherein the parameter table is stored in the memory array.
4. The apparatus of claim 1, wherein the plurality of memory cells includes one or more phase change memory cells.
5. The apparatus of claim 1, further comprising a write count circuit configured to store the number of write operations performed by the memory access circuits in the memory array.
6. The apparatus of claim 1, wherein the plurality of memory cells are arranged in a three-dimensional cross point array.
7. The apparatus of claim 1, wherein the set of write parameters comprises at least one of a programming voltage amplitude, pulse duration, pulse shape, a leading edge, and a trailing edge.
8. The apparatus of claim 1, wherein the control logic is further configured to apply the set of write parameters responsive to receiving a command to establish the set of write parameters for a memory device.

9. An apparatus comprising:
a memory device including a plurality of memory cells and configured to store information on the plurality of memory cells based on a set of write parameters, and further including a parameter table, stored in a subset of the plurality of memory cells of the memory device, the parameter table configured to store a set of write cycle bins corresponding to the set of write parameters, wherein the parameter table includes a minimum number of write operations and a maximum number of write operations for each of the plurality of write cycle bins, wherein a first range defining a first write cycle bin at least partially overlaps a second range defining a second write cycle bin.
10. The apparatus of claim 9, further comprising a write count circuit configured to store a number of write operations performed by the memory device.
11. The apparatus of claim 10, wherein the set of write operation parameters is selected based on the number of write operations performed by the memory device and the set of bins.
12. An apparatus comprising:
memory access circuits configured to store data in a plurality of memory cells based on a set of write parameters;
a parameter table stored in a portion of the plurality of memory cells, the parameter table including a plurality of write cycle bins corresponding to a plurality of sets of write parameters; and
control logic coupled to the memory access circuits, the control logic configured to determine at least one of the write cycle bins based on a number of write operations performed by memory access circuits and apply the set of write parameters from the plurality of sets of write parameters based on the determined write cycle bins, wherein each of the write cycle bins is defined by a range of write operations having a minimum and a maximum number of write operations, wherein a first range defining a first write cycle bin at least partially overlaps a second range defining a second write cycle bin.
13. The apparatus of claim 12, wherein the first range overlaps the second range by at least one order of magnitude.
14. The apparatus of claim 12, further comprising, a write count circuit coupled to the control logic and configured to store the number of write operations performed by the plurality of memory cells.
15. The apparatus of claim 12, wherein the set of write parameters comprises at least one of a programming voltage amplitude, pulse duration, pulse shape, a leading edge, and a trailing edge.

16. A method comprising:
identifying a number of write operations performed on a memory device;
adjusting write parameters based, at least in part, on the number of write operations performed on the memory device;
applying the adjusted write parameters to perform write operations on a plurality of memory cells responsive to a write command, wherein adjusting write parameters based, at least in part, on the number of write operations performed on the memory device comprises:
comparing, by control logic, the number of write operations to a plurality of write cycle bins to determine an applicable write cycle bin;
identifying a set of applicable write parameters based, at least in part on the applicable write cycle bin; and
adjusting the write parameters according to the identified set of applicable write parameters,
wherein the plurality of write cycle bins are defined by ranges of write operations having a minimum number of write operations and a maximum number of write operations, wherein a first range of a first write cycle bin overlaps with a second range of a second write cycle bin.
17. The method of claim 16, further comprising:
executing at least one write operation on the plurality of memory cells according to the set of write parameters.
18. The method of claim 16, wherein identifying the number of write operations is responsive to powering on or powering off the memory device.
19. The method of claim 16, wherein the number of write operations is periodically updated.
20. The method of claim 16, wherein each of the plurality of write cycle bins is associated with a different set of write parameters.
21. The method of claim 16, wherein the each of the ranges of write operations overlaps with an adjacent range of write operations.
22. The method of claim 16, wherein adjusting the write parameters is responsive to receiving a command to establish a set of write parameters for a memory device.
23. A method comprising:
receiving, by control logic, a command to establish a set of write parameters for a memory device;
receiving, by the control logic, a current number of write operations performed by the memory device;
receiving, by the control logic, a parameter table defining a plurality of write cycle bins;

comparing, by the control logic, the current number of write operations to the plurality of write cycle bins to determine an applicable write cycle bin; and

providing the set of write parameters to the memory device based, at least in part, on the applicable write cycle bin, wherein each of the plurality of write cycle bins is defined by a range of write operations having a minimum number of write operations and a maximum number of write operations, wherein a first range of a first write cycle bin overlaps with a second range of a second write cycle bin.

24. The method of claim 23, further comprising:
storing the parameter table in at least one of a register, a cache memory, or a random access memory.
25. The method of claim 23, further comprising:
executing at least one write operation according to the set of write parameters.
26. The method of claim 23, further comprising:
periodically receiving, by the control logic, an updated number of write operations.
27. The method of claim 26, wherein the command to establish the set of write parameters is received in conjunction with receiving the updated number of write operations.
28. The method of claim 23, wherein comparing the current number of write operations to the plurality of write cycle bins comprises determining a write cycle bin having a minimum number of write cycles that is less than the current number of write cycles and a maximum number of write cycles that is greater than the current number of write cycles.
29. The method of claim 23, wherein the set of write parameters comprises at least one of a programming voltage, pulse shape, leading edge, trailing edge, and pulse duration.