ABSTRACT

IMPROVED METHOD OF FILLING SHALLOW TRENCHES

This invention relates to a method of fabrication used for semiconductor integrated circuit devices, and more specifically to an improved method of filling shallow trenches, in shallow trench isolation, STI sub-quarter micron technology. The present method relates to a process for forming trench gap filling with chemically vapor deposited (CVD) silicon dioxide layers within trenches within substrates employed in integrated circuit fabrication.

There is first provided a silicon substrate having a trench formed therein. There is then formed a silicon dioxide layer through tetraethylorthosilicate (TEOS) and ozone reaction, at either sub-atmospheric, or atmospheric pressure, with enhanced surface sensitivity features, which lines the trench providing corner rounding. Then there is a thermal oxidation to form within the trench a thermal silicon dioxide layer underneath the TEOS-ozone trench silicon dioxide liner. Finally, there is formed on top of the trench a silicon dioxide layer formed by either low pressure CVD using TEOS, or non-surface sensitive TEOS ozone CVD, or a high-density plasma CVD process. All layers are further annealed to form a void-free trench fill.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)