Abstract

A finFET device includes a doped source and/or drain extension that is disposed between a gate spacer of the finFET and a bulk semiconductor portion of the semiconductor substrate on which the n-doped or p-doped source or drain extension is disposed. The doped source or drain extension is formed by a selective epitaxial growth (SEG) process in a cavity formed proximate the gate spacer. After formation of the cavity, advanced processing controls (APC) (i.e., integrated metrology) is used to determine the distance of recess, without exposing the substrate to an oxidizing environment. The isotropic etch process, the metrology, and selective epitaxial growth may be performed in the same platform.

[FIG. 5]