METHOD OF IMPROVING A SURFACE

The invention relates to a method of improving a surface of a semiconductor substrate, said surface consisting at least partially of silicon.

In semiconductor device production, it is more and more important to provide semiconductor substrates with a very high quality. Defects of semiconductor substrates can be of very different origin and may occur in the bulk material of wafers or layers or on the surface of a structure. Deficient wafers, like wafers or layers with holes or scratches on their surface or with oxide precipitates or so-called "HF-defects", which are present in or on a wafer and will be apparent by an HF-etch step, are mostly not suitable for further use.

To improve the surface characteristic of a defective wafer, a wafer treatment of a wafer surface such as an etching step or a CMP step can be used to remove or to reduce the number or the size of defects at or near the wafer surface. Typical etchants are halogen bearing compounds such as HCl, HBr, HI, HF, and others. The etchant can also be a fluorine bearing compound such as SF_6, or C_xF_x. Moreover or in addition, it is possible to treat a defect containing wafer thermally, preferably in a hydrogen bearing environment, to smooth it and to diminish its defects. The thermal treatment can be performed in a furnace or in a tool for rapid thermal processing (RTP). According to another approach disclosed in the document US 6,287,941 B1, a defective wafer such as a cleaved film can be subjected to a combination of etching and deposition at very high temperature using a combination of etchant and deposition gases to result in a better surface quality.

Although such methods lead, in the first instance, to a superficial improvement of the surface condition of a defective wafer by smoothing, abrasion or defect covering of the respective wafer, the known methods are mostly very laborious and the corresponding defects cannot really be repaired.

It is therefore the object of the present invention to provide a method of improving a surface of a semiconductor substrate, said surface consisting at least partially of silicon, wherein

with this method defects present in or on the semiconductor substrate can be really repaired to provide a semiconductor substrate with a high surface quality.

This object is solved by a method of the above mentioned type wherein the method comprises a deposition step comprising a selective epitaxial deposition of silicon on silicon in at least one hole on the surface of said semiconductor substrate.

The invention makes it possible to deposit silicon in said hole to seal or to close said hole selectively with high-quality mono-crystalline silicon material wherein a formation of polycrystalline silicon is avoided leading to the effect that the original hole disappears from the surface and the resulting repaired surface gets a high surface quality which is comparable to surfaces which are free from holes or defects from the outset.

In a preferred variant of the invention, said deposition step comprises a selective growth of silicon on at least a part of a side wall of said hole. In this manner, a hole in a silicon layer lying on another material can be closed by a gradual growth beginning from the side walls of the corresponding hole. This kind of method is, in particular, of interest for closing large holes in SOI structures with high-quality silicon.

In another favorable variant of the invention, said method comprises an etching step applied on the surface of the semiconductor substrate before the deposition step, said etching step comprising an etch-back of at least one defect being on the surface of the semiconductor substrate whereby forming said at least one hole on the surface. By means of this etching step, the at least one defect can be removed leading to at least one hole at the surface of the semiconductor structure which can be closed with silicon with the result that the original defect can be removed and a nearly perfect repaired surface of the originally defective semiconductor structure can be provided.

According to an advantageous embodiment of the invention, said deposition step is applied at least until the at least one hole is plugged with silicon. In some cases, it can be sensible or sufficient only to plug the hole so that the hole is closed wherein it is of minor interest whether the whole hole is filled with silicon or not. In any case, as a result, the former hole in

the surface of the semiconductor structure treated with this method is closed so that this semiconductor structure can be used for further processing.

Preferably, said deposition step is applied at least until the at least one hole is filled with silicon. In doing so, the former hole can be fully removed and the resulting structure can be provided with a high-quality both at and under the surface.

Advantageously, said etching step comprises a HF-dip to etch-back oxide containing defects at the surface of said semiconductor structure. An HF-etch step removes effectively oxide and thus reveals oxide containing defects at the surface resulting in a formation of holes on said surface which in turn can be closed with the selective deposition of silicon on silicon.

According to a preferred embodiment of the invention, in said selective epitaxial deposition, etchant and silicon containing gas are used as source gas. HCl as the etchant and SiH_2Cl_2 as the silicon containing gas are especially well suited material for a high-quality selective deposition of monocrystalline silicon since the respective source gas highly prevents nucleation of silicon on oxide surfaces or walls which would result in a growth of polysilicon. For selective epitaxial growth, favorable etchant concentrations are a few % of the total volume of the source gas.

In a preferred example of the present invention, silicon is deposited in the deposition step up to a thickness corresponding at least to about one half of the diameter of the hole on the surface. This thickness has been shown to be especially advantageous for a solid and durable sealing of the respective hole.

In order to remove contaminants from the etched surface, it has been shown as advantageous to apply a H_2 bake at about 650°C, preferably for about 2 minutes, on the semiconductor structure before the deposition step. This relatively low-temperature H_2 bake leads to an effective removal of contaminants but to a low risk of agglomeration of silicon during the deposition step.

It has been shown to be advantageous to perform said deposition step at about 750°C. This deposition temperature is lower than the temperature used in standard epitaxy processes.

That way, agglomeration of silicon can be avoided, in particular if SOI structures with thin silicon top layers are treated with the inventive method.

In a further embodiment of the invention, said deposition step is performed under reduced pressure, for example from about 20 Torr to 80 Torr. The deposition in a reduced atmosphere with this pressure leads to especially good and homogenous silicon formation.

In another variant of the invention, the thickness of silicon on the surface of the semiconductor substrate is reduced before and/or after said deposition step. This enables a reduction of the final thickness of the treated semiconductor substrate, which can be in particular of importance in repairing of SOI wafers.

Advantageous embodiments of the invention will be described in the following with respect to the figures in which

Fig. 1 schematically shows a SOI substrate containing a defect;

Fig. 2 schematically shows the substrate of Fig. 1 after a short HF dip;

Fig. 3 schematically shows the substrate of Fig. 2 after selective deposition of silicon;

Fig. 4 schematically shows after a deeper HF dip;

Fig. 5 schematically shows the substrate of Fig. 4 after selective deposition of silicon;

Fig. 6 schematically shows a hole in a SOI-substrate sealed with silicon in accordance with the present invention; and

Fig. 7 schematically shows another hole in a SOI-substrate sealed with silicon in accordance with the present invention.

Fig. 1 schematically shows a SOI substrate 1 containing at least one defect such as a HF-defect or the shown oxide precipitate 2. The SOI substrate 1 is only shown exemplarily to

demonstrate the principle of the present invention, wherein the present invention can also be used to improve the surface quality of another semiconductor substrate like a silicon wafer or any other substrate having on top at least partially silicon. In particular, it is not necessary to provide a substrate with an oxide layer, as shown in Fig. 1, to apply the inventive idea of repairing this substrate.

The inventive method is also applicable to other materials such as silicon alloys, for example SiGe structures.

The SOI substrate of Fig. 1 comprises a silicon substrate 3, on which a buried oxide 4 is formed, and has on top a silicon layer 5 having a certain thickness t_1 and comprising the at least one defect such as the shown oxide precipitate 2 situated at a surface 6 of the silicon layer 5 and extending into the bulk region of this silicon layer 5. The only one defect shown in Fig. 1 consists in the example shown mainly of silicon dioxide and is only shown exemplarily to illustrate the idea of the invention, wherein in fact considerably more defects as the one defect shown can be present in or on the silicon layer 5. The oxide precipitate of Fig. 1 shall show exemplarily a "small" defect having a rather small lateral extension being in the order of magnitude of the thickness of the silicon layer 5 or smaller.

According to Fig. 2, the structure shown in Fig. 1 is subjected to HF leading to an at least partial removal of the oxide precipitate 2 beginning at the surface 6 and continuing in the depth of the oxide precipitate 2 without or with only minimum effects on the silicon layer 5 since HF etches silicon with a much lower rate than silicon dioxide. In the same way, the HF dip treatment can be used to etch-back HF-defects to create space which can be filled or plugged in a subsequent process step described below with defect-free silicon.

The longer the HF dip the deeper is the resulting hole 7 in the surface 6 of the SOI structure 1. As shown in Fig. 4, a longer HF dip can result in a hole 17 extending into the buried oxide layer 4 underlying the silicon layer 5.

Fig. 3 schematically shows the SOI substrate of Fig. 2 after a selective deposition of silicon using Selective Epitaxial Growth (SEG) wherein the dashed lines and the direction of arrow

A shall demonstrate schematically the progress of silicon deposition leading to a thickness t_2 of the resulting silicon top layer 8.

SEG is an epitaxial deposition process which has the advantage that it will prevent, in general, nucleation of silicon on a polycrystalline or an amorphous material like an oxide surface. An epitaxial silicon growth does only occur on mono-crystalline silicon.

Prior to the SEG step, wet cleaning and in situ H_2 bake at about 650°C to 800°C for about 2 minutes under a reduced pressure, for example of 20 Torr is applied on the SOI-structure shown in Fig. 2 in order to remove C, O and F contaminants on the surface 6. If a bulk material such as a silicon wafer shall be repaired instead of the SOI-structure shown in Fig. 2, the H_2 bake is performed at higher temperatures. If the silicon layer 5 is thinner than 20 nm, temperatures in excess of about 700°C should not be applied during H_2 bake on the SOI structure 1 to prevent a Si film retraction during SEG. Only in cases in which the film thickness of the silicon layer 5 is higher than 20 nm, the H_2 bake can be performed at temperatures up to 850°C or higher. Although in comparison with other conventional H_2 bake processes the recommended temperature of the invention for the H_2 bake is relatively low, the contaminants left on the surface 6 prior SEG silicon formation have not such an impact on the electrical properties of the resulting devices since they will be partially consumed or removed during later procedural steps. The H_2 bake is followed by a ramping-up of the temperature up to the temperature of the SEG step.

To avoid an agglomeration of silicon, the SEG of silicon is performed in a reduced atmosphere of about 20 Torr applying a relatively low temperature of about 650°C to 800°C and using for instance HCl as an etchant and for instance SiH_2Cl_2 as the Si gaseous precursor and using H_2 as carrier gas, optionally with some gaseous hydrochloric acid to achieve full selectivity vs. SiO_2 and Si_3N_4. For an ultra-thin silicon layer 6 with a thickness t_1 in the range of 3 to 10 nm, the SEG step should be performed at about 750°C using for example a SiH_2Cl_2 + HCl chemistry to avoid any severe islands formation during silicon growth. During SEG, the growth rate of silicon should be fairly low which can be achieved by source gas reduction wherein the reaction rate is reduced in the presence of HCl.

As shown schematically in Fig. 3 by the dashed lines, silicon grows during SEG on the surface 6 of the silicon layer 5, on the open silicon at the side walls of the etched hole 7 as well as on the already grown silicon in such a way that the hole in the silicon layer 6 is gradually closed or plugged with silicon. After a certain process time, a thickness t_2 of silicon with a high surface quality is reached on top of the silicon layer 6. The non-etched part of the defect 2 and a small unfilled residual part of the etched hole 7 are buried in the structure above the oxide surface where no nucleation occurs.

If the defect shown in Fig. 1 is fully etched away during the etching step and the etching step is performed in such a way that the buried oxide below the silicon layer 5 is not influenced, the defect(s) in or on the silicon layer 5 can be fully removed and replaced by high-quality silicon resulting in a nearly perfect structure having a surface 6 without defects or with only a minimum of defects.

During the SEG deposition step, it can be assumed that the opening of the hole 7 is sealed if the thickness t_2 of the deposited silicon layer is about ½ of the diameter w of the hole 7. Therefore, a minimum epitaxial thickness t_2 of about ½ of the hole 7 diameter w is necessary in order to seal the opening.

With reference to Fig. 4, the structure of Fig. 1 is etched deeper than in Fig. 2 during the etching step so that the buried oxide 4 lying under the silicon layer 5 was affected. The resulting hole 17 in the SOI structure 1 has silicon side walls formed by the silicon layer 5 and a bottom of silicon dioxide formed by the attacked buried oxide layer 4.

As shown schematically in Fig. 5, the hole 17 of the SOI substrate of Fig. 4 is gradually filled during the SEG process with silicon. At a certain time of growth, the hole 17 is plugged and covered with high-quality mono-crystalline silicon wherein a little cavity 27 can remain in the buried oxide layer 4 which hole 27 is not filled with silicon.

The Figs. 6 and 7 show schematically that the idea of the invention can also be used to improve the surface quality of substrate or structures having on top layer with "larger" holes such as "wells" having a large aspect ratio wherein the width w of the holes is a few times higher than their depth h ($w / h >> 1$). In the examples shown in Figs. 6 and 7, the diameter

w of the holes 37 and 47 is about 0.5 μm, the silicon top layer 5 has a thickness of about 50 nm and the oxide layer 4 has a thickness of about 150 nm resulting in an aspect ratio of 2.5.

The arched lines in the Figs. 6 and 7 indicate the sequence of epitaxial deposition.

With reference to Fig. 6, a SOI substrate 10 is shown, said SOI substrate 10 consisting of a silicon substrate 3, an oxide layer 4 on the silicon substrate 3 and a thin silicon top layer 5. The SOI substrate 10 has a hole 37 through the silicon top layer 5 and the oxide layer 4. The hole 37 has in the example shown nearly perpendicular, flat side walls formed, for instance, by photolithography and etching, but can have, in other not shown embodiments of the present invention, also inclined and/or rough side walls. The bottom 39 of the hole 37 is formed by the surface of the silicon substrate 3 and consists, therefore, of mono-crystalline silicon.

In the embodiment shown in Fig. 6, the surface 6 of the structure 10 can be smoothed and straightened by filling the hole 37 in accordance with the present invention using the Selective Epitaxial Growth of silicon. In the particular case shown in Fig. 6, a HF dip prior SEG is not necessary but can, for instance if native oxide should be removed from the bottom 39, be applied. As explained above with reference to Figs. 3 and 5, it is furthermore possible to apply a wet cleaning step before SEG.

As also explained above with reference to Figs. 3 and 5, prior to SEG a H_2 bake is applied.

Then follows a SEG step in accordance with the exemplification of Figs. 3 and 5. During the SEG step, silicon grows on the exposed silicon areas of the structure 10, in particular on the surface 6 of the silicon layer 5, on the exposed side walls 20, 21 of the silicon layer 5 and on the bottom 39 of the hole 37 as well as on the already grown silicon. As result, the silicon grows in such a way that the hole 37 is gradually filled during SEG with mono-crystalline silicon wherein it can be possible that at the end of SEG very small buried cavities in the former "large" hole 37 remain which are not overgrown.

Fig. 7 schematically shows an oxide hole or well 47 in a SOI substrate 11 sealed with silicon in accordance with the present invention. The SOI substrate 11 consists, like the SOI

substrate 10 of Fig. 6, of a silicon substrate 3, an oxide layer 4 and a silicon top layer 5 having a surface 6 with the "large" hole 47 having a more lateral than vertical extension. In contrast to the structure of Fig. 6, the SOI substrate 11 has on the bottom 49 of the hole 47 a residual thickness of SiO_2 of the not completely etched oxide layer 4 so that the bottom 49 consists of silicon dioxide. Consequently, the silicon growing during SEG does not form on the bottom 49 but only on the surface 6 and the exposed side walls 20, 21 of the silicon layer 5 as well as on the already grown silicon resulting in an overgrowth of the hole 47 from the sides what can be proceeded till the hole 47 is closed. At the end, there is a smooth, nearly perfect surface of the SOI-substrate formed wherein it is possible that residual little cavities are buried in the treated structure which are not completely filled with mono-crystalline silicon.

In the following, the thickness of the structures as shown in the Figs. 3, 5, 6 or 7 can be adjusted onto certain requirements by a reduction of the thickness of the grown silicon using oxidation, CMP and/or silicon etching. Optionally, the final SOI thickness can also be thinned by an initial reduction of the thickness t_1 of the silicon top layer 5, for instance by oxidation, CMP and/or silicon etching prior to HF-dip or SEG, or by a combination of initial and final thickness reduction. Furthermore, additional finishing steps, like smoothing annealing can be performed on the final structure.

Thus, the present invention offers a method for repairing defects or closing holes in a surface of a semiconductor substrate consisting at least partially of silicon. The method of the invention can be used to repair defects in silicon substrates as well as in Semiconductor on Insulator Substrates (SeOI) like Silicon on Insulator (SOI) wafers. Regarding the repair of defect(s), the combined action of HF dip and SEG leads not only to a removal of the corresponding defect(s) but also to a plug of the etched hole with high-quality mono-crystalline silicon without a formation of poly-Si in the rebuilt structure.

By means of the inventive method which uses as a new approach the SEG process on a blanket silicon surface, the quality of a defective semiconductor substrate can be enhanced making this substrate attractive for further fabrication processes. SOI substrates repaired with the method of the invention are especially well suited for prospective applications where thicker SOI substrates are required. Depending on the respective top layer specifications, in

particular the final thickness ($t_1 + t_2$) of a repaired substrate can be adapted in such a way that the repaired wafer can rejoin the original product group.

SOI wafers repaired with the method of the invention are applicable for the formation of advanced substrates using Direct Substrates Bonding (DSB). Furthermore, the method according the present invention allows repair of defects occurring in structures produced by the so-called "Smart Cut®"-process.

Moreover, the inventive technology is in particular advantageous for repairing deep defects or for closing large holes in a semiconductor substrate which can not be repaired or closed using the known surface smoothing methods.

Claims

1. Method of improving a surface of a Silicon on Insulator(SOI) semiconductor substrate, said surface comprising at least partially silicon, the method comprising

   a deposition step comprising a selective epitaxial deposition in at least one hole at the surface of said SOI semiconductor substrate,
   an etching step applied on the surface of the SOI semiconductor substrate before the deposition step,
   said etching step comprising an etch-back of at least one defect being at the surface of the SOI semiconductor substrate whereby forming said at least one hole at the SOI semiconductor surface.

2. Method according to claim 1, wherein said deposition step comprises a selective growth of silicon on at least a part of a side wall of said hole.

3. Method according to claim 1 or claim 2, wherein said deposition step is applied at least until the at least one hole is plugged with silicon.

4. Method according to claim 1 or claim 2, wherein said deposition step is applied at least until the at least one hole is filled with silicon.

5. Method according to claim 1 or claim 2, wherein said etching step comprises a HF-dip to etch-back oxide containing defect(s) at the surface of said SOI semiconductor structure.

6. Method according to claim 1 or claim 2, wherein in said selective epitaxial deposition etchant and silicon containing gas are used as source gas.

7. Method according to claim 6, wherein said etchant is HCl and said silicon containing gas is SiH_2Cl_2.

8. Method according to claim 1 or claim 2, wherein silicon is deposited in the deposition step up to a thickness(t_2) corresponding at least to one half of the diameter (w) of the hole at the surface.

9. Method according to claim 1 or claim 2, wherein prior to the deposition step a H_2 bake at 650°C is applied on the semiconductor structure.

10. Method according to claim 1 or claim 2, wherein said deposition step is performed at 750°C.

11. Method according to claim 1 or claim 2, wherein said deposition step is performed at 20 Torr to 80 Torr.

12. Method according to claim 1 or claim 2, wherein the thickness of silicon on the surface of the SOI semiconductor substrate is reduced before and/or after said deposition step.

13. Method according to claim 1 or claim 2, wherein said surface comprises a silicon alloy.

14. Method according to claim 1 or claim 2, wherein said surface comprises SiGe.