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[Continued on next page]

(54) Title: APPARATUS AND METHOD FOR EFFECTING CHANGES IN PROGRAM CONTROL FLOW

JAVASW

JAVA INTERPRETER SWITCH

OPERATION: JUMP TO BYTECODE EMULATION SEQUENCE;

91 ~ IF (SWCOUNT<0)

92 ~ PC<-(((PC+2) & 0xffffe000) | (R4<<5));

93 ~ ELSE

94 ~ PC<-(((PC+2) & 0xffffe000) | (0x8));

95 ~ SWCOUNT--;

ASSEMBLER

SYNTAX: JAVASW RX

DESCRIPTION: JUMP TO BYTECODE EMULATION SEQUENCE. THE LOW ORDER 13 BITS OF THE VALUE OF PC+2 ARE FORCED TO ZERO, AND BASED ON THE STATE OF THE SWCOUNT (IN REGISTER R12), EITHER A SCALED VALUE IN REGISTER RX IS LOGICALLY "OR'ED", OR A CONSTANT VALUE 0x8 OR'ED, AND INSTRUCTION EXECUTION RESUMES AT THE NEW PC VALUE. THE SWCOUNT REGISTER R12 IS DECREMENTED. NOTE THAT BECAUSE PC+2 IS USED AS THE BASE VALUE, A JAVASW INSTRUCTION SHOULD NOT BE USED IN THE LAST INSTRUCTION OF INSTRUCTION GROUP 255.

CONDITION CODE: UNAFFECTED

INSTRUCTION FORMAT:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

INSTRUCTION FIELDS:

JAVA INTERPRETER SWITCH SUPPORT IS PROVIDED BY THE JAVASW INSTRUCTION. THIS INSTRUCTION CAUSES CONTROL FLOW TO BE DIRECTED INTO A TABLE OF INSTRUCTION GROUPS. MOST GROUPS CONSISTS OF 16 INSTRUCTIONS AND CORRESPOND TO A SINGLE JAVA BYTECODE.

(57) Abstract: A data processor executes an instruction (JAVASW) to implement efficient interpreter functionality by combining the tasks of table jumps and thread or task switching which is controlled by a running value such as a counter or a timer. Execution of the instruction always requires a change of flow to be taken. In one form, the instruction may cause a hardware accelerator to be signaled to complete instruction execution. Additionally, a memory table containing emulation code correlated to specific byte codes may be compressed for a large number of identified byte codes by the use of separate storage. Further, use of a same portion of the memory table may occur in connection with execution of different bytecodes. While discussed in the context of Java bytecodes, the instruction is applicable to any programming language and processor architecture.



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WO 02/065276 A3



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