

PATENT SPECIFICATION

(11) 1 487 955

1 487 955

- (21) Application No. 52478/74 (22) Filed 4 Dec. 1974
 (31) Convention Application No. 48/135301
 (32) Filed 5 Dec. 1973 in
 (33) Japan (JA)
 (44) Complete Specification published 5 Oct. 1977
 (51) INT CL² G04C 3/00 H03K 21/00
 (52) Index at acceptance
 G3T A5X
 G4D 1D11 6C1 6C2 6Y



(54) IMPROVEMENTS IN OR RELATING TO TIMEPIECES HAVING TIME STANDARDS CONSTITUTED BY PIEZO-ELECTRIC CRYSTAL OSCILLATORS

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company, of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to timepieces of the kind which comprise a time standard constituted by a piezo-electric crystal oscillator. Timepieces of the kind are commonly called quartz crystal timepieces and will hereinafter be referred to by this expression.

The main object of the invention is to provide a timepiece of the kind referred to in which regulation is achieved automatically under the control of an externally produced standard time signal as distinct from measuring the advance or retard necessary to obtain the data for regulation and then putting in the data. As will be seen later the invention provides improved timepieces in which such desirable fully automatic regulation is obtainable easily and reliably over as wide a range as is required in practice. The timing regulation of a quartz crystal timepiece determines its accuracy as a time keeper and is obviously a matter of the greatest importance.

In a conventional quartz crystal timepiece as at present in common use timing regulation is effected manually, usually by changing the oscillation frequency of the time standard oscillator by varying the capacitance of a trimmer capacitor which forms part of the oscillator circuit. However, there is nothing automatic about this and, moreover, because a trimmer capacitor has a movable part it tends to lack reliability. Moreover, if it is of the very small physical size it must be if it is to be accommodated in a watch or small clock, its range of capacitance variation is undesirably limited and therefore the range of oscillation frequency variation of which it is capable is also undesirably limited. Accordingly, when a trimmer capacitor is used to regulate the frequency of the quartz crystal

oscillator of a timepiece, the requirement as regards frequency tolerance in the crystal itself is very severe and this fact means that an expensive crystal has to be used if a high degree of time accuracy is to be attained by the timepiece. Moreover the fact that regulation of the frequency of the quartz oscillator involves mechanical movement of a part of the trimmer capacitor involves an obvious disadvantage.

The recent increasing popularity of quartz crystal timepieces and the increasing demand for inexpensive but accurate timepieces of this kind has led to a demand for the use of cheap quartz crystal oscillators in such timepieces, but, of course, if an inexpensive quartz crystal is used provision must be made for a relatively extensive range of frequency adjustment. Moreover there is also a demand for the timing regulation to be automatic. Timing regulation by the use of a trimmer capacitor for frequency regulation of the quartz oscillator is inherently unlikely to satisfy these requirements.

The range of frequency adjustment can be substantially increased (as compared with that practically achievable by a trimmer capacitor) by effecting timing regulation by varying the division ratio of a frequency divider which is employed to divide in frequency the output oscillations of a quartz crystal oscillator. However, known timepieces employing this principle of timing have the defect of circuit complexity mainly owing to the increased number of circuit branches or terminals which have been required in order to enable automatic timing regulation control to be applied to the portion of the watch circuitry—the variable ratio frequency divider—by means of which the required wide range of timing regulation is achieved. Accordingly known timepieces employing the principle in question are undesirably complicated in circuitry and in operation and are difficult to make cheaply and of the small physical size so often required, for example in a wrist watch.

The present invention seeks to provide

50

55

60

65

70

75

80

85

90

95

improved quartz crystal timepieces which have automatic timing regulation, which can be made relatively cheaply and of small size, and which shall at the same time be reliable and robust.

According to this invention a timepiece comprises a time standard constituted by a piezo-electric crystal oscillator; an electronic circuit including a frequency dividing circuit driven by output from said oscillator; time display means driven by the divided frequency output; receiving means in said timepiece for receiving an externally produced standard time signal; a frequency deviation measuring circuit for measuring frequency deviation between the piezo-electric crystal oscillator frequency and a basic frequency in fixed frequency relationship with said externally produced standard time signal received by said receiving means, a frequency deviation memory circuit for memorising data representative of the frequency deviation measured by said frequency deviation measuring circuit; a regulating circuit for regulating timing by controlling under the control of the memorised data, the effective division ratio of said frequency dividing circuit; and control means for bringing said receiving means, frequency deviation measuring circuit, memory circuit and regulating circuit into operation to effect timing regulation.

Preferably said receiving means is the normal provided driving coil of an electromechanical converter actuating the time display means of the timepiece.

Preferably the effective division ratio of said dividing circuit is controlled by controlling the number of pulses produced thereby from the output of said oscillator.

Said frequency deviation measuring circuit may be constituted by part of said frequency dividing circuit.

Said frequency dividing circuit, said frequency deviation measuring circuit and said memory circuit may comprise each a series of master slave flip-flop circuits.

In one embodiment of the invention the frequency deviation measuring circuit comprises a first series of master slave flip-flops; said frequency dividing circuit comprises said first series and a following second series of master slave flip-flops; said memory circuit comprises a third series of master slave flip-flops each connected to receive and memorise data from a respective one of the flip-flops in said first series; a first plurality of gates each having an input terminal connected to a respective flip-flop in said second series and a second input terminal connected to a respective flip-flop in said third series; and a second plurality of gates controlled by the gates in said first plurality and included in a feed back circuit across said frequency dividing circuit.

The invention is illustrated in and further

explained in connection with the accompanying drawings in which:

Figure 1 is a simplified block diagram of one embodiment of the invention;

Figure 2 is a highly simplified diagram showing in general manner one way of utilising an external standard time signal for automatic timing regulation;

Figure 3, which is composed of two portions, Figure 3a and Figure 3b, shows, so far as is necessary to an understanding of the invention, one embodiment thereof in diagrammatic manner;

Figure 4 shows in more detail, one of the flip-flops included in the embodiment of Figure 3; and

Figure 5 is a graphical figure explanatory of the operation of the embodiment of Figure 3.

Referring to Figure 1 the time standard of the timepiece therein represented is a quartz crystal oscillator 1 the output from which is fed to a frequency divider 2. Block 3 represents a time display unit and may be regarded as including the time display means and the necessary circuitry for driving it under the control of the divided frequency output from divider 2. Block 4 is frequency deviation measuring circuit which measures the difference between the frequency of the quartz crystal oscillator 1 and a basic oscillation frequency determined by the dividing circuit 2. 5 is a frequency deviation memory circuit which memorises the frequency deviation as obtained by the frequency deviation measuring circuit 4, or a coded signal representative of said frequency deviation. 6 is a regulating circuit which effects timing regulation by controlling the division ratio of the divider 2, this control being effected in accordance with the memorised data in the frequency deviation memory circuit 5. 7 is a receiver which receives a standard time signal obtained from outside the timepiece. 8 is a control circuit which controls the circuit units 4 and 5 via control leads referenced a, b and c. 9 is a timing regulation lock switch.

The general operation is as follows:— When the lock switch 9 is set to "ON" (closed) a previously existing lock on regulation is released and a reset signal is generated by and passed from the control circuit 8 over lead a to the deviation measuring circuit 4 and resets said circuit. Suppose now that an external standard time signal occurring at (say) an interval of one second or of seconds is applied from some external source (not shown) to the receiver. Suppose also that the design frequency of the output from the divider 2 is f_1 and that the division ratio of the said divider, when regulation is not being effected, is A. What is herein termed a "basic" frequency of $1/A \times f_1$ will accordingly be produced in circuit 8. Then,

accomplishing

block diagram of
the system, one way of
measuring the signal for

used of two
blocks, shows, so
that the deviation of the
frequency in dia-

ally, one of the
components of

an explanatory
part of Figure

is a standard of
which is a quartz
oscillator which is
represented by block 3. The
oscillator is regarded
as a standard and the
output from the
frequency deviation
measuring circuit 2
of the quartz
oscillation fre-
quency circuit
deviation as
a representative
regulating
quantity by
the divider 2,
in accordance with
the frequency deviation
measuring circuit
4 and 5 via
lead c. 9 is a

follows:—
the "ON"
lock on
the control
measuring
circuit. Suppose
the time signal
one second
external
reference. Suppose
the output
the division
regulation is
herein
1/A × f₀, will
it 8. Then,

if the input frequency to the divider departs
from the value which will produce the design
output frequency f₀, there will be a frequency
deviation between the basic frequency and
the external standard time signal and this
deviation, which gives rise to a count, is
measured in the deviation measuring circuit 4,
this measurement of deviation being obtained
in response to a measuring order signal sent
over lead b. For example, to take typical
practical figures for a wrist watch, if the time
standard frequency source therein is a quartz
crystal controlled oscillator having a frequency
of, say, 32768 KHz or 16384 KHz, and this
is divided down to a frequency of 1 Hz for
feeding to the remaining time measuring
circuitry of the watch, this 1 Hz frequency
would be the basic frequency. The measured
deviation is memorised in the frequency
deviation memory circuit 5 in response to a
memory order signal sent over lead c. There
is thus established in the memory circuit 5
memorised data—hereinafter referred to as the
"regulating quantity" which is representative
of the deviation measured by the measuring
circuit 4. At this stage the lock switch 9 is
set to the "OFF" position (opened) in order
to ensure that noise or other disturbance will
not interfere with the memorised regulation
quantity. Since the regulating quantity
memorised in the frequency deviation memory
circuit 5 is representative of the deviation of
the oscillation frequency of the quartz crystal
oscillator 1 with respect to the basic fre-
quency, timing regulation can be effected by
changing the effective division ratio of the
divider 2 in correspondence with the said
deviation. The regulating circuit 6 performs
this operation and carries out timing regulation
by controlling the said effective division ratio
in accordance with the data memorised in the
frequency deviation memory circuit 5.

As will now be apparent timing regulation
is, from the point of view of the user or
operator, extremely simple. All that he has
to do is to operate the switch 9 to remove
the regulating lock and then return the switch
to its initial position. Apart from this the
whole operation of timing regulation in
accordance with a received external standard
time signal is completely automatic.

An embodiment of this invention will now
be described in more detail. Figure 2 illus-
trates the principle of the embodiment. In
Figure 2 11 is a generator, external to the
timepiece and which generates a standard time
signal at intervals of two seconds. This signal
is transmitted magnetically from a trans-
mitting coil L₂ to a receiving coil L₁ in the
timepiece. The coil L₁ is also used as the
driving coil of the normally provided electro-
mechanical converter of the timepiece. The
electronic circuitry of the timepiece is repre-
sented by block 10 in Figure 2 and includes
the means already described with reference

to Figure 1 for measuring and utilising fre-
quency deviation. From the functional point
of view coil L₁ of Figure 2 is, in effect, the
receiver 7 of Figure 1.

Figure 3 shows the circuitry in block 10
of Figure 2 in some detail. For convenience
of drawing Figure 3 is divided into two parts
referenced Figure 3a and Figure 3b respec-
tively, the leads on the right hand side of
Figure 3a being the same as those on the
left hand side of Figure 3b.

Referring to Figure 3, FF₁ to FF₂₄ are
master slave type flip-flop circuits. One of
them is shown in more detail in Figure 4.
In Figure 4 D is a data input terminal; CL
is a clock pulse input terminal; Q_M is a master

signal output terminal; Q_M is a master signal
output terminal providing a master signal
whose phase is the opposite of that from Q_M;

Q_S is a slave signal output terminal; Q_S is a
slave signal output terminal providing a slave
signal whose phase is the opposite of that
from Q_S; and R is a reset terminal.

In Figure 3 the master slave flip-flops are
represented simply and without detail, only
those terminals necessary to an understanding
of the general operation being shown. The

actual connections between D and Q_S and R
and ground are as shown in Figure 4, ground
being the minus potential terminal. FF₁ to
FF₁₄ are frequency dividers and FF₁ to FF₆
are also in the frequency deviation measuring
circuitry. E₁ to E₄ are exclusive OR gates
and A₁ to A₄ are NAND gates, E₁ to E₄
being included in a feedback loop across the
chain of dividers FF₁ to FF₁₄. FF₂₀ to FF₂₄
are in the memory in which the regulating
quantity, which is dependent on the measured
deviation, is stored. As will be apparent from
the Figure 3, these memory flip-flops are con-
nected to and memorise deviation measured
by the deviation measuring flip-flops FF₁ and
FF₂ and are also connected to control the
opening and closing of the gates A₁ to A₄,
the second inputs to which are taken from
the flip-flops FF₁₄ to FF₁₈. The output of
each of the gates A₂ to A₄ provides one input
to each of the gates E₁ to E₄ respectively,
the second input to each of the said gates E₂,
E₃, E₄ being provided from the output of the
respective preceding gate E₁, E₂ or E₃ and the
second input to gate E₁ being provided by
the output from the gate A₁. More in detail
the gates A₁ to A₄ are associated with the
flip-flops FF₁₄ to FF₁₈ as regards one input
and with the flip-flops FF₂₀ to FF₂₄ as
regards the other, each of said gates having
one input connected to a Q_M terminal of one
of the former flip-flops and its other input

connected to a Q_M terminal of one of the
latter flip-flops, all as shown. Gate E₁ has one

input fed from the output of gate A, and the other fed from the output of gate A₂. The gates E₂, E₃ and E₄ each has one input fed from the gates E₁, E₂ and E₃ respectively and the other from the gates A₃, A₄ and A₅ respectively. The last gate E₅ has one input fed from oscillator 1 and is controlled by the output from NAND gate O₁ to be mentioned later. E₅ feeds its output to FF₁ through another NAND gate connected as shown and controlled by an inverted signal taken from a NAND gate O₂ in the regulating control circuit. By means of these gates, connected as shown, the number of pulses fed in from the oscillator 1 to FF₁ is regulated in accordance with the data stored in the memory flip-flops FF₂₀ to FF₂₄ so that automatic regulation is effected by controlling the effective division ratio of the divider FF₁ to FF₅. The flip-flop FF₁₀ is a delaying circuit

and produces at the common $\overline{Q}_s$ terminal of

FF₁₀ and $\overline{Q}_M$ terminal of FF₁₀ a delayed pulse for operating the drive circuit for the driving coil L₁ of the electro-mechanical converter of the timepiece. This drive circuit includes MOS transistors T_{N1} and T_{N2} which can carry the necessary relatively large currents required by the coil L₁. FF₂₅ and FF₂₆ are used for regulating control and O₁ is a gate for stopping regulation while the regulating quantity is being established. Switch 9 is the lock and reset switch as in Figure 1.

When the switch 9 is opened, FF₂₅ and

FF₂₆ are reset, $\overline{Q}_M$ is at "high" level and QS is "low". When switch 9 is closed, FF₂₅ is released from reset and is triggered by the

output $\overline{Q}_s$ of FF₁₀, output $\overline{Q}_M$ of FF₂₅ becomes "low" and FF₂₆ is released from reset, both inputs to NOR gate NG become "low", its output becomes "high" and FF₁ to FF₁₀ are reset. This is the state between times t₁ and t₂ in Figure 5.

When the standard time signal is received FF₂₆ is triggered, its output Q_s becomes "high", the output of NG becomes "low", FF₁ to FF₁₀ are released from reset, and the measurement of frequency deviation commences. Accordingly the master portion FF₂₀—FF₂₄ assumes the "write-in" state. This is the condition in the period t₂ to t₃ of Figure 5.

When the next standard time signal comes in, FF₂₆ is triggered, its output Q_s becomes "low" again, the output of gate NG becomes "high", FF₂₀—FF₂₄ assume the "data holding" state, the frequency deviation is memorised and FF₁—FF₁₀ are reset. This is the period t₃—t₄ in Figure 5.

When switch 9 is opened again, FF₂₅ and FF₂₆ are reset and FF₁ to FF₁₀ are released from reset and normal operation occurs. The

frequency deviation is thus measured by the count made during the period t₂ to t₃ by the counters FF₁ to FF₅ (Figure 3A).

To recapitulate briefly, assume the lock and reset switch 9 is closed, so that the dividing circuit is reset and the timepiece is stopped. In this condition T_{N1} is "ON" and T_{N2}, T_{P1} and T_{P2} are "OFF". The terminal A of the driving coil L₁ will therefore be at ground (minus) potential, the terminal B will be floating, so that the said driving coil L₁ can act as a receiving coil and is able to receive a standard time signal from an external source as explained in connection with Figure 2. This standard time signal, occurring at terminal B of the coil L₁ is shaped and clamped by diodes D₁ and D₂ and sent to the control circuit flip-flop FF₂₆.

A timing chart of operation is shown conventionally in Figure 5. In this figure line 12 shows the voltage at the armature of the switch 9; line 13 represents the external standard time signal; line 14 represents a reset signal for the dividing circuitry; and line 15 is a memory order signal. From the time t₁ when the reset switch 9 is closed to the time t₂ when the external standard time signal enters, the dividing circuit is kept reset. At the latter time t₂ the reset is released and the frequency deviation measuring circuit, that is, the dividing circuit comprising the flip-flops FF₁ to FF₅ begin to count and the frequency deviation memory circuit comprising the flip-flops FF₂₀ to FF₂₄ begins writing in data from the said frequency deviation measuring circuit having been caused to do so by the memory order signal (line 15 of Figure 5). The writing in continues from time t₂ to the time t₃ when the next external standard time signal enters. At this time t₃ the writing in ceases, leaving in the memory stored data representative of the frequency deviation. At t₃ the dividing circuit is reset again and at t₄ at which the reset is released, normal operation takes place.

As will be appreciated, in this embodiment the effective division ratio is increased by the operation of the regulating circuit so that it is necessary to make the oscillation frequency of the quartz oscillator in the watch higher than the basic oscillating frequency as calculated from the basic division ratio of the dividing circuit. However, this is not a practical disadvantage. If desired, however, a regulating circuit arrangement capable of reducing the division ratio or of reducing or increasing the division ratio, could be provided.

As will now be seen the invention provides a convenient and satisfactory means whereby timing regulation can be effected fully automatically in accordance with a standard time signal produced outside the case of the timepiece by, for example, a simple generator generating said standard time signal. The

asure y the
t₂ to t₃ by
e 3A).
e the lock and
t the dividing
ce is topped.
and T_{N2}, T_{P1}
inal A of the
be at ground
will be float-
oil L₁ can act
to receive a
external source
Figure 2. This
at terminal B
clamped by
o the control

is shown con-
figure line 12
ature of the
the external
represents a
itry; and line
from the time
closed to the
rd time signal
ept reset. At
released and
g circuit, that
sing the flip-
t and the fre-
it comprising
ins writing in
cy deviation
used to do so
15 of Figure
from time t₂
ernal standard
t₃ the writing
y stored data
deviation. At
again and at
ased, normal

s embodiment
reased by the
uit so that it
ion frequency
watch higher
frequency as
sion ratio of
this is not a
d, however, a
capable of
f reducing or
could be

ation provides
eans whereby
d fully auto-
standard time
of the time-
ple generator
signal. The

timing regulation thus achieved is reliable and
of good accuracy, the range of regulation
achievable is a large one, and, in the embodi-
ment illustrated, there are no mechanically
moving parts in the apparatus for achieving
timing regulation while a relatively inexpen-
sive quartz oscillator can be used in the time-
piece.

WHAT WE CLAIM IS:—
1. A timepiece comprising a time standard
constituted by a piezo-electric crystal
oscillator; an electronic circuit including a
frequency dividing circuit driven by output
from said oscillator; time display means
driven by the divided frequency output;
receiving means in said timepiece for receiving
an externally produced standard time signal;
a frequency deviation measuring circuit for
measuring frequency deviation between the
piezo-electric crystal oscillator frequency and
a basic frequency in fixed frequency relation-
ship with said externally produced standard
time signal received by said receiving means,
a frequency deviation memory circuit for
memorising data representative of the fre-
quency deviation measured by said frequency
deviation measuring circuit; a regulating
circuit for regulating timing by controlling
under the control of the memorised data, the
effective division ratio of said frequency divid-
ing circuit; and control means for bringing
said receiving means, frequency deviation
measuring circuit, memory circuit and
regulating circuit into operation to effect
timing regulation.
2. A timepiece as claimed in claim 1
wherein said receiving means is the normal
provided driving coil of an electro-mechanical
converter which actuates the time display
means of the timepiece.

3. A timepiece as claimed in claim 1 or 2
wherein the effective division ratio of said
dividing circuit is controlled by controlling
the number of pulses produced thereby from
the output of said oscillator.
4. A timepiece as claimed in any of the
preceding claims wherein said frequency
deviation measuring circuit is constituted by
part of said frequency dividing circuit.
5. A timepiece as claimed in any of the
preceding claims wherein said frequency
dividing circuit, said frequency deviation
measuring circuit and said memory circuit
comprise each a series of master slave flip-flop
circuits.
6. A timepiece as claimed in claims 3 and 5
wherein the frequency deviation measuring
circuit comprises a first series of master slave
flip-flops; said frequency dividing circuit com-
prises said first series and a following second
series of master slave flip-flops; said memory
circuit comprises a third series of master slave
flip-flops each connected to receive and
memorise data from a respective one of the
flip-flops in said first series; a first plurality of
gates each having an input terminal connected
to a respective flip-flop in said second series
and a second input terminal connected to a
respective flip-flop in said third series; and a
second plurality of gates controlled by the
gates in said first plurality and included in a
feedback circuit across said frequency dividing
circuit.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
Lincoln House,
296—302 High Holborn,
London, WC1V 7JH.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1977
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
which copies may be obtained.



* C L M S *

1,487,955

5

the
to t_2 by
).
lock and
dividing
opped.
 T_{x2} , T_{P1}
A of the
it ground
l be float-
can act
receive a
al source
re 2. This
terminal B
mped by
e control

own con-
ce line 12
e of the
external
resents a
; and line
the time
ed to the
me signal
reset. At
ased and
rcuit, that
the flip-
d the fre-
omprising
writing in
deviation
d to do so
of Figure
1 time t_2
l standard
e writing
ored data
iation. At
in and at
l, normal

4

5

timing regulation thus achieved is reliable and of good accuracy, the range of regulation achievable is a large one, and, in the embodiment illustrated, there are no mechanically moving parts in the apparatus for achieving timing regulation while a relatively inexpensive quartz oscillator can be used in the timepiece.

WHAT WE CLAIM IS:—

1. A timepiece comprising a time standard constituted by a piezo-electric crystal oscillator; an electronic circuit including a frequency dividing circuit driven by output from said oscillator; time display means driven by the divided frequency output; receiving means in said timepiece for receiving an externally produced standard time signal; a frequency deviation measuring circuit for measuring frequency deviation between the piezo-electric crystal oscillator frequency and a basic frequency in fixed frequency relationship with said externally produced standard time signal received by said receiving means, a frequency deviation memory circuit for memorising data representative of the frequency deviation measured by said frequency deviation measuring circuit; a regulating circuit for regulating timing by controlling under the control of the memorised data, the effective division ratio of said frequency dividing circuit; and control means for bringing said receiving means, frequency deviation measuring circuit, memory circuit and regulating circuit into operation to effect timing regulation.

2. A timepiece as claimed in claim 1 wherein said receiving means is the normal provided driving coil of an electro-mechanical converter which actuates the time display means of the timepiece.

3. A timepiece as claimed in claim 1 or 2 wherein the effective division ratio of said dividing circuit is controlled by controlling the number of pulses produced thereby from the output of said oscillator.

4. A timepiece as claimed in any of the preceding claims wherein said frequency deviation measuring circuit is constituted by part of said frequency dividing circuit.

5. A timepiece as claimed in any of the preceding claims wherein said frequency dividing circuit, said frequency deviation measuring circuit and said memory circuit comprise each a series of master slave flip-flop circuits.

6. A timepiece as claimed in claims 3 and 5 wherein the frequency deviation measuring circuit comprises a first series of master slave flip-flops; said frequency dividing circuit comprises said first series and a following second series of master slave flip-flops; said memory circuit comprises a third series of master slave flip-flops each connected to receive and memorise data from a respective one of the flip-flops in said first series; a first plurality of gates each having an input terminal connected to a respective flip-flop in said second series and a second input terminal connected to a respective flip-flop in said third series; and a second plurality of gates controlled by the gates in said first plurality and included in a feedback circuit across said frequency dividing circuit.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
Lincoln House,
296—302 High Holborn,
London, WC1V 7JH.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1977
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

abodiment
ed by the
so that it
frequency
ch higher
uency as
ratio of
is not a
however, a
eable of
ducing or
could be

n provides
s whereby
ully auto-
ard time
the time-
generator
gnal. The

120

125

45

50

55

60

65

70