Multi-layer Substrate For Semiconductor Packaging

Field of Invention

[001] The present invention relates to multi-layer substrates for semiconductor packaging and methods of manufacturing such substrates.

Background

[002] Conventional semiconductor dies are mounted on leadframes. These leadframes are usually formed by coating a copper substrate with a photoresist layer, exposing a pattern on the photoresist layer using a mask, positively or negatively removing the photoresist layer and then etching away the copper to give a patterned leadframe. However, such a patterned leadframe formed by etching is not suitable for use with dies that require finer and closer ~~interconnecting~~ conductive traces than conventional leadframe. Etching inherently causes undercutting and fine conductive traces thus formed may have reliability issue for high throughput manufacturing.

[003] US Patent No. 7,795,071, assigned to Advanpack Solutions, describes a method for forming a single-layer patterned substrate for semiconductor packaging. A gang of patterned conductor layouts is formed on a steel carrier, and insulating material is injected in a mold cavity to seal the conductive traces of the patterned conductor layouts. After removing the steel carrier, a substrate containing a gang of patterned conductor layouts, is formed. Advantageously, the patterned conductor layouts are embedded or recessed in the insulating material of the substrate such that finer and closer conductive traces are fabricated effectively. The patterned conductor layouts are electrically isolated from each other, whereas on a conventional leadframe, each conductor layout corresponding to each die is electrically connected to an adjacent layout.

[004] It can thus be seen that there exists a need to form a multi-layer substrate with more complex routing of conductive traces to support future designs of integrated circuits. Advantageously, these multi-layer substrates allow separate conductor layers to be used for signal, power, digital, analogue circuits and so on.

Summary

[005] The following presents a simplified summary to provide a basic understanding of the present invention. This summary is not an extensive overview of the invention, and is not intended to identify key features of the invention. Rather, it is to present some of the inventive concepts of this invention in a generalised form as a prelude to the detailed description that is to follow.

[006] The present invention seeks to provide substrates containing two or more built-up structural layers formed on a sacrificial carrier. Each built-up structural layer comprises a conductor trace layer and an interconnect layer. Each built-up structural layer is molded in a ~~resin~~ molding compound. The multi-layer substrate is then completed by forming an outermost conductor trace layer and removing the carrier.

[007] In one embodiment, the present invention provides a multi-layer substrate comprising: a sacrificial carrier that is electrically conductive and chemically etchable; a first conductor trace layer formed on the sacrificial carrier; a second conductor trace layer and an interconnect layer disposed between the first and second conductor trace layers, wherein ~~studs~~ the interconnect layer connects selected areas between the first and second conductor trace layers.

[008] In one embodiment of the multi-layer substrate, the first conductor trace layer and the interconnect layers are encapsulated in a ~~resin~~ molding compound. The top surface of the ~~resin molding~~molded encapsulation is abrasively ground and an adhesion layer is deposited on the ground surface. The adhesion layer may be a photo-imagable polymer material or a laser-exposurable polymer material~~conductor seed layer, a polyimide layer or a woven glass fiber laminate~~. The multi-layer substrate thus comprises two or more built-up layers, each of the built-up layer is made up of a conductor trace layer, an interconnect layer and an adhesion layer, such that the outermost layer is a conductor trace layer.

[009] In another embodiment, the present invention provides a method for manufacturing multi-layer ~~semiconductor~~ substrates. The method comprises: forming a first conductor trace layer on a sacrificial carrier, wherein the first conductor trace layer contains a plurality of conductor trace

layouts; forming an interconnect layer on the first conductor trace layer, wherein the interconnect layer comprises conductor studs that connect with selected areas of the first conductor trace layer; encapsulating the first conductor trace and interconnect layers in a ~~resin~~ molding compound; abrasively grinding a surface of the molded encapsulation for planarity and to expose the ~~interconnect~~ conductor studs; depositing an adhesion layer on the ground ~~encapsulation~~ surface; repeating the above steps to form an additional built-up structure of the multi-layer substrate so that there are ~~2~~ two or more built-up structural layers; and forming an outermost conductor trace layer on the top ~~adhesion~~ build-up structural layer.

[0010] In another embodiment, the method further comprises: sealing the outermost conductor trace layer with ~~an insulating~~ a soldermask layer; selectively removing the ~~insulating~~ soldermask layer to expose areas of the outermost conductor trace layer for external ~~electrical~~ connection.

[0011] Preferably, an internal portion of the carrier is removed to leave a ~~reinforcing~~ carrier ring around the substrate or a gang of conductor trace layouts contained in the first conductor trace layer. Preferably, the first conductor trace layer is sealed with a soldermask layer and selective removal of the solder-mask layer exposes areas on the first conductor trace layer for external ~~electrical~~ connection.

Brief Description of the Drawings

[0012] This invention will be described by way of non-limiting embodiments of the present invention, with reference to the accompanying drawings, in which:

[0013] FIGs. 1A-1J illustrate structures of a two-layer substrate according to an embodiment of the present invention;

[0014] FIGs. 2A-2D, 3 and 4 illustrate methods for forming semiconductor packages using the multi-layer substrate shown in FIG. 1J;

[0015] FIGs. 5 and 6 illustrate structures of a two-layer substrate according to another embodiment of the present invention;

[0016] FIGs. 7A-7F illustrate structures of a three-layer substrate according to yet another embodiment of the present invention; and

[0017] FIG. 8 illustrates a plan view of a finished substrate obtained according to the present invention.

Detailed Description

[0018] One or more specific and alternative embodiments of the present invention will now be described with reference to the attached drawings. It shall be apparent to one skilled in the art, however, that this invention may be practised without such specific details. Some of the details may not be described at length so as not to obscure the invention. For ease of reference, common reference numerals or series of numerals will be used throughout the figures when referring to the same or similar features common to the figures.

[0019] FIGs. 1A-1J show progressive build-up of a multi-layer substrate 105 comprising two conductor trace layers according to an embodiment of the present invention. As shown in FIG. 1A, the first step in the process 100 is to provide a carrier 110 having a first surface and an opposite facing second surface. Preferably, the carrier 110 is made of a ~~low-cost~~ material having high Young's modulus of elasticity, is electrically conductive and is suitable for chemical etching, such as steel or copper. These properties of the carrier 110 allow it to be sacrificially removed partially during fabrication of the multi-layer substrate 105 and/or removed completely after a semiconductor die 10 is encapsulated. Preferably, the carrier 110 is stress-relieved or partially stress-relieved, for example, by annealing.

[0020] Subsequent process steps involve coating a surface of the carrier 110 with a photoresist, exposing the photoresist with a mask, selectively etching away the photoresist, and obtaining a patterned photoresist. By depositing a first electric conductor material 114, such as copper, over the patterned photoresist and then removing the photoresist, a patterned first conductor trace

layer 114a is formed on the carrier 110. The patterned first conductor trace layer 114a thus contains a plurality of first conductor layouts for connection with some semiconductor dies. Preferably, the first conductor material 114 is copper and a suitable depositing process is electroplating. FIG. 1B shows an enlarged part of a section through the first conductor trace layer 114a. For easier referencing, the patterned first conductor trace layer and the first conductor layouts are identified by the same reference numeral 114a. By similar photolithographic process and by depositing a second electric conductor material 118, such as copper, on a resulting patterned photoresist defining interconnecting vias, a first interconnect layer 118a made up of conductor studs 118 is thus formed on the first conductor trace layer 114a, as shown in FIG. 1C. Alternatively, the first conductor trace layer 114a and first interconnect layer 118a are formed by subtractive photolithographic processes. Various combinations of additive, semi-additive or semi-subtractive processes can be adopted to create the required patterned structure. To electrically isolate the conductor traces/studs and to encase the conductor traces/studs in an insulating or dielectric material, a gang of the first conductor layouts 114a and conductor studs 118a is disposed in a cavity or gangs of the first conductor layouts 114a and conductor studs 118a are disposed in a plurality of cavities. An insulating or dielectric molding compound, preferably preheated to a fluid state, is injected into the cavity or cavities at a melt temperature. Preferably, the fluid molding compound is injected at a positive pressure so that the molding compound is densely packed with the gang of the first conductor layouts 114a and conductor studs 118a to form a compact composite structure or a first insulator layer 120 after the molding compound has solidified; as a result, the molding compound bonds strongly onto the first conductor layouts 114a and conductor studs 118a such that during wet processing, fluid cannot enter the conductor-molding compound interfaces. A semi-finished substrate, as shown in FIG. 1D, is thus obtained. Preferably, the first insulator layer 120 comprises a molding compound containing a matrix of resin and ~~silica~~ fillers, such as epoxy resin and silica fillers. Preferably, after the first insulator layer 120 is formed, the ~~silica~~ fillers are embedded within the resin.

[0021] The semi-finished substrates shown in FIG. 1D are moved to a machining centre and the free surface of the first insulator layer 120 is made planar by abrasive grinding, to a depth when all the conductor studs 118a are exposed on the ground surface 122, as shown in FIG. 1E. Preferably, the exposed surfaces of the conductor studs 118a are leveled with or recessed in the rear surface of the first ~~insulating~~ insulator layer 120 (as seen in FIG. 1E) such that the first

~~insulating~~ insulator layer 120 defines the edges of the conductor studs and isolates the conductor studs one from one another. After grinding, the ~~silica~~ fillers in the molding compound are also exposed. Specifically, the ground surface 122 now comprises resin interposed with ~~silica~~ fillers; the ground surface 122 was found to provide strong adhesion for depositing a conductor seed layer 124, as shown in FIG. 1F. Alternatively, by increasing the rate of material removal during abrasive grinding, the surface ~~silica~~ fillers are extracted from the resin to form a plurality of dimples on the ground surface 122. The dimpled ground surface 122 provides an increased surface area to improve adhesion buildup of the next adjacent layer. Alternatively, an adhesion layer, as shown in FIG. 5, can be further deposited on the dimpled ground surface to cover the plurality of dimples for planarity and to interface with the next adjacent layer. When the first conductor material 114 is copper, the conductor seed 124 material is also copper. Suitable methods for depositing the copper seed layer 124 are electroless plating, electrolytic plating, sputtering, CVD or PVD.

[0022] By using the photolithographic process, a patterned photoresist is then formed on the conductor seed layer 124 and by electroplating copper on the patterned photoresist, a patterned second conductor trace layer 128a is obtained, as shown in FIG. 1G. The second conductor trace layer 128a is made up of a plurality of second conductor layouts 128a; each of these second conductor layouts 128a is therefore electrically connected to each of the associated first conductor layouts 114a through the associated first conductor studs 118a.

[0023] As shown in FIG. 1H, the patterned second conductor trace layer 128a is completed by sealing it with a second ~~insulating~~ insulator or dielectric layer 130. Preferably, the second ~~insulating~~ insulator layer 130 is a soldermask layer containing a photo--imageable polymer material. Preferably, the second ~~insulating~~ insulator layer 130 is screen-printed onto the patterned second conductor trace layer 128a. The second ~~insulating~~ insulator layer 130 is then exposed to radiation, such as ultra-violet, infra-red or laser radiation, through a mask, and by selective removal, selected areas 128b of the second conductor trace layer 128a are exposed through the second insulator layer 130 for external electrical connections, as shown in FIG. 1I. Further processing on the exposed second conductor trace layer 128b for solderability may include depositing a tin layer or a nickel/gold layer.

[0024] As shown in FIG. 1I, the carrier 110 is larger than the molded first insulator layer 120. Advantageously, an internal portion 110a of the carrier 110 is partially sacrificed and removed, for example by etching, so that a ring 110b remains and a finished substrate 105 is obtained, as shown in FIG. 1J. Alternatively, the carrier 110 is completely sacrificed and removed. After removing the carrier 110, the first conductor layouts 114a are exposed together with the surface of the first insulator layer 120. Preferably, the surfaces of the first conductor layouts 114a are leveled or recessed in the top surface of the first insulator layer 120 (as seen in FIG. 1J) such that insulator layer 120 defines the edges of the first conductor layouts 114a and isolates a first conductor layout from one another. As described above, the carrier 110 is made from a material with high Young's modulus and is stress-relieved; by leaving a ring 110b of the carrier on the substrate 105, the carrier ring 110b helps to maintain planarity of the finished substrate 105, at the same time, providing rigidity to the finished substrate 105 for handling and subsequent manufacturing. In another embodiment, the internal opening 110a is smaller than a gang of molded first insulator layers 120 so that a plurality of openings 110a are formed on the carrier 110, instead of just leaving a carrier ring around the entire substrate. In addition, in the peripheral area outside the ~~molded area~~ first insulator layer 120, the carrier ring 110b is formed with positioning or fiducial holes 160 (as seen in FIG. 8); in addition, if the carrier 110 is not stress-relieved before use, stress-relief slots 170 (shown in FIG. 8) may be stamped or formed in the peripheral area before the internal portions 110a are etched away or at the time when the internal openings 110a are etched away. Advantageously, the peripheral area of the carrier with positioning/fiducial holes or stress-relieved slots defines the clamping area for the above injection or compression molding of the first insulator layer 120, singulation of finished semiconductor packages or for other uses in other intermediate manufacturing processes such that the required clamping areas are located away from the delicate molded areas that contain the ~~first and second~~ conductor trace~~s~~ layouts and ~~interconnecting~~ conductor studs, thus ensuring that the subsequent processes do not damage the molded area~~s~~.

[0025] For simplicity of illustration, FIG. 2A shows the carrier ring 110b being formed around a molded first insulator layer 120. As shown in FIG. 2A, a semiconductor die 10 is connected to the first conductor layout 114a through solder bumps 20 and metal pillars 24 connections. Mounting of the die 10 is also strengthened by an underfill compound 30. In FIG. 2B, after the die 10 is mounted on the substrate 105, the entire die is encapsulated in ~~a~~ another molding compound 40. Preferably, the molding compound 40 is made from a material having similar or

identical properties with the material of the first insulator layer 120 to minimize stresses created due to property differences. Solder balls 22 may also be disposed in contact with the exposed second conductor layouts 128b for external electrical connection. In FIG. 2C, the encapsulated die is cut along singulation lines XX and YY to provide a finished semiconductor package 150 containing the substrate 105 obtained by the process 100 of the present invention.

[0026] Instead of using ~~solder bump~~ flip-chip connection, the die 10 may be wire-bonded to the first conductor layout 114a, as shown in FIG. 3, and another finished semiconductor package 150a containing the substrate 105 is obtained by the above process 100. Further, as shown in FIG. 4, a finished semiconductor package 150c may comprise two or more dies, passives or packages, including dies that are made using different semiconductor fabrication techniques.

[0027] Referring back to FIGs. 1J and 2C, around each first conductor layout 114a, some of the peripheral conductors 114b are not electrically connected to the rest of the first conductor layout 114a and they are provided to control electroplating. For example, the conductors 114b may act as "current stealers" to change the current distribution during electroplating of the conductor trace layouts 114a, the conductor studs 118 and/or the second conductor trace ~~layer~~ layouts 128a to achieve uniform electroplating thickness. Alternatively, the peripheral conductors 114b are provided to change a stress distribution on the substrate 105 by changing the composite coefficient of thermal expansion (CTE) across the substrate area.

[0028] FIGs. 5 and 6 show variations in the structures of the above embodiments. For example, as shown in FIG. 5, before disposing the conductor seed layer 124, an adhesion layer 123 is applied on the ground surface 122 of the molded first insulator layer 120 to promote adhesion of the second conductor trace layer 128a. Preferably, the adhesion layer 123 is a photo-imagable polymer material, such as polyimide or a laser-exposurable polymer material, such as epoxy~~woven glass fiber~~ laminate. In FIG. 6, a top surface of the substrate 105 is deposited with a soldermask layer 140 so that selected areas of the first conductor trace layer 114a are exposed for external electrical connection.

[0029] FIGs. 7A-7F show progressive buildup of a multi-layer substrate 105a comprising three conductor trace layers. FIG. 7A shows continued buildup of the structure of the semi-finished substrate shown in FIG. 1G. As shown in FIG. 7A, a second interconnect layer 218, comprising

second conductor studs 218, is formed on the patterned second conductor trace layer 128a by photolithographic and electroplating processes. In FIG. 7B, the conductor seed layer 124 that are not built-up by the second conductor trace layer 128a is removed, preferably by chemical etching.

[0030] In FIG. 7C, the molded first insulator layer 120 on the semi-finished substrate is over-molded with a second insulator molding 220. As in the first insulator layer, the second insulator molding preferably also contains a matrix of epoxy resin and embedded inorganic silica fillers. The second insulator molding 220 can be the same size as the first insulator molding 120. As shown in FIG. 7C, the second insulator molding 220 is larger and it encapsulates the first insulator molding 120 in a so-called molding-over-molding.

[0031] As in FIG. 1E, the free surface of the second insulator molding 220 is abrasively ground to provide a planar surface 222. The ground molding surface 222 also provides good adhesion for a second conductor seed layer 224 to be deposited and a third conductor trace layer 228a to be built-up. When the third conductor trace layer 228a is the outermost conductor trace layer of the finished substrate, the outermost conductor trace layer is sealed with an outermost insulator layer, such as a soldermask layer and selected areas of the outermost conductor trace layer are then exposed, as seen in FIG. 7F, for external electrical-connection.

[0032] In FIGs. 7E and 7F, it is shown that an internal portion of the carrier 110 is partially etched away to expose the first conductor trace layer 114a so that a reinforcement ring 110b remains on the substrate 105a before the processing on the substrate is completed. It is possible that the reinforcement ring 110b is formed after processing on the substrate 105a is completed. The resulting substrate 105a comprises a plurality of insulator layers adjoining to one another with each insulator layer having a corresponding (conductor elements) conductor trace layer and an interconnect layer embedded within. A dividing plane parallel to the contacting surfaces of the adjoining insulator~~ing~~ layers lies in-between two insulator layers such that the conductor ~~trace~~ elements in one insulator layer does not cross over the dividing plane to the adjacent insulator layer. However, the conductor ~~trace~~ elements in each corresponding insulator layer are electrically connected to one another such that the top surface of the substrate 105a is electrically connected to the rear surface of the substrate 105a. Specifically, the interconnect

layer in one insulator layer is electrically and physically connected to the conductor trace layer of the adjoining insulator~~ing~~ layer.

[0033] FIG. 8 shows a plan view of the substrate 105, 105a as seen from the top according to FIG. 1J or 7F. As seen in FIG. 8 through the opening 110a in the carrier 110, the first conductor trace layer 114a illustrates a gang of 9 conductor layouts 114a are encapsulated in a molding 120, 220. As described earlier, within each conductor layouts 114a, there are stand-alone peripheral conductors 114b that are provided as "current stealers" to adjust the current distribution during electroplating; in addition these stand-alone peripheral conductors 114b can be used to modify the composite coefficient of thermal expansion across the substrate to minimise any warpage due to thermal changes during processing. In the clamping ~~zone~~ area around the substrate 105, 105a, that is, through the thickness of the reinforcement or carrier ring 110b, there are positioning or fiducial holes 160 and stress-relief slots 170.

[0034] The above drawings illustrate forming multi-layer substrate with 2 and 3 conductor trace layers. It is possible to obtain multi-layer substrate with more than 3 conductor trace layers by forming each additional built-up layer with a conductor trace layer and an interconnect ~~stud~~ layer and encapsulating these two component layers in a ~~resin~~ molding compound. With the present invention, the multi-layer substrates allow more complex interconnect routing to support packaging of new semiconductor chips. Advantageously, the multi-layer conductor trace~~s~~ layouts can also be separately designated to carry different types of signal or power, for example, to reduce signal interference. As the feature sizes of the conductor trace layouts are not limited by the characters of etching, the multi-layer substrates according to the present invention also provide an advance in achieving circuit miniaturization.

[0035] While specific embodiments have been described and illustrated, it is understood that many changes, modifications, variations and combinations thereof could be made to the present invention without departing from the scope of the present invention. For example, it is possible to form a patterned via layer to connect a conductor trace layer with a conductor trace layer located two or more layers away in the built-up structure of the substrate; this feature will provide an additional level of interconnect routing that is not possible with conventional leadframes.

CLAIMS:

1. A ~~multi-layer~~ semiconductor substrate comprising:

~~a sacrificial carrier that is electrically conductive and chemically etchable;~~

a first conductor trace layer ~~formed on the sacrificial carrier~~;

a second conductor trace layer; and

a (first) interconnect layer disposed between the first and second conductor trace layers, wherein studs connect selected areas between the first and second conductor trace layers;

wherein the first conductor trace layer and the (first) interconnect layer are encapsulated in a molding compound.

2. ~~A multi-layer~~ The semiconductor substrate according to claim 1, wherein the ~~first conductor trace layer and (first) interconnect stud layer are encapsulated in a resin~~ molding compound comprises resin and fillers.

3. The ~~A multi-layer~~ semiconductor substrate according to claim 2, wherein the ~~resin molding~~ molded encapsulation is abrasively ground to expose the (first) interconnect studs and the ground surface is then deposited ~~a conductor seed layer~~the second conductor trace layer on the exposed interconnect studs.

4. The ~~A multi-layer~~ semiconductor substrate according to claim 3, wherein the second conductor trace layer ~~the conductor seed layer~~ is built on an adhesion layer to promote adhesion of the second conductor trace layer.

5. The ~~A multi-layer~~ semiconductor substrate according to claim 4, wherein the adhesion layer comprises a polyimide or ~~a woven glass fiber~~ an epoxy laminate.

6. The ~~A multi-layer~~ semiconductor substrate according to claim 3 or 4, further comprising a second insulating layer deposited on the second conductor trace layer, so that the second insulating layer is operable to be selectively removed to expose areas of the second conductor trace layer for external electrical connections.

7. The ~~A multi-layer~~ semiconductor substrate according to claim 3 or 4, further comprising one or more intermediate built-up layers, with each intermediate built-up layer comprising a conductor trace ~~component~~ layer and an interconnect ~~stud component~~ layer, and each built-up layer is encapsulated in a ~~resin~~ molding compound so that the ~~molding~~ molded encapsulation surface is abrasively ground ~~and then deposited with a conductor seed layer~~ to expose the interconnect layer.

8. The ~~A multi-layer~~ semiconductor substrate according to claim ~~6 or 7~~1, further comprising a sacrificial carrier that is electrically conductive and chemically etchable, wherein an internal portion of the sacrificial carrier is etched away so that a reinforcement carrier ring remains on a peripheral area of the substrate or around a gang of conductor layouts.

9. The semiconductor substrate according to claim 7, wherein a dividing plane or an adhesion layer lies in-between two adjacent intermediate layers.

10~~9~~. A method for manufacturing a ~~multi-layer~~ semiconductor substrate ~~for semiconductor packaging, the method~~ comprising:

forming a first conductor trace layer on a sacrificial carrier, wherein the first conductor trace layer ~~contains~~ comprises a plurality of conductor layouts;

forming an interconnect layer on the first conductor trace layer, wherein the interconnect layer comprises studs that connect with selected areas of the first conductor trace layer;

encapsulating the first conductor trace and interconnect layers in a ~~resin~~ molding compound;

abrasively grinding a surface of the molded encapsulation for planarity and to expose the interconnect studs; and

~~depositing an adhesion layer on the ground encapsulation surface;~~

repeating the above steps to form an additional built-up ~~structure~~ structural layer of the ~~multi-layer~~ substrate so that there are ~~2~~ two or more built-up structural layers~~; and~~

~~forming an outermost conductor trace layer on the top adhesion layer~~.

11. The manufacturing method according to claim 10, wherein encapsulating of the first conductor trace and interconnect layer comprises disposing the first conductor trace and interconnect layer in a cavity and injecting a molding compound into the cavity to densely packed the first conductor trace and interconnect layer.

~~10~~12. ~~A~~ The manufacturing method according to claim ~~9~~10, wherein the ~~resin~~ molding compound comprises a resin and ~~silica~~ fillers.

~~11~~13. The manufacturing ~~A~~ method according to claim ~~9~~ 10 or ~~10~~11, wherein abrasive grinding of the molded encapsulation comprises exposing the ~~silica~~ fillers to promote adhesion of the next contiguous layer.

~~12~~14. The manufacturing ~~A~~ method according to claim ~~9~~ 10 or ~~10~~11, wherein abrasive grinding of the molded encapsulation comprises extracting surface ~~silica~~ fillers to create a dimpled surface to promote adhesion of the next contiguous layer.

~~13~~15. The manufacturing method according to claim 10, further comprising depositing an adhesion layer on the ground encapsulation surface.

16. The manufacturing ~~A~~ method according to ~~any one of claims 9-12~~claim 14, wherein depositing the adhesion layer comprises depositing ~~a conductor seed layer,~~ a polyimide layer or ~~a woven glass fiber~~ an epoxy laminate.

17. The manufacturing method according to claim 10, further comprising forming an outermost conductor trace layer after forming the built-up structural layers.

~~14~~18. The manufacturing ~~A~~ method according to claim 16~~9~~, further comprising:

sealing the outermost conductor trace layer with an insulating layer; and

selectively removing the insulating layer to expose areas of the outermost conductor trace layer for external electrical connection.

~~15~~19. The manufacturing ~~A~~ method according to claim ~~14~~10, further comprising removing an internal portion of the sacrificial carrier to expose the first conductor trace

layer and leaving a ~~reinforcing~~ reinforcement carrier ring around a periphery of the substrate or around a gang of conductor layouts located in the first conductor trace layer.

~~16~~20. The manufacturing ~~A~~ method according to claim ~~15~~18, further sealing a soldermask layer on the first conductor trace layer and selectively removing the soldermask layer to expose areas of the first conductor trace layer for external electrical connection.

~~17. A multi-layer substrate obtained according to any one of claims 9-16, wherein the conductor trace layers are defined for carrying separate signals and/or power types.~~

21. A semiconductor substrate comprising:

a first conductor trace layer;

a second conductor trace layer;

a first interconnect layer disposed between the first and second conductor trace layers, wherein the first interconnect layer connects selected areas between the first and second conductor trace layers; and

a first insulator layer having a first surface and a second surface opposite the first surface, wherein the first insulator layer encapsulates the first conductor trace layer and the first interconnect layer between the first and second surface, so that the first conductor trace layer is exposed on the first surface and the first interconnect layer is exposed on the second surface.

22. The semiconductor substrate according to claim 21, wherein the first insulator layer is formed by densely packing a molding compound in one or more cavities by injection or compression molding.

23. The semiconductor substrate according to claim 21, wherein the first insulator layer comprises a molding compound containing a matrix of resin and fillers, and the fillers are embedded within the resin in the compact composite structure.

24. The semiconductor substrate according to claim 23, wherein the second surface of the first insulator layer comprises a resin surface interposed with exposed fillers.

25. The semiconductor substrate according to claim 24, wherein the second surface of the first insulator layer further comprises a plurality of dimples on the resin surface.

26. The semiconductor substrate according to claim 25, further comprising an adhesion layer disposed on the resin surface, wherein the adhesion layer covers the plurality of dimples to form a planar surface.

27. The semiconductor substrate according to claim 21, further comprising a second insulator layer disposed on the second conductor trace layer, wherein selected areas of the second conductor trace layer is exposed through the second insulator layer for electrical connections.

28. The semiconductor substrate according to claim 21, further comprising:

a second interconnect layer connected to selected areas of the second conductor trace layer; and

a second insulator layer encapsulates the second conductor trace layer and the second interconnect layer, so that the second conductor trace layer is exposed.

29. The semiconductor substrate according to claim 28, further comprising:

a third conductor trace layer connected to the second interconnect layer; and

a third insulator layer disposed to seal the third conductor trace layer, wherein selected areas of the third conductor trace layer is exposed through the third insulator layer for electrical connections.

30. The semiconductor substrate according to claim 28, wherein the size of the second insulator layer is larger than the first insulator layer and the second insulator layer encapsulates the first insulator layer in an overmolding.

31 The semiconductor substrate according to claim 28, wherein the size of the second insulator layer is the same as the size of the first insulator layer.

32. A semiconductor substrate comprising:

a plurality of insulator layers adjoining to one another, wherein each insulator layer has a first surface and a second surface opposite the first surface and comprising:

a conductor trace layer; and

an interconnect layer;

wherein each insulator layer encapsulates the conductor trace layer and the interconnect layer between the first and second surfaces, so that the conductor trace layer is exposed on the first surface and the interconnect layer is exposed on the second surface.

33. The semiconductor substrate according to claim 32, further comprising:

an outermost conductor trace layer electrically connected to the interconnect layer exposed on a rear surface of the semiconductor substrate; and

an outermost insulator layer disposed on the rear surface of the semiconductor substrate to seal the outermost conductor trace layer, so that selected areas of the third conductor trace layer is exposed through the outermost insulator layer for electrical connections.

34. The semiconductor substrate according to claim 32, wherein the size of one insulating layer is larger than the adjacent insulator layer and the larger insulator layer encapsulates the smaller insulator layer in an overmolding.

35. The semiconductor substrate according to claim 32, wherein the size of one insulator layer is the same as the adjacent insulator layer and the plurality of insulator layers is built up upon one another.

36. The semiconductor substrate according to claim 32, 34 or 35, wherein each of the plurality of insulator layers is formed by densely packing a molding compound in one or more cavities by injection or compression molding.

37. The semiconductor substrate according to claim 27, 28, 29 or 32, wherein a dividing plane parallel to the contacting surfaces of adjoining insulator layers lies in-between the adjoining insulator layers, and the conductor trace layer in one insulating layer does not cross over the dividing plane to the adjacent insulating layer.

38. The semiconductor substrate according to claim 27, 28, 29 or 32, further comprising an adhesion layer disposed between adjacent insulator layers to promote adhesion of one insulator layer to the adjacent insulator layer.

39. The semiconductor substrate according to claim 38, wherein the adhesion layer comprises a photo-imagable polymer or a laser-exposurable polymer.

40. The semiconductor substrate according to claim 21 or 32, wherein the top surface of the semiconductor substrate comprises surfaces of an insulator layer and a conductor trace layer, wherein the conductor trace layer is leveled or recessed in the surface of the insulator layer and the edges of the conductor trace layer is defined by the insulator layer.

41. The semiconductor substrate according to claim 40, wherein the conductor trace layer comprises one or more conductor layouts for connection with semiconductor dies.

42. The semiconductor substrate according to claim 41, further comprising a plurality of peripheral conductors disposed around and isolated from a plurality of conductor trace layouts, wherein a coefficient of thermal expansion of the semiconductor substrate is modified.

43. The semiconductor substrate according to claim 41, further comprising a sacrificial carrier disposed on the top surface of the semiconductor substrate, wherein the sacrificial carrier comprises one or more internal openings that exposes the one or more conductor layouts.

44. The semiconductor substrate according to 42, wherein the sacrificial carrier is larger than the semiconductor substrate and part of the sacrificial carrier overhangs outside the periphery of the semiconductor substrate to define a clamping area.

45. The semiconductor substrate according to claim 43, wherein the sacrificial carrier forms a carrier ring around the periphery of the semiconductor substrate.

46. The semiconductor substrate according to claim 43, wherein the semiconductor substrate comprises a gang of insulator layers supported by the sacrificial carrier, and each insulator layer corresponds to one internal opening.

47. The semiconductor substrate according to 21 or 32, further comprising a soldermask layer disposed on the top surface of the semiconductor substrate and sealed the conductor trace layer, so that selected areas of the conductor trace layer is exposed through the soldermask layer for electrical connections.

48. A semiconductor package comprising:

a semiconductor substrate according to claim 1, 21 or 32, wherein the conductor trace layer comprises a conductor layout;

one or more semiconductor dies disposed on the semiconductor substrate, wherein the semiconductor die is connected to the conductor layout; and

a molding compound disposed on the semiconductor substrate and encapsulates the semiconductor die.

49. A method of manufacturing a semiconductor substrate comprising:

providing a sacrificial carrier;

forming a first conductor trace layer on the sacrificial carrier;

forming a first interconnect layer on the first conductor trace layer;

forming a first insulator layer to encapsulates the first conductor trace layer and the first interconnect layer;

grinding the first insulator layer to expose the first interconnect layer; and

forming a second conductor trace layer on the ground first insulating layer.

50. The manufacturing method according to 49, wherein the first conductor trace layer forms one or more conductor trace layouts, the method of manufacturing further comprising forming a plurality of peripheral conductors around and isolated from the conductor trace layouts.

51. The manufacturing method according to 49, wherein the first insulator layer is formed by densely packing a molding compound in one or more cavities by injection or compression molding.

52. The manufacturing method according to claim 49, wherein the step of forming the first insulator layer comprising:

disposing the sacrificial carrier with the conductor trace layer and the interconnect layer formed thereon in one or more cavities;

injecting a molding compound into the cavity at a positive pressure, wherein the molding compound densely packed the conductor trace layer and the interconnect layer in the cavity; and

solidifying the molding compound to form a compact composite structure with the conductor trace layer and the interconnect layer.

53. The manufacturing method according to claim 52, wherein the sacrificial carrier with the conductor trace layer and the interconnect layer formed thereon is disposed in a plurality of cavities to form a gang of insulator layers on the sacrificial carrier.

54. The manufacturing method according to claim 52, wherein the insulator layer comprises a molding compound containing a matrix of resin and fillers, and the fillers are embedded within the resin in the compact composite structure.

55. The manufacturing method according to claim 49, wherein

grinding a surface of the insulator layer forms an abraded planar ground surface, wherein the interconnect layer is leveled or recessed in the planar ground surface and the edges of the interconnect layer is defined by the insulator layer.

56. The manufacturing method according to claim 55, wherein the insulator layer comprises a molding compound containing a matrix of resin and fillers, and the ground surface exposes a surface of resin interposed with fillers.

57. The manufacturing method according to claim 56, wherein the fillers exposed on the ground surface are extracted from the resin during abrasive grinding to form a plurality of dimples on the ground surface.

58. The manufacturing method according to claim 57, wherein after the step of grinding of the first insulator layer, the manufacturing method further comprises depositing an adhesion layer on the ground surface, wherein the adhesion layer covers the plurality of dimples to form a planar surface.

59. The manufacturing method according to claim 49, further comprising:

sealing the second conductor trace layer with a second insulator layer and exposing selected areas of the second conductor trace layer through the second insulator layer for electrical connections.

60. The manufacturing method according to claim 59 comprises forming additional build-up layers including:

forming a third conductor trace layer on the second insulator layer; and

repeating the steps to form each additional build-up layer.

61. The manufacturing method according to claim 49, further comprising:

forming a second interconnect layer on the second conductor trace layer;

forming a second insulator layer to encapsulate the second conductor trace layer and the second interconnect layer; and

grinding the second insulator layer to expose the second interconnect layer.

62. The manufacturing method according to claim 61 comprises forming additional build-up layers including:

forming a third conductor trace layer on the second insulator layer; and

repeating the steps to form each additional build-up layer;

63. The manufacturing method according to claim 61, wherein the size of the second insulator layer is larger than the first insulator layer and the second insulator layer encapsulates the first insulator layer in an overmolding.

64. The manufacturing method according to claim 61, wherein the size of the second insulator layer is the same as the size of the first insulator layer.

65. The manufacturing method according to claim 61, wherein after the step of grinding of the first insulator layer, the manufacturing method further comprises depositing an adhesion layer on the first insulating layer, and forming the second conductor trace layer on the adhesion layer.

66. The manufacturing method according to claim 61, further comprising:

removing the sacrificial carrier to expose the first insulator layer and the first conductor trace layer, wherein the first conductor trace layer is leveled or recessed in the exposed surface of the first insulator layer and the edges of the first conductor trace layer is defined by the first insulator layer.

67. The manufacturing method according to claim 66, wherein the sacrificial carrier is partially removed to form a plurality of openings exposing the first conductor trace layer.

68. The manufacturing method according to claim 66, wherein the internal portion of the sacrificial carrier is removed to form a carrier ring around the periphery of the semiconductor substrate.

69. The manufacturing method according to claim 68, wherein the sacrificial carrier is larger than the first insulator layer and part of the carrier ring overhangs outside the periphery of the semiconductor substrate to define a clamping area.

70. The manufacturing method according to claim 66, further comprises sealing the exposed first insulator layer and the first conductor trace layer with a soldermask layer, and exposing selected areas of the first conductor trace layer through the soldermask layer for electrical connections.

71. A method of manufacturing a semiconductor package comprising:

forming a semiconductor substrate according to claim 66; wherein the first conductor trace layer comprises one or more conductor layouts;

mounting one or more semiconductor dies on the semiconductor substrate, wherein each semiconductor die is connected to a corresponding conductor layout; and

encapsulating the semiconductor die with a molding compound.