

Abstract of the Disclosure

"INTERFACE CIRCUIT FOR USE IN A
SEMICONDUCTOR INTEGRATED CIRCUIT"

5 To an input terminal (11) is connected one end of
the source-to-drain current path of an NMOS (12) the
gate of which is connected to Vcc. The other end of
the current path of the NMOS (12) is connected by a
protection circuit (13) comprised of a PMOS (16) and an
NMOS (17) to the common gates of a PMOS (14) and an
10 NMOS (15) in the input stage of an internal circuit.
In the protection circuit, the PMOS (16) has its source
and gate connected to Vcc and its drain connected to
the common gates of the PMOS (14) and the NMOS (15),
while the NMOS (17) has its source and gate connected
15 to Vss and its drain connected to the common drains of
the PMOS (14) and the NMOS (15).

(Please note that Figure 1 should accompany the abstract when published.)