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Bulk and Strained Silicon on Insulator Using Local Selective Oxidation

Field of the Invention

This invention relates to forming bulk or strained Si/SiGe layered regions adjacent to or on an insulator and more particularly to local selective oxidation of SiGe for forming an insulator region underneath semiconductor regions for device applications such as complementary metal-oxide-semiconductor (CMOS) field effect transistors (FET's), modulation-doped field-effect transistors (MODFET's), dynamic random access memories (DRAM's), mixed DRAM and CMOS, static random access memories (SRAM's), BiCMOS, and rf.

Background of the Invention

In silicon semiconductor technology, the only way to achieve insulating substrates is by resorting either to silicon on insulator (SOI), silicon on sapphire (SOS), or etch and bond back to achieve SOI. The main advantage of using an insulating substrate in CMOS and high speed FET's is to reduce the parasitic junction capacitance and the short channel effects and thus, increase the speed performance of the devices. One major problem with all of the above methods is that the insulator covers the

entire wafer and consequently, the entire device area including underneath the ohmic contacts and channel of a FET. The buried oxide over an entire wafer results in the well known 'floating body' problem, since the semiconductor substrate is floating with respect to the channel. This problem has adverse affects on threshold voltage control and circuit operation. The other problem with the above solutions is that they are far more expensive than regular bulk silicon substrates. In addition, there is no simple way of getting strained silicon on insulator, which would have higher electron and hole transport properties.

Summary of the Invention

In accordance with the present invention, a method for forming buried oxide regions below a region of a single crystal semiconductor layer is described comprising the steps of selecting a single crystal silicon substrate, forming a first epitaxial layer of constant or graded SiGe on the upper surface of the substrate having a first rate of oxidation. This layer can be either strained or relaxed SiGe or lattice matched SiGeC. Then forming a second epitaxial layer containing silicon on the first layer having a second rate of oxidation less than the first rate of oxidation, forming a mask over the second layer, patterning the mask to form openings in the mask, and oxidizing through the mask openings the second layer and the first layer whereby an oxide region forms having portions replacing portions or all of the first layer

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underneath the second layer.

The invention further provides forming FET's with its channel in the second layer above remaining portions of the first layer.

Brief Description of the Drawing

These and other features, objects, and advantages of the present invention will become apparent upon consideration of the following detailed description of the invention when read in conjunction with the drawing in which:

Figs. 1 and 2 are cross section views of a layered structure illustrating the steps in practicing the invention.

Fig. 3 is a cross section view along the line 3-3 of Fig. 2 after the oxidation step illustrating one embodiment of the invention.

Fig. 4 is a graph of the oxidation rate of silcon versus boron concentration at various temperatures and ambients.

Fig. 5 is a TEM of a fabricated sample of the embodiment shown in Fig. 3; and

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Fig. 6 is a cross section view of a second embodiment of the invention illustrating a plurality of FET's.

Fig. 7 is a cross section view of a layered structure illustrating an additional step of removing the oxide formed during the step of oxidation.

Fig. 8 is a cross section view illustrating an additional step of oxidation.

Description of the Preferred Embodiments

Referring to Fig. 1, a cross section view of a layered structure 12 is shown to illustrate initial process steps. First, a single crystal semiconductor substrate 14 is selected which may be Si, SiGe, etc. Next, an epitaxial layer 16 of constant or graded $Si_{1-x}Ge_x$ or $(Si_{1-x}Ge_x)_aC_{1-a}$ is formed on the upper surface 15 of substrate 14. For a description of UHV-CVD methods for growing silicon containing films, reference is made to US Patent No. 5,298,452 by B.S. Meyerson which issued Mar. 29, 1994 entitled "Method and Apparatus for Low Temperature, Low Pressure Chemical Vapor Deposition of Epitaxial Silicon Layers" which is incorporated herein by reference. Epitaxial layer 16 may have a Ge content X in the range from 0.15 to 0.25. Epitaxial layer 16 has a first rate of thermal oxidation at a specified temperature and ambient. The

ambient may include oxygen, water vapor and/or HCl. The constant or graded composition of epitaxial layer 16 is required to grow epitaxially even where layer 14 and 16 have different lattice constants, and is selected to have a first rate of thermal oxidation. The thickness of epitaxial layer 16 is adjusted to be below or above the critical thickness to provide a strained or relaxed layer respectively. For a description of forming relaxed layers of SiGe, reference is made to US Patent 5,659,187 by F.K. LeGoues and B.S. Meyerson which issued Aug. 19, 1997 entitled "Low Defect Density/Arbitrary Lattice Constant Heteroepitaxial Layers" which is incorporated herein by reference.

Next, an epitaxial layer 20 of Si or $Si_{1-Y}Ge_Y$ is formed on the upper surface 17 of epitaxial layer 16. Epitaxial layer 20 may have a constant or graded Ge content Y where Y is less than X and may be zero. The composition of layer 20 is chosen so that layer 20 has a second rate of oxidation less than the rate of oxidation of layer 16 and has desired electrical properties.

Next, a mask 24 is formed over the upper surface 21 of layer 20. Mask 24 may be a blanket layer of silicon nitride or of other material such as a material that is slow or resistant to oxidation or a material which is already an oxide. Silicon nitride is a preferred material because it can be selectively removed with respect to an oxide i.e. silicon dioxide. Mask 24 is patterned to form openings 26 as shown in Fig. 2. Openings 26 may extend along

a path or pattern to form a mask shape 29 or a number of mask shapes 30 shown in Fig. 2. Mask shapes 30 may form a rectangle, square, and/or circle. Other shapes may also be formed by the pattern of openings 26. Mask shapes 30 may be a plurality of rectangles and/or squares having dimensions of 1μm by 1μm or less. Mask shapes and size may be selected to accomodate one device on a single area of Si or SiGe surrounded entirely by oxide with a remaining portion or no portion of SiGe below in contact with substrate 14.

Next, layered structure 12 is placed in an oxidizing ambient at a temperature to oxidize epitaxial layers 16 and 20 through openings 26 and hence around the edges of masks shapes 30. Dependent on the three dimensional composition profile of Ge in SiGe, the three dimensional doping profile of boron in layers 16 and 20 and the time of oxidation, oxide 33 and 34 are formed as shown in Fig. 3 could and termination layuer 16' or extend through layer 16'and terminate in substrate 14. The oxidizing ambient may be wet thermal oxidation in steam, oxygen and/or hydrochloric acid at a temperature in the range from 700°C to 950°C and preferably in the range from 700°C to 800°C. For example at 750°C, Si has an oxidation rate in the range from 0.5 to 1nm/min. SiGe with 7% Ge has an oxidation rate of about 3.5nm/min. SiGe with 16% Ge has an oxidation rate of about 5.2nm/min. SiGe with 53.5% Ge has an oxidation rate of about 44nm/min. SiGe with 76.6% Ge has an oxidation rate of about 66nm/min. For more data on oxidation rates

of SiGe as a function of temperature and as a function of composition for rapid thermal dry and wet oxidation (RTO), reference is made to a publication by U. Konig and J. Hersener, entitled "Needs of Low Thermal Budget Processing in SiGe Technology" Solid State Phenomena Vols. 47-48 (1996) pp. 17-32 published by Scitec Publications, Switzerland.

Fig. 3 is a cross section view along the line 3-3 of Fig. 2 after oxidation of epitaxial layers 16 and 20 around the edges of mask 29 through openings 26 shown in Fig. 2. As shown in Fig. 3, epitaxial layer 20 is totally consumed by oxide regions 33 and 34 except below mask shape 29. Epitaxial layer 16 is almost or totally consumed below openings 26 and extends laterally in layer 16 below layer 20'. The oxide formed is $Si_rGe_sO_2$ where r and s have values in the range from greater than 0 to 2 dependent on the Ge content in layer 16 as a function of thickness and on the oxidation conditions.

Oxides 33 and 34 extend in layer 16 underneath layer 20' where layer 16' has a rate of oxidation greater than the rate of oxidation of layer 20' which is controlled by the grading of Ge in SiGe and by the doping profile of boron, if any is present. Boron may be doped up to 10^{21}atoms/cc to enhance oxidation of SiGe. The amount of germanium provides a corresponding increase in the oxidation rate. The amount of boron provides a corresponding increase in oxidation rate as shown in Fig 4. In Fig. 4, the

ordinate represents oxidation rate (Å/min) and the abscissa represents boron concentration (cm^{-3}). Curve 41 shows the oxidation rate of silicon as a function of boron concentration at 700°C in oxygen at 1 atmosphere pressure. Curve 42 shows the oxidation rate of silicon as a function of boron concentration at 600°C in oxygen and steam at 10 atmospheres pressure also known as High Pressure Oxidation (HIPOX). Curve 43 shows the oxidation rate of silicon as a function of boron concentration at 700°C in oxygen and steam at 10 atmospheres pressure. HIPOX may occur at pressures in the range from 1 to 20 atmospheres and typically at 12 atmospheres in an oxygen containing ambient. The presence of both Ge and B provide a cumulative increase in the oxidation rate. Thus three dimensional profiles of Ge composition in SiGe in layer 16 and three dimensional profiles of boron concentration in a layers 14, 16 and 20 can provide a predetermined profile as a function of time of the peripheral surface or leading edges 35 and 36 of oxides 33 and 34 respectively. Arrows 37 and 38 show the respective lengths l_1 and l_2 of oxides 33 and 34 extending underneath mask shape 29. Layer 20' is also oxidized with respect to mask shape 29 but extends much less underneath mask shape 29 due to the lower oxidation rate. With the oxidation of Si and SiGe layers, the thickness of the resulting oxidized material increases as shown (not to scale) in fig. 3.

By continuing the step of oxidation at one or more temperatures as a function of time, the lengths l_1 and l_2 which are

are equal for constant composition in the growth plane of layers 16 and 20 may be determined or controlled. The spacing d shown by arrow 39 may likewise by determined or controlled. The spacing d allows ohmic contact to layer 16' and substrate 14 to control the voltage on the body of a field effect transistor formed in layer 20' and thus prevent the floating bodyu effect due to accumulated charge. Typically, spacing d would be less than the gate length of a FET. Oxides 33 and 34 may join together for the case where spacing d is zero in which case layer 20' would be isolated electrically from substate 14.

Fig. 5 is a Transmission Electron Microscope (TEM) of a fabricated sample of the embodiment of Fig. 3. Fig. 5 shows a substantial correspondence to the view in Fig. 3. In Fig. 5, l_1 and l_2 are about 0.17μm. The spacing d is about 0.15μm. Mask shape 29 has a width of 0.5μm. In Fig. 5, like reference numerals are used for the apparatus in Fig. 3 and incorporate the same materials as described with respect to Fig. 3.

Fig. 6 is a cross section view of a FET's 52 and 53. In Fig. 6, like reference numerals are used for the same structural elements as shown in Fig. 3. Mask shape 29 (not shown) which may be silicon nitride is removed. A gate dielectric 56 such as silicon dioxide may be formed above layer 20'for transistors 52 and 53, respectively. A polysilicon layer may be formed over gate dielectric 56 and patterned to form gate electrode 57 for

transistors 52 and 53, respectively. Using gate electrode 57, source region 60 and drain region 61 may be formed by ion implantation and ohmic contact implants may be formed extending to the upper surface of oxides 32, 33 and 34. A gate sidewall spacer may be formed on the sidewalls of gate electrode 57 (not shown) prior to forming self aligned ohmic contact implants. With ohmic contacts extending to the surface of oxides 32, 33 and 34, parasitic junction capacitances with layer 16' are reduced because of the three times lower dielectric constant of oxide compared to Si, in addition to the absence of a p-n junction. For a channel width of .13μm, the parasitic junction capacitance of source 60 and drain 61 may be less than 0.02 $fF/\mu m^2$. By positioning oxide 32, 33 and 34 underneath source 60 and drain 61, short channel effects are reduced by preventing a depletion region from extending into the channel as the drain bias voltage is increased. FET 52 may be n-type and FET 53 may be p-type to form CMOS circuits. Each FET source and drain may be doped with the appropriate dopant by masking off the other FET reserved for the opposite dopant during ion implantation. A CMOS circuit is well know in the art where the drain of one FET is couple to the source of the other via lead 66 to form an output. The gate electrodes are coupled together via lead 67 to form an input. Ground and a power supply voltage are coupled to the remaining source and drain of respective FET's via leads 68 and 69.

Fig. 7 is a cross section view of a layered structure 70

similar to the structure shown in Fig 3 but with oxide 33 and 34 removed. Oxide 33 and 34 may be removed by etching such as by etching with buffered HF.

Subsequent to removal of oxide 33 and 34, exposed layers 14, 16' and 20' may be exposed to an oxidation ambient to resume oxidation of layer 16' and to a lesser extent layers 14 and 20' depending upon the oxidation rate. Oxide 33 and 34 may act to block or slow down oxidation of layer 16'. Thus removal of oxide 33 and 34, speeds up oxidation of layer 16'.

Fig. 8 is a cross section view of layered structure 74 after substrate 14 and layers 16' and 20' are further oxidized as shown by oxide regions 77 and 78.

The steps of oxide removal and oxidation of the layered structure in an oxidizing ambient may be repeated a number of times. After the desired structure has been formed, a dielectric such as silicon oxide, may be used to fill in the voids formed by oxide removal. Chemical mechanical processes may be used to form a planar upper surface for further processing to form useful semiconductor devices.

In Figs. 7 and 8, like references are used for structures corresponding to the apparatus of Fig. 3.

While there has been described and illustrated a process for forming buried oxide regions below a region of a single crystal semiconductor layer which is under strain or relaxed with ohmic contact to the substrate and a FET structure with submicron channel lengths for device and circuit applications such as CMOS, MODFET's, DRAM's, SRAM's, rf, BiCMOS and mixed DRAM and CMOS, it will be apparent to those skilled in the art that modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.



CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A method for forming buried oxide regions below a region of a single crystal semiconductor layer comprising the steps of:

selecting a single crystal silicon substrate,

forming a first epitaxial layer selected from the group consisting of $Si_{1-x}Ge_x$ and $(Si_{(1-x)}Ge_x)_aC_{1-a}$ on the upper surface of said substrate, said first layer having a first rate of oxidation,

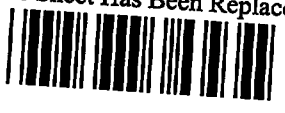
forming a second epitaxial layer containing silicon on said first layer, said second layer having a second rate of oxidation less than said first rate of oxidation,

forming a mask over said second layer,

patterning said mask to form openings in said mask, and

oxidizing through said mask openings said second layer and said first layer whereby an oxide region forms in said first and second layers with portions of said oxide region replacing portions of said first layer underneath said second layer.

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2. The method of claim 1 wherein said step of oxidizing continues for a time to form said oxide region with said portions of said oxide region extending a predetermined distance underneath said second layer.

3. The method of claim 2 further including the step of positioning apart two mask openings to provide two respective portions of said oxide regions underneath said second layer spaced apart by a predetermine distance.

4. The method of claim 1 wherein one of said openings extends along a path to form a mask shape.

5. The method of claim 4 wherein said mask shape is selected from the group consisting of a rectangle, square, and circle.

6. The method of claim 1 wherein said openings form a plurality of rectangles out of said mask corresponding to the dimensions of active MOS devices, respectively.

7. The method of claim 6 wherein said plurality of rectangles out of said mask are 1μm by 1μm or less.

8. The method of claim 6 wherein said step of oxidizing continues for a time to leave a limited area in the center of said rectangle where said first epitaxial layer has not been oxidized.

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9. The method of claim 8 further including the step of forming source and drain regions in said second layer to define a channel therebetween above said limited area of said first epitaxial layer to avoid the floating body effect of a FET.

10. The method of claim 9 further including the steps of forming a gate dielectric and a gate electrode over said channel to form a FET.

11. The method of claim 8 further including the step of forming ohmic contact ion implantation in said source and drain regions over said oxide regions whereby the parasitic junction capacitances are reduced.

12. The method of claim 1 wherein said oxidizing step includes wet thermal oxidation at a temperature in the range from 700°C to 800°C.

13. The method of claim 1 wherein said oxidizing step includes high pressure oxidation (HIPOX) at a temperature in the range from 650°C to 800°C.

14. The method of claim 1 further including the step of removing a portion of said oxide formed by said step of oxidizing.

15. The method of claim 14 further including the step of

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removing substantially all of said oxide formed by said step of oxidizing.

16. The method of claim 14 further including the step of continuing said step of oxidizing after said step of removing.

17. The method of claim 16 further including the step of repeating said steps of removing and oxidizing a plurality of times.

18. The method of claim 1 wherein said step of forming a mask includes the step of forming a layer of silicon nitride.

19. The method of claim 1 wherein said step of forming said first epitaxial layer includes forming a layer of graded composition.

20. The method of claim 19 wherein said step of forming said first epitaxial layer includes forming a layer having a upper surface with lattice parameters larger than the lattice parameters of said second layer to provide tensile strain in said second layer.

21. The method of claim 1 wherein said step of forming said first epitaxial layer includes the step of growing said first epitaxial layer until it relaxes to a lattice constant that is

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larger than the lattice constant of said second epitaxial layer to be formed whereby said second epitaxial layer when formed will be under tensile strain to have high electron and hole mobilities.

22. The method of claim 1 wherein said oxidizing step continues for a time to form said oxide region downward into said substrate.

23. The method of claim 1 further including the step of doping regions of said first layer with boron to promote the rate of oxidation.

24. The method of claim 1 wherein said first layer is graded in composition of Ge to promote the rate of oxidation.

25. A structure for forming an electronic device therein comprising:

a single crystal silicon substrate,

a first epitaxial layer selected from the group consisting of $Si_{1-x}Ge_x$ and $(Si_{(1-x)}Ge_x)_aC_{1-a}$ on the upper surface of said substrate,

a second single crystal layer containing silicon on said first layer, and

first and second oxide regions spaced apart, each said first and second oxide regions extending in said first region below said second layer.

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26. The structure of claim 25 wherein said first and second oxide regions are formed in said first epitaxial layer and said second single crystal layer.

27. The structure of claim 25 wherein said first and second oxide regions are spaced apart in said first layer in the range from 0.01 to 0.5μm.

28. The structure of claim 25 wherein said first and second oxide regions enclose a portion of said first layer.

29. The structure of claim 28 wherein said enclosed portion of said first layer forms at its upper surface a shape selected from the group consisting of a rectangle, square, and circle.

30. The structure of claim 29 further including a plurality of enclosed portions of said first layer, each enclosed portions of said first layer less than 1μm by 1μm.

31. The structure of claim 28 wherein said second layer between said first and second oxide regions is underneath and in contact with said enclosed portion of said first layer.

32. The structure of claim 25 wherein said first epitaxial layer includes a layer of graded composition of Ge.

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33. The structure of claim 25 wherein said first epitaxial layer includes boron doping.

34. The structure of claim 25 wherein said second single crystal layer is under strain due to the lattice parameters of the upper surface of said first layer.

35. The structure of claim 25 wherein said first and second oxide regions extend through said first layer into said substrate.

36. The structure of claim 25 further including spaced apart sourc and drain regions in said first layer extending down to the upper surface of said first and second oxide regions, respectively to define a channel in said first layer.

37. The structure of claim 36 further including a dielectric above said channel and a gate electrode on said dielectric to form a field effect transistor.

38. The structure of claim 37 further including ohmic contacts to said source and drain extending to the upper surface of said first and second oxide regions.

39. The structure of claim 37 wherein said channel is under strain.

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40. The structure of claim 37 wherein said second layer has a graded composition of Ge to lattice strain to said channel in said first layer.

41. The structure of claim 37 wherein said first layer is relaxed.

42. The structure of claim 37 wherein said first layer is commensurate with said first layer.

43. The structure of claim 37 further including a plurality of said field effect transistors of n and p type respectively.

44. The structure of claim 43 further including interconnection wiring to form complementary metal oxide semiconductor (CMOS) circuits.

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