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Specification



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1. Title of the Invention:

Signal output device, driver circuit, and system and method for sending signals

2. Detailed Description of the Invention:

Field of the invention

The present invention relates to a system and a method that can set a plurality of different data transfer rates just like a signal sending system and a signal sending method conforming to, for example, the ATA (AT Attachment) interface and enables a signal to be sent from a signal output device to a signal receiving device via a signal sending line at a predetermined data transfer rate.

Background art

A signal sending system that can set a plurality of different data transfer rates and enables a signal to be sent from a signal output device to a signal receiving device via a signal sending line at a predetermined data transfer rate is employed, for example, as a signal sending system among such peripheral devices as a host system, a hard disk drive (HDD), and a CD-ROM drive in a computer system.

There are the ATA interface, the SCSI (Small Computer System Interface), etc. for the interface standards used between a signal output device and a signal receiving device (between a host system and peripheral devices) in a signal sending system as described above. Of those standard interfaces, the ATA interface, which provides a variety of interfaces from the legacy ATA interface to the Ultra ATA/66 interface, includes a

plurality of different interface standards to cope with various data transfer procedures (signal sending procedures) and various maximum data transfer rates. There are also two types of sending cables (flat cables) used for the connection between those output and receiving devices. Figure 2 lists up those ATA interfaces.

In Figure 2, the legacy ATA interface supports all the data transfer rates (modes 0 to 4) in the PIO data transfer mode and all the data transfer rates (modes 0 to 2) in the multi-word DMA data transfer mode. The Ultra ATA/33 interface supports data transfer rates up to 33.3[MB/s](mode 2) of the Ultra DMA data transfer mode while it enables the legacy ATA interface to keep its compatibility with higher-ranking interfaces. The Ultra ATA/66 interface supports data transfer rates up to 66.6[MB/s](mode 4) of the Ultra DMA data transfer mode while it enables the Ultra ATA/33 interface to keep its compatibility with higher-ranking interfaces. Consequently, for example, a signal sending system conforming to the Ultra ATA/66 interface must be able to send signals at 9 types of data transfer rates from 3.3[MB/s] to 66.6[MB/s].

The above mentioned ATA interface sends 16-bit parallel data with use of 16 data buses. A signal sending system conforming to the ATA interface uses a flat cable (described as a 40C cable) comprising 40 signal lines (data signal lines, control signal lines, and ground lines) or a flat cable (described as a 80C cable) comprising 80 signal lines. The 40C cable includes 16 data signal lines disposed in parallel therein. And, because the potentials of those 16 data signal lines are changed simultaneously due to a simultaneous switching by the driver circuit of the signal output device, a cross talk noise is apt to be generated at a high data transfer rate. To avoid such a trouble, therefore, a ground line is inserted between signal lines in the 80C cable, thereby suppressing the generation of such a cross talk noise.

The accuracy of data signal/strobe signal sending between a

host system and such a peripheral device as an HDD is generally referred to as signal integrity. The strobe signal is assumed to be a timing reference for latching the data signal. If there is a possibility that a latching timing is disturbed and/or a data signal level is changed by a generated noise, thereby a data transfer error occurs (a data value output from a signal output device differs from a data value received by a signal receiving device), then the signal integrity is degraded. And, if there is not such a possibility, the signal integrity becomes high.

A signal I/O device is provided for each of the host system and the peripheral devices described below. Those signal I/O devices are used to exchange data between the host system and each of the peripheral devices. A signal I/O device provided at the data transfer side is used as a signal output device and a signal I/O device provided at the data receiving side is used as a signal receiving device. Such a signal output device is provided with drive circuits used to output signals to signal lines. A drive circuit is provided for each signal line for outputting a signal. The drive circuit can output a signal with electrical properties (predetermined peculiar properties) common to all the possible data transfer rates and all the usable cable types (40C and 80C cables).

Problems to be Solved by the Invention

The data transfer rate employed between a host system and such a peripheral device as an HDD or the like is demanded to become higher and higher in recent years. To meet such a requirement, a new standard is prepared for the ATA interface so that data transfer is enabled at 100[MB/s] or over in the Ultra DMA mode. While the maximum data transfer rate is getting higher and higher, the minimum data transfer rate remains the same, since the legacy ATA interface must be kept at its compatibility with higher-ranking interfaces. This is why the range of the data transfer rate that must be supported becomes wider as the

maximum data transfer rate becomes higher.

However, the above mentioned conventional signal output device is composed so that its drive circuit that operates with predetermined peculiar electrical properties is used to output a signal at every possible data transfer rate, it cannot meet the requirement of a higher signal integrity with respect to all the possible data transfer rates, which will be wider and wider in the future.

If a new cable that can further reduce the cross talk noise is developed, then cable types that must be supported will also be increased so as to enable the 40C and 80C cables to keep their compatibility with higher-ranking interfaces.

However, there has been a limit to the conventional drive circuit; the drive circuit cannot obtain a high signal integrity on all the signal sending conditions comprising all the possible data transfer rates and all the usable cable types.

Under such circumstances, it is an object of the present invention to provide a signal output device and a signal sending method for realizing a high signal integrity at every possible data transfer rate. It is another object of the present invention to provide a signal output device and a signal sending method for realizing a high signal integrity on all the signal sending conditions comprising all the possible data transfer rates and all the usable cable types.

Summary of the Invention

According to one aspect of the present invention there is provided a signal output device, comprising:

a driver circuit for setting a plurality of different slew rates and relaying a signal to a signal sending line at a selected slew rate among said plurality of different slew rates;

a controller for selecting said selected slew rate of said driver circuit according to a predetermined data transfer rate, said controller being configured to set said selected slew rate of said driver circuit according to said predetermined data transfer rate and a type of said signal sending line, wherein said controller includes a memory system for storing a table containing a slew rate for each predetermined data transfer rate, said slew rate of said driver circuit being set with reference to said table.

According to another aspect of the present invention there is provided a signal output device, comprising:

a driver circuit for setting a plurality of different slew rates and relaying a signal to a signal sending line at a selected slew rate among said plurality of different slew rates; and

a controller for selecting said selected slew rate of said driver circuit according to a predetermined data transfer rate, said driver circuit being configured to adjust a first slew rate at the start of its output signal separately from a second slew rate at the end of said output signal, wherein said controller includes a memory system for storing a table containing a slew rate for each predetermined data transfer rate, said slew rate of said driver circuit being set with reference to said table.

According to another aspect of the present invention there is provided a signal sending system, enabling a signal to be sent to a host system via a signal sending line, comprising:

a signal output device that can set a plurality of different data transfer rates and send a signal to an object device via a signal sending line at a selected data transfer rate, said signal output device including:

a driver circuit for setting a plurality of different slew rates and relaying a signal to a signal sending line at a predetermined slew rate; and

a controller for setting a slew rate of said driver circuit according to a predetermined data transfer rate from a signal output device provided for a host system, a type of said signal sending line, and a quantity of peripheral devices connected to said signal sending line.

Preferred embodiment

Embodiment 1

Figure 1 is a block diagram of a computer system to which Embodiment 1 of the present invention applies. The computer system in Figure 1 comprises a host system 1, an ATA (AT Attachment) flat cable (IDE: Integrated Device(Drive) Electronics) flat cable) 2, such peripheral devices 3 as a hard disk drive (HDD) 3a, a CD-ROM drive 3b, a DVD (Digital Video Disc) drive, etc., a display 4, and such data input devices 5 as a keyboard 5a, a mouse 5b, etc.

The host system 1 controls the whole computer system shown in Figure 1. The host system 1 is provided with a mother board 10 on which a chip set including a CPU (Central Processing Unit) chip 11 is mounted.

On the mother board 10 are mounted a CPU chip 11, a bus controller chip 12, a main memory 13, an AT controller chip (ISA (Industry Standard Architecture) controller chip) 14, an I/O controller chip 15, a system BIOS chip (ROM) 16, a graphic accelerator (chip or card) 17, such PCI (Peripheral Component Interconnect) expansion cards as a SCSI (Small Computer System Interface) card 18, an IDE card 19, etc.

On the mother board 10 are further provided a host bus 21, a PCI bus 22, an ISA bus (AT bus) 23, PCI slots 24, ISA slots (AT slots) 25, an ATA port (IDE port) 26, USB (Universal Serial Bus) ports 27, and I/O ports 28.

The host bus 21 is provided between the CPU 11 and a bus controller 12. The bus 21 includes, for example, a 32-bit parallel data bus and a 40-bit parallel control bus.

The PCI bus 22 is provided so as to connect the bus controller 12, the AT controller 14, and the PCI slots 25 to each another. The PCI bus 22 includes a 32-bit parallel bus to be used

commonly by both data and control signals. Such PCI expansion cards as a SCSI card 18, an IDE card 19, etc. are inserted in the PCI slots 22. Such peripheral devices as an HDD 6a, a CD-ROM drive, a DVD drive 6b, etc. that are conforming to the SCSI interface standard can be connected to the SCSI card 18. Such peripheral devices as an HDD, a CD-ROM drive, a DVD drive 8, etc. that are conforming to the ATA interface standard can be connected to the IDE card 19 via an IDE cable (ATA cable) 7 respectively.

The ISA bus 23 is provided so as to enable the AT controller 14, the I/O controller 15, the system BIOS chip 16, and the ISA slots 25 to be connected to each another. The ISA bus 23 includes a 16-bit parallel data bus and a 24-bit parallel control bus. This ISA bus 23 conforms to the ATA interface standard. The system BIOS chip 16 records system BIOS for controlling the initial operation of the computer system when the system is powered. An ISA expansion card can be inserted in an ISA slot 25. The I/O controller 15 controls data transfer between the ISA bus 23 and each I/O port 28. Such data input devices as the keyboard 5a, a mouse, etc., and a printer are connected to the I/O ports 28 (the keyboard 5a is connected to an I/O port 28 in Figure 1).

The bus controller 12 is connected to the main memory 13, the PCI bus 22, and the graphic accelerator 17. The bus controller 12 is also connected to the CPU 11 via the host bus 21 so as to control data transfer between the CPU 11 and the main memory 13 or the PCI bus 22 or the graphic accelerator 17, as well as between the main memory 13 and the PCI bus 22 or the graphic accelerator 17, and between the PCI bus 22 and the graphic accelerator 17. The display 4 is connected to the graphic accelerator 17.

The AT controller 14 is connected to the main memory 13, the PCI bus 22, the ISA bus 23, the ATA ports 26, and the USB ports 27. The AT controller 14 controls data transfer between the main memory 13 and the ATA port 26 or the USB ports 27 or the

ISA bus 23, as well as between the PCI bus 22 and the ATA port 26 or the USB ports 27 or the ISA bus 23. Such peripheral devices 3 as an HDD 3a, a CD-ROM drive 3b, a DVD drive, etc. are connected to the ATA port 26 via an ATA cable 2 respectively. (In Figure 1, the HDD 3a and the CD-ROM drive 3b are connected to one ATA cable 2.) Such data input devices as a mouse 5b, a keyboard, etc. are connected to the USB ports 27. (In Figure 1, the mouse 5b is connected to a USB port 27.)

Signal Sending System Conforming to the ATA Interface

An ATA flat cable 2 conforming to the ATA interface is connected to the ATA port 26. And, such peripheral devices 3 as the HDD 3a, the CD-ROM drive 3b, the DVD drive, etc. that are conforming to the ATA interface are connected to the ATA port via this ATA cable 2. Up to two peripheral devices can be connected to one ATA port 26 via one ATA cable 2. The host system 1 and the peripheral devices 3 (the HDD 3a and the CD-ROM drive 3b) are provided with a signal I/O device conforming to the ATA interface respectively. The signal I/O device of the host system 1, the ATA cable 2, and the signal I/O device of the HDD 3a are combined to compose a signal sending system conforming to the ATA interface. In the same way, the signal I/O device of the host system 1, the ATA cable 2, and the signal I/O device of the CD-ROM drive 3b are combined to compose a signal sending system conforming to the ATA interface.

A signal sending system conforming to the ATA interface enables bi-directional signal sending. For example, when data is sent from the HDD 3a to the host system 1, the signal I/O device of the HDD 3a is assumed to be a signal output device for outputting a signal to the ATA cable 2 and the signal I/O device of the host system 1 is assumed to be a signal receiving device for receiving a signal from the ATA cable 2.

The above ATA interface sends 16-bit parallel data with use of 16 data buses. The ATA cable 2 conforming to the ATA interface

is divided into 40-core flat cable (16 data signal lines, control signal lines, and ground lines) (hereafter, to be described as a 40C cable) and 80-core flat cable (hereafter, to be described as a 80C cable). The 80C cable is obtained by adding 40 ground lines to a 40C cable. In the 80C cable, a ground line is provided between signal lines, thereby reducing the cross talk noise during high speed data transfer.

ATA Interface Standard

Figure 2 shows the ATA interface standard. In Figure 2, (a) shows data transfer rates in ATA interface standard data transfer modes, as well as a data transfer rate in each data transfer mode and (b) shows data transfer modes supported by each ATA interface, the maximum data transfer rate and the minimum data transfer rate supported by each ATA interface, and cable types used by each ATA interface.

As shown in Figure 2, there are PIO (Program Input/Output) data transfer and multi-word DMA (Direct Memory Access) data transfer, and Ultra DMA data transfer modes for the ATA interface data transfer mode. The PIO data transfer is a method that the CPU 11 of the host system 1 accesses the ATA port 26 directly, thereby sending data. The data sent from the ATA port 26 is received by the main memory 13, etc. via the CPU 11. The DMA data transfer (multi-word DMA data transfer and Ultra DMA data transfer) is a method that data is sent directly between the main memory 13 and such a peripheral device 3 as the HDD 3a without using the CPU 11. The load of the CPU 11 can thus be reduced more than in the PIO data transfer method.

The ATA interface sends data signals with use of the data signal lines of the ATA cable 2 and a strobe signal with use of the strobe signal line of the ATA cable 2. The strobe signal is assumed to be a timing reference for latching the data signal in the signal receiving device.

The multi-word DMA data transfer method latches a data signal

at the start of the strobe signal. The Ultra DMA data transfer method latches a data signal at both rising edge and falling edge of the strobe signal, thereby realizing a data transfer rate double that of the multi-word DMA data transfer method.

As shown in Figure 2(a), the data transfer rates in the above PIO data transfer mode are:

Mode 0 = 3.3[MB/s],
Mode 1 = 5.2[MB/s],
Mode 2 = 8.3[MB/s],
Mode 3 = 11.1[MB/s], and
Mode 4 = 16.6[MB/s].

The data transfer rates in the above multi-word DMA data transfer mode are:

Mode 0 = 8.3[MB/s],
Mode 1 = 11.1[MB/s], and
Mode 2 = 16.6[MB/s].

The data transfer rates in the above Ultra DMA data transfer mode are:

Mode 0 = 16.6[MB/s],
Mode 1 = 22.2[MB/s],
Mode 2 = 33.3[MB/s],
Mode 3 = 44.4[MB/s],
Mode 4 = 66.6[MB/s], and
Mode 5 = 100[MB/s].

The Ultra DMA data transfer mode 5 is a data transfer rate whose standardization is being prepared now so as to meet the requirement of a higher data transfer rate.

As shown in Figure 2(b), the ATA interface standard includes the legacy ATA interface, as well as the Ultra ATA/33 interface, the Ultra ATA/66 interface, the Ultra ATA/100

interface, etc. The Ultra ATA/100 interface is being prepared now for standardization so as to meet the requirement of a higher data transfer rate.

The legacy ATA interface supports every mode (modes 0 to 4) of the PIO data transfer method and every mode (modes 0 to 2) of the multi-word DMA data transfer method. The Ultra ATA/33 interface supports data transfer rates of 16.6[MB/s] (mode 0), 22.2[MB/s] (mode 1), 33.3[MB/s] (mode 2) in the Ultra DMA data transfer mode while enabling the legacy ATA interface to keep its compatibility with higher-ranking interfaces. The Ultra ATA/66 interface supports the data transfer rates of 44.4[MB/s] (mode 3) and 66.6[MB/s] (mode 4) in the Ultra DMA data transfer mode while enabling the legacy ATA interface and the Ultra ATA/33 interface to keep its compatibility with higher-ranking interfaces. In addition, the Ultra ATA/100 interface supports the data transfer rate of 100[MB/s] (mode 5) in the Ultra DMA data transfer mode while enabling the Ultra ATA/66 interface to keep its compatibility with higher-ranking interfaces.

Consequently, for example, a signal sending system conforming to the Ultra ATA/66 interface must be able to send a signal at 9 data transfer rates from 3.3 to 66.6[MB/s]. And, a signal sending system conforming to the Ultra ATA/100 interface must be able to send a signal at 10 data transfer rates from 3.3 to 100[MB/s].

Although a 40C or 80C cable can be used for data transfer rates within 33.3[MB/s], a 80C cable must be used for data transfer rates at 44.4[MB/s] or over. Consequently, the legacy ATA interface and the Ultra ATA/33 interface, even when a 40C cable is used, can set the maximum data transfer rate (data transfer at the maximum data transfer rate), but the Ultra ATA/66 interface and the Ultra ATA/100 interface can set their maximum data transfer rates of 66.6 or 100[MB/s] only when a 80C cable is used. If a 40C cable is used, the data transfer rate is set to 33.3[MB/s] or under.

The ATAPI (AT Attachment Packet Interface) is also another ATA interface. For the ATAPI, only the command sending protocol is changed from that of the ATA interface. The data transfer modes, the data transfer rates, and the cable types are common between the ATA interface and the ATAPI interface. Either the ATA interface or the ATAPI interface is selected according to the type of the object peripheral device. For example, the ATA interface is used for data transfer between the host system and an HDD and the ATAPI interface is used for data transfer between the host system and a CD-ROM drive.

Configuration of Signal Sending System Conforming to ATA Interface

Figure 3 is a block diagram of a signal sending system conforming to the ATA interface. The system comprises a signal I/O device of the host system 1, an ATA cable 2, and a signal I/O device of a peripheral device 3 (HDD 3a or CD-ROM drive 3b).

Peripheral Devices, HDD, and Their Signal I/O Devices

In Figure 3, the HDD 3a conforms to the ATA interface. The HDD 3a is provided with an ATA interface controller 31 having a driver/receiver unit (DRU) 31a connected to the ATA cable 2, an MPU (Micro Processing Unit) 32 for controlling the whole HDD, a memory 33, a hard disk (magnetic disk), and an accessing mechanism for accessing the hard disk, and an HDC (Hard Disk Controller) 34 for controlling the accessing mechanism. This HDD 3a records data received from the host system 1 on a hard disk and regenerates data from the hard disk and sends the regenerated data to the host system 1. The ATA interface controller 31, the MPU 32, the memory 33, and the HDC 34 are mounted on a card (printed board) 30.

The HDD 3a is provided with a signal I/O device for controlling signal exchanges with the host system 1 via the ATA interface, outputting a signal to the ATA cable 2, and receiving a signal

from the ATA cable 2. The signal I/O device of the HDD 3a includes an ATA interface controller 31, an MPU (Micro Processing Unit) 32, and a memory 33. The ATA interface controller 31 includes a driver/receiver unit 31a connected to the ATA cable 2.

Peripheral Devices, CD-ROM Drive and Their Signal I/O Devices

The CD-ROM drive 3b conforms to the ATA interface and it is provided with an ATAPI controller 41 having a driver/receiver unit 41a connected to the ATA cable 2, an MPU 42 for controlling the whole CD-ROM drive, a memory 43, an accessing mechanism for accessing the loaded CD-ROM, and a CDC (Compact Disk Controller) 44 for controlling the accessing mechanism. This CD-ROM drive 3b regenerates data recorded on the CD-ROM and sends the regenerated data to the host system 1. The ATAPI controller 41, the MPU 42, the memory 43, and the CDC 44 are mounted on a card (printed board) 40. The CD-ROM drive may be of a type that can record data received from the host system 1 on a CD-ROM.

The CD-ROM drive 3b is provided with a signal I/O device for controlling signal exchanges with the host system 1 via the ATA interface, outputting a signal to the ATA cable 2, and receiving a signal from the ATA cable 2. The signal I/O device of the CD-ROM drive 3b includes an ATAPI controller 41, an MPU 42, and a memory 43.

Signal I/O Device of Host System

The host system 1 is provided with a signal I/O device for controlling signal exchanges with a peripheral device 3 (HDD 3a or CD-ROM drive 3b) via the ATA interface, outputting a signal to the ATA cable 2, and receiving a signal from the ATA cable 2. The signal I/O device of the host system 1 includes an AT controller 14 having a driver/receiver unit 14a connected to the ATA cable 2, a CPU 11 (see Figure 1), and a main memory 13 (see Figure 1).

Structure of ATA Cable

At one end of the ATA cable 2 is provided a connector 2a for connecting the ATA port 26 of the host system 1 and at a middle portion and at the other end of the ATA cable 2 are provided connectors 2b and 2c for connecting the IDE ports provided on the cards of the peripheral devices 3 respectively. In Figure 3, the connector 2b is connected to the IDE port 35 provided on the card 30 of the HDD 3a and the connector 2c is connected to the IDE port 45 provided on the card 40 of the CD-ROM drive 3b.

The signal lines of the ATA cable are connected to the driver/receiver unit 14a of the AT controller 14 via the connector 2a and the ATA port 26, as well as to the driver/receiver unit 35a of the ATA interface controller 31 via the connector 2b and the IDE port 35 and further to the driver/receiver unit 45a of the ATAPI controller 41 via the connector 2c and the IDE port 45.

In the 40C cable are disposed 16 signal lines and 24 control signal lines (including 3 strobe signal lines and one ground line) side by side.

In the 80C cable are disposed 16 signal lines and 64 control signal lines (including 3 strobe signal lines and 41 ground lines) side by side.

The 80C cable is obtained by adding 40 ground lines to the 40C cable so that a ground line is disposed between signal lines, thereby reducing the cross talk noise in high speed data transfer. In the connection connectors 2a, 2b, and 2c, the added 40 ground lines are connected to the ground line provided in the 40C cable from the beginning. Consequently, the connection connectors 2a, 2b, and 2c for both 40C and 80C cables are provided with 40 pins respectively. Any of the 40C and 80C cables can thus be connected to the ATA port 26, the IDE ports 35 and 45.

Driver/Receiver Unit

Figure 4 is a circuit diagram of the driver/receiver unit 51a (31a or 41a) of a peripheral device 3 (HDD 3a or CD-ROM drive 3b). As shown in Figure 4, the driver/receiver unit 51a provided in the interface controller 51 (ATA interface controller 31 or ATAPI controller 41) of the peripheral device 3 is composed so that any of a driver/receiver circuit 52, a driver circuit 53, and a receiver circuit 54 is provided between the signal lines of the ATA cable 2 (except between ground lines) and the signal lines of the interface controller 51 corresponding to the signal lines of the ATA cable 2 respectively. The driver circuit 53 outputs a signal to the ATA cable 2. The signal is a signal sent to the signal I/O device of the host system 1 from the peripheral device 3. The receiver circuit 54 receives the signal output to the ATA cable 2 from the signal I/O device of the host system 1.

The driver/receiver circuit 52 is provided with a driver circuit 53 and a receiver circuit 54 and receives a signal from the ATA cable 2 via the receiver circuit 54 and outputs a signal to the ATA cable 2 via the driver circuit 53. The signal received from the ATA cable 2 is a signal output from the signal output device of the host system 1 and the signal output to the ATA cable 2 is a signal sent from the peripheral device 3 to the host system 1. The driver/receiver circuit 52, when the peripheral device 3 sends data to the host system 1, is controlled by the interface controller 51 so that only the driver circuit 53 is activated (the circuit 52 can thus be regarded to be provided only with the driver circuit 53 at this time). When the host system 1 sends data to the peripheral device 3, the driver/receiver circuit 52 is controlled by the interface controller 51 so that only the receiver circuit 54 is activated (the circuit 52 can thus be regarded to be provided only with the driver circuit at this time).

The 16 data signal lines DD of the ATA cable 2 are bi-directional signal lines used to send data signals to the

peripheral device 3 from the host system 1, as well as to send signals to the host system 1 from the peripheral device 3. On the contrary, the strobe signal line DST1 (referred to as "IORDY") is a one-way signal line used to send a strobe signal from the peripheral device 3 to the host system 1 in the Ultra DMA data transfer mode. The strobe signal line DST2 (referred to as "DIOW-") is a one-way signal line used to send a strobe signal from the host system 1 to the peripheral device 3 in the PIO data transfer mode and in the multi-DMA data transfer mode. The strobe signal line DST3 (referred to as "DIOR-") is a one-way signal line used to send a strobe signal from the peripheral device 3 to the host system 1 in the PIO data transfer mode and in the multi-DMA data transfer mode and send a signal from the host system 1 to the peripheral device 3 in the Ultra DMA data transfer mode.

In the driver/receiver unit 51a, a driver/receiver circuit 52 is provided for the bi-directional signal sending line of the ATA cable 2 and only the driver circuit 53 or receiver circuit 52 is provided for the one-way signal sending line of the ATA cable 2.

The input terminals of the driver circuit 53 are connected to signal wiring (data signal lines dd, strobe signal lines dst1, dst3, etc.) corresponding to the interface controller 51. The output terminals of the driver circuit 53 are connected to the signal lines (data signal lines DD, strobe signal lines DST2, DST3, etc.) corresponding to the ATA cable 2 via the IDE ports 35 and 45, as well as the peripheral device connection connectors 2b and 2c. The input terminals of the receiver circuit 54 are connected to the signal lines (data signal lines DD, strobe signal lines DST2, DST3, etc.) corresponding to the ATA cable 2 via the IDE ports 35 and 45, as well as the peripheral device connection connectors 2b and 2c. The output terminals of the receiver circuit 54 are connected to the signal wiring (data signal lines DD, strobe signal lines DST2, DST3, etc.) corresponding to the interface controller 51. The ground line DG of the ATA cable 2 is connected to the ground

pattern GND of the card (card 30 or 40 shown in Figure 3) of the peripheral device 3 via the interface controller 51.

The driver/receiver unit 14a of the host system 1 in the circuit diagram is almost the same as the driver/receiver unit 51a shown in Figure 4. In the unit 14a, however, the disposition of the driver circuit 53 and the receiver circuit 54 is changed from that of the driver/receiver unit 51a of the peripheral device 3 with respect to each one-way signal sending line of the ATA cable 2. For example, the receiver circuit 54 is provided for the strobe signal line DST1 and the driver circuit 53 is provided for the strobe signal line DST2.

Signal Output Device and Its Driver Circuit in Embodiment 1

In a signal sending system conforming to the ATA interface as shown in Figure 3, the higher the data transfer rate is and the larger the driver circuit slew rate is, the more the number of switching times per output signal time is increased and the sharper the potential change with respect to the output signal time becomes. (The slew rate is a potential change rate with respect to an output signal time when the subject driver circuit changes the potential of an output signal according to the potential change of an input signal. The unit of the change rate is [V/ns] or the like.) Consequently, the cross talk noise in the ATA cable 2 is increased, thereby the signal integrity is degraded. If a low data transfer rate is set, for example, to 3.3[MB/s], then a driver circuit of a small slew rate is provided so that the potential of the output signal is changed gently. With this, the cross talk noise is reduced, thereby the signal integrity is improved. If such a high data transfer rate as 66.6[MB/s] or 100[MB/s] is set, however, changes of the output signal cannot follow up with changes of the input signal in the driver circuit of a small slew rate as described above. Thus, the output signal cannot keep the "low" level period or "high" level period enough, thereby the signal integrity is degraded.

This is why the conventional signal output device is provided with a driver circuit of a large slew rate so as to cope with the maximum data transfer rate, since the driver circuit having a fixed slew rate is used commonly for all the possible data transfer rates. The Ultra ATA/66 interface and the Ultra ATA/100 interface that is now being prepared must use the 80C cable so as to reduce the cross talk noise.

In this case, however, it is unknown what kind of a host system will communicate with a signal sending system in which such peripheral devices as an HDD, etc. are employed. If an HDD provided with a driver circuit designed so as to use the 80C cable and set the 100[MB/s] data transfer rate is connected to a host system via a 40C cable, then a large cross talk noise will be generated, thereby the signal integrity is degraded to a serious level, since the slew rate of the driver circuit is large.

The signal output device in Embodiment 1 is provided with a driver circuit 53 that can set a plurality of different slew rates and can output a signal at a predetermined slew rate, as well as a controller that can set a slew rate of the driver circuit 53 according to the signal sending condition comprising the predetermined data transfer rate and the type of a cable in use so that the device can set the best slew rate according to the signal sending condition.

In the HDD 3a, the ATA interface controller 31 and the MPU 32 are combined to compose the above controller. In the CD-ROM drive 3b, the ATAPI controller 41 and the MPU 42 are combined to compose the controller. In the host system 1, the AT controller 14 and the CPU 11 are combined to compose the controller. As shown in Figure 4, the slew rate of the driver circuit 53 in Embodiment 1 is set to the best value according to the signal sending condition in response to the control signal SRC entered from the controller.

The driver circuit 53 in Embodiment 1 is mounted on one IC chip

together with part of the controller (the ATA interface controller 31, the ATAPI controller 41, or the AT controller 14). However, the driver circuit 53 may be mounted on one IC chip together with the whole controller.

Configuration of the Driver Circuit in Embodiment 1

Figure 5 is a circuit diagram of a driver circuit 53 in the signal output device in Embodiment 1 according to the present invention. In Figure 5, the driver circuit 53 is provided with pMOS transistors (p1, p2, and p3), nMOS transistors (n1, n2, and n3), delay circuits (DL1 and DL2), switching circuits (SW1 and SW2), and an inverter (IV).

The driver circuit 53 shown in Figure 5 can set a plurality of different slew rates if it is configured so as to be able to adjust the switching timings of the three CMOS inverters comprising transistors p1 to p3 and n1 to n3. The delay circuits DL1 and DL2, as well as the switching circuits SW1 and SW2 are combined to compose a device for setting a slew rate if the switching timings of the three CMOS inverters are delayed by a time respectively corresponding to the values of the bits b1 and b2 of the slew rate control signal SRC.

The inverter IV inverts the transmit signal SIN entered to the signal input terminal "in" from the interface controller 51, thereby supplying the inverted transmit signal rSIN to the gate electrodes of the transistors p1 and n1, the input terminal of the delay circuit DL1, and the terminals A of the switching circuits SW1 and SW2 respectively.

The delay circuit DL1 delays the entered transmit signal rSIN and supplies the delayed signal to the terminal B of the switching circuit SW1. The delay circuit DL2 delays a signal supplied from the terminal C of the switching circuit SW1 and supplies the delayed signal to the terminal B of the switching circuit SW2. In this case, it is premised that the signal delay time delayed by each of the delay circuits DL1 and DL2 is

The slew rate control signal SRC entered to the terminal src from the interface controller is used to set a slew rate of the driver circuit and it is a 2-bit signal comprising bits b1 and b2. The bit b1 is entered to the switching circuit SW1 and the bit b2 is entered to the switching circuit SW2.

The switching circuit SW1 connects the terminal C to either the terminal A or B according to the logical value of the bit b1 of the slew rate control signal SRC. In this case, the switching circuit SW1 connects the terminal C to the terminal A at b1 = "0," thereby the transmit signal rSIN is supplied to the gate electrodes of the transistors p2 and n2, as well as to the input terminal of the delay circuit DL2. At b1 = "1," the switching circuit SW1 connects the terminal C to the terminal B, thereby the transmit signal rSIN is delayed by a time T and the delayed signal is supplied to the gate electrodes of the transistors p2 and n2, as well as to the input terminal of the delay circuit DL2.

The switching circuit SW2 connects the terminal C to the terminal A or B according to the value of the bit b2 of the slew rate control signal SRC. The signal supplied to the terminal B of the switching circuit SW2 is varied according to the setting of the switching circuit SW1. The signal is delayed by a time T or (2xT) from the transmit signal rSIN. In this case, the switching circuit SW2 connects the terminal C to the terminal A at b2 = "0," thereby the transmit signal rSIN is supplied to the gate electrodes of the transistors p3 and n3. At b2 = "1," the switching circuit SW2 connects the terminal C to the terminal B, thereby the signal is delayed by a time T or (2xT) from the transmit signal rSIN and the delayed signal is supplied to the gate electrodes of the transistors p3 and n3.

The source electrodes of the transistors p1 to p3 are connected to the power supply VDD and the drain electrodes of those transistors are connected to the output terminal "out." The

source electrodes of the transistors n1 to n3 are connected to the ground GND and the drain electrodes of those transistors are connected to the output terminal "out." The output terminal "out" is connected to the AT cable 2 (see Figures 3 and 4) and the transmit signal SOUT output from the driver circuit 53 at a predetermined slew rate is supplied to the AT cable 2.

The current driving performance (for example, a mutual conductance is an index of the current driving performance) should preferably be identical in both transistors p1 and n1, in both transistors p2 and n2, and in both transistors p3 and n3 respectively. In addition, the threshold should be the same in both transistors p1 to p3, as well as in both n1 to n3. In this case, it is premised that the current driving performance is the same among the transistors p1 to p3, as well as among the transistors n1 to n3.

The CMOS inverter composed of transistors p1 and n1 is always switched according to a level change of the transmit signal rSIN. The CMOS inverter composed of transistors p2 and n2, when the switching circuit SW1 is set to the terminal A, is switched at the same timing as that of the transistors p1 and n1 according to a level change of the transmit signal rSIN. When the switching circuit SW1 is set to the terminal B, however, the CMOS inverter is switched at a timing delayed by a time T from the switching timing of the transistors p1 and n1 according to a level change of a signal delayed by a time T from the inverted transmit signal SIN. The CMOS inverter composed of transistors p3 and n3 is switched at any one of the same timing as that of the transistors p1 and n1, a timing delayed by a time T from that of the transistors p1 and n1, and a timing delayed by a time (2xT) from that of the transistors p1 and n1 according to setting of the switching circuits SW1 and SW2.

Operation of the Driver Circuit in Embodiment 1

Figure 6 shows the operation of the driver circuit 53 and the correspondence among the settings of the switching circuits SW1 and SW2, the slew rate values, and output signal waveforms of the driver circuit 53. The output signal waveforms shown in Figure 6 are explanatory ones for describing changes of slew rates.

As shown in Figure 6, a slew rate can be set in three steps of $sr1$ (maximum), $sr2$ ($<sr1$), and $sr3$ ($<sr2$) according to the slew rate control signal SRC in the driver circuit 53. The transmit signal SOUT has an adjusted slew rate, which is supplied to the AT cable from the driver circuit 53. The signal SOUT and the signal SIN entered to the driver circuit 53 are identical in phase.

If $b1 = b2 = "0"$ is set in the slew rate control signal SRC and both switching circuits SW1 and SW2 are set to the terminal A, then the inverted transmit signal rSIN is supplied to the gate electrodes of the transistors p1 to p3, as well as n1 to n3.

If the level of the transmit signal SIN is changed from Low (hereafter, to be described as "L") to High (hereafter, to be described as "H"), the transistors p1 to p3 are turned on simultaneously and the transistors n1 to n3 are turned off simultaneously at a timing t_r when the voltage of the inverted transmit signal rSIN falls to the threshold. With the switching operations of those transistors, the level of the transmit signal SOUT is changed from "L" to "H."

If the level of the transmit signal SIN is changed from "H" to "L," the transistors p1 to p3 are turned off simultaneously and the transistors n1 to n3 are turned on simultaneously at a timing t_f when the voltage of the inverted transmit signal rSIN rises to the threshold. With the switching operations of those transistors, the level of the transmit signal SOUT is changed from "H" to "L."

Consequently, if $b1 = b2 = "0"$ is set for the slew rate control signal SRC, the driver circuit 53 drives the AT cable with the maximum current driving performance of the driver circuit 53 obtained by the transistors $p1$ to $p3$ between the timing tr and the following timing tf and drives the AT cable 2 with the maximum current driving performance of the driver circuit 53 obtained by the transistors $p1$ to $p3$ between the timing tf and the following timing tr .

Consequently, the slew rate of the driver circuit 53 takes the maximum value srl . The transmit signal SIN thus begins rising from the "L" level at the timing tr , then keeps rising at a slew rate of srl to reach the "H" level. The transmit signal SIN begins falling from the "H" level at the timing tf , then keeps falling at a slew rate of srl to reach the "L" level.

If $b1 = "0"$ and $b2 = "1"$ are set for the slew rate control signal SRC and the switching circuit SW1 is set to the terminal A and the switching circuit SW2 is set to the terminal B, then the inverted transmit signal $rSIN$ is supplied to the gate electrodes of the transistors $p1$, $p2$, $n1$, and $n2$ and a signal delayed by a time T from the inverted transmit signal $rSIN$ is supplied to the gate electrodes of the transistors $p3$ and $n3$ respectively.

If the level of the transmit signal SIN is changed from "L" to "H," the transistors $p1$ and $p2$ are turned off and the transistors $n1$ and $n2$ are turned on at the timing tr . And, the transistor $p3$ is turned on and the transistor $n3$ is turned off at the following timing $(tr+T)$. With the switching operations of those transistors, the level of the transmit signal SOUT is changed from "L" to "H."

If the level of the transmit signal SIN is changed from "H" to "L," the transistors $p1$ and $p2$ are turned off and the transistors $n1$ and $n2$ are turned on at the timing tr and the transistor $p3$ is turned off and the transistor $n3$ is turned on at the following timing $(tr+T)$ respectively. With the

switching operations of those transistors, the level of the transmit signal SOUT is changed from "H" to "L."

Consequently, if $b1 = "0"$ and $b2 = "1"$ are set for the slew rate control signal SRC, the driver circuit 53 drives the AT cable 2 according to the state of the transistors $p1$ and $p2$ between the timing tr and the timing $(tr+T)$ and drives the AT cable 2 with its maximum current driving performance obtained by the transistors $p1$ to $p3$ between the timing $(tr+T)$ and the following timing tf . In addition, the driver circuit 53 drives the AT cable 2 according to the state of the transistors $n1$ and $n2$ between the timing tf and the timing $(tf+T)$ and drives the AT cable 2 with its maximum current driving performance obtained by the transistors $n1$ to $n3$ between the timing $(tf+T)$ and the following timing tr .

Because the current driving performance is adjusted during a level change of the transmit signal SIN by delaying the switching timing of the transistors $p3$ and $n3$ by a time T in this way, the slew rate of the driver circuit 53 takes a value of $sr2(<sr1)$. The transmit signal SIN thus begins rising from the "L" level at the timing tr and keeps rising at a slew rate of $sr2$ to reach the "H" level. And, the transmit signal SIN begins falling from the "H" level at the timing tf and keeps falling at a slew rate of $sr2$ to reach the "L" level.

The slew rate of the driver circuit 53 also takes a value of $sr2$ when $b1 = "1"$ and $b2 = "0"$ are set for the slew rate control signal SRC and the switching circuit SW1 is set to the terminal B and the switching circuit SW2 is set to the terminal A. This is the same as the slew rate when $b1 = "0"$ and $b2 = "1"$ are set. When $b1 = "1"$ and $b2 = "0"$ are set, the operations of the transistors $p2$ and $p3$, as well as the operations of the transistors $n2$ and $n3$ are reversed from those when $b1 = "0"$ and $b2 = "1"$ are set.

If $b1 = b2 = "1"$ is set for the slew rate control signal SRC and the switching circuits SW1 and SW2 are set to the terminal

B, the inverted transmit signal $rSIN$ is supplied to the gate electrodes of the transistors $p1$ and $n1$ and a signal delayed by a time T from the inverted transmit signal $rSIN$ is supplied to the gate electrodes of the transistors $p2$ and $n2$ and a signal delayed by a time $(2 \times T)$ from the inverted transmit signal $rSIN$ is supplied to the gate electrodes of the transistors $p3$ and $n3$.

If the level of the transmit signal SIN is changed from "L" to "H," the transistor $p1$ is turned on and the transistor $n1$ is turned off at the timing t_r and the transistor $p2$ is turned on and the transistor $n2$ is turned off at the following timing $(t_r + T)$. And, the transistor $p3$ is turned on and the transistor $n3$ is turned off further at the following timing $(t_r + 2 \times T)$. With the switching operations of those transistors, the level of the transmit signal $SOUT$ is changed from "L" to "H."

If the level of the transmit signal SIN is changed from "H" to "L," the transistor $p1$ is turned off and the transistor $n1$ is turned on at the timing t_r and the transistor $p2$ is turned off and the transistor $n2$ is turned on at the following timing $(t_r + T)$, and the transistor $p3$ is turned off and the transistor $n3$ is turned on further at the following timing $(t_r + 2 \times T)$. With the switching operations of those transistors, the level of the transmit signal $SOUT$ is changed from "H" to "L."

Consequently, if $b1 = b2 = "1"$ is set for the slew rate control signal SRC , the driver circuit 53 drives the AT cable 2 according to the state of the transistor $p1$ between the timing t_r and the timing $(t_r + T)$ and drives the AT cable 2 according to the state of the transistors $p1$ and $p2$ between the timing $(t_r + T)$ and the timing $(t_r + 2 \times T)$ and drives the AT cable 2 with its maximum current driving performance obtained by the transistors $p1$ to $p3$ between the timing $(t_r + 2 \times T)$ and the timing t_f . In addition, the driver circuit 53 drives the AT cable 2 according to the state of the transistor $n1$ between the timing t_f and the timing $(t_f + T)$ and drives the AT cable 2 according to the state of the transistors $n1$ and $n2$ between the timing

(t_f+T) and the timing ($t_f+2\times T$) and drives the AT cable 2 with its maximum current driving performance obtained by the transistors $n1$ to $n3$ between the timing ($t_f+2\times T$) and the following timing t_r .

Because the current driving performance is adjusted during a level change of the transmit signal SIN by delaying the switching timing of the transistors $p2$ and $n2$ by a time T and the switching timing of the transistors $p3$ and $n3$ by a time ($2\times T$) in this way, the slew rate of the driver circuit 53 takes a value of $sr3$ ($<sr2$). The transmit signal SIN thus begins rising from the "L" level at the timing t_r and keeps rising at a slew rate of $sr3$ to reach the "H" level. And, the transmit signal SIN begins falling from the "H" level at the timing t_f and keeps falling at a slew rate of $sr3$ to reach the "L" level.

As described above, the driver circuit 53 is composed so that it controls the switching timings of the CMOS inverter composed of the transistors $p2$ and $n2$ and the CMOS inverter composed of the transistors $p3$ and $n3$, thereby changing the slew rates only during the rising period and during the falling period of the transmit signal SOUT without changing its current driving performance during both "H" and "L" level periods thereof.

How to Create Slew Rate Setting Table for Driver Circuit

Next, how to create a slew rate setting table for the driver circuit 53 will be described. At first, the best slew rate is set beforehand for each signal sending condition comprising a data transfer rate and an ATA cable type, then a slew rate setting table in which the best slew rate for each signal sending condition is written is stored beforehand in each of the AT controller 14 or the main memory 13 of the host system 1 and the interface controller 31, 41 or the memory 33, 43 of the peripheral device 3. This procedure is executed, for example, in the manufacturing process of the subject computer system. For the peripheral device 3 supplied as a single unit, the procedure is executed in the manufacturing process thereof. In

this case, the storage for storing the slew rate setting table also composes the controller for setting a slew rate of the driver circuit 53 according to each signal sending condition.

For example, the slew rate of the driver circuit 53 is changed on each signal sending condition while a signal is sent and the waveform of the signal, as well as the data transfer error occurrence rate are monitored, thereby the best slew rate is decided and tabulated for each signal sending condition so as to be stored in both the host system 1 and peripheral device 3.

Figure 7 is a configuration of the slew rate setting table of the driver circuit 53. The table shown in Figure 7 is for the driver circuit that can set slew rates in seven or more steps like $sr1$ (maximum)> $sr2$ > $sr3$ > $sr4$ > $sr5$ > $sr6$ > $sr7$ > ... In the slew rate value (slew rate standard value) field in the table shown in Figure 7 are actually recorded bit values of the slew rate control signal SRC. The signal output device reads the bit values of the slew rate control signal SRC related to the object signal sending condition from the slew rate setting table and supplies the bit values to the driver circuit 53.

A signal output device provided with a slew rate setting table as shown in Figure 7 sets $sr1$ for the slew rate of the driver circuit 53 if the data transfer rate is 66.6[MB/s] and the cable type is 80C. If the data transfer rate is 44.4 or 33.3[MB/s] and the cable type is 80C, the signal output device sets $sr2$ (< $sr1$) for the slew rate of the driver circuit 53. And, if the data transfer rate is 33.3[MB/s] and the cable type is 40C, the signal output device sets $sr3$ (< $sr2$) for the slew rate of the driver circuit 53.

[How to Set Data Transfer Rate and Slew Rate of Driver Circuit]

Figure 8 is a flow chart for describing how to set a data transfer mode and a data transfer rate, as well as how to set a slew rate of a driver circuit 53 in Embodiment 1 according to the present invention. The setting procedure shown in Figure 8

enables commands and data to be sent between the host system 1 and the peripheral device 3. In this stage, however, none of the host system 1 and the peripheral device 3 recognizes the information of its partner's device, so the above data transfer is done, for example, in the PIO data transfer mode.

If the subject computer system is powered or reset, the host system 1 and the peripheral device 3 detect the type of the ATA cable 2 (40C or 80C cable) in steps S1 and S2.

Detecting the type of the ATA cable 2, the host system 1 sends a setting start command in the data transfer mode to the peripheral device 3 (HDD 3a or CD-ROM 3b) and requests the peripheral device 3 to notify the information (data transfer modes and data transfer rates supported by the peripheral device 3) to itself in step S3.

Receiving the setting start command in step S4, the peripheral device 3 notifies the host system 1 of its own information such as the data transfer modes and data transfer rates that the peripheral device 3 can support in step S5.

The host system 1, receiving the information of the peripheral device 3 in step S6, sets a data transfer mode and a data transfer rate to be used in the communication with the peripheral device 3 with reference to the data transfer modes and the data transfer rates that the peripheral device 3 can support, as well as the type of the ATA cable in use and the data transfer modes and the data transfer rates that the host system 1 itself can support in step S7. After that, the host system 1 notifies the peripheral device 3 of both set data transfer mode and data transfer rate that are set in step S8.

If the ATA cable 2 is a 40C cable, the host system 1 does not set a data transfer rate of 44.4[MB/s] or over which the 80C cable must set, but sets a data transfer rate of 33.3[MB/s] or under in step S7 even when the host system 1 and the peripheral device 3 can support a data transfer rate of 44.4[MB/s] or

over.

If the ATA cable 2 is a 40C cable, the peripheral device 3 may notify the host system 1 of the effect that it can support a data transfer rate of 33.3[MB/s] or under in step S5 even when it can support a data transfer rate of 44.4[MB/s] or over. The peripheral device 3 may also detect the cable type and notifies it to the peripheral device 3 or the host system 1 may detect the cable type and notifies it to the peripheral device 3.

Next, the host system 1 reads the bit value of the slew rate control signal SRC from the slew rate setting table stored in the main memory 13 or the AT controller 14 in step S9. The bit value is used to set the best slew rate on the subject signal sending condition comprising the set data transfer rate and the type of the cable in use. The host system 1 then supplies the read bit values to all the driver circuits 53 of the driver/receiver unit 14a. Consequently, all the driver circuit 53 are set to the best slew rate standard value on the above signal sending condition.

The peripheral device 3, receiving the report of both data transfer mode and data transfer rate that are set in step S10, reads the bit values of the slew rate control signal SRC from the slew rate setting table held in the memory 33 or 43 and supplies the bit values to all the driver circuits 53 of the driver/receiver unit 51a (31a or 41a) in step S11. The bit values are used to set the best slew rate on the above signal sending condition comprising the set data transfer rate and the type of the cable in use. Consequently, all the driver circuits 53 of the driver/receiver unit 51a are set to the best slew rate standard value on the above signal sending condition.

This completes setting of the data transfer mode and the data transfer rate, as well as setting of the slew rate of those driver circuits. Hereafter, data transfer can be made in the predetermined data transfer mode at the predetermined data transfer rate.

Comparison between Signal Output Device in Embodiment 1 and Conventional One

Figures 9 and 10 are charts for comparison between the signal waveforms of the signal output device in Embodiment 1 according to the present invention and the signal waveforms of the conventional signal output device. In Figures 9 and 10, (a) shows the waveforms of the strobe signal DST and the data signal DD output from the signal output device in Embodiment 1 and (b) shows the waveforms of the strobe signal DST and the data signal DD output from the conventional signal output device. The scales of the time axis (horizontal) and the potential axis (vertical) in Figures 9 and 10 are completely the same. The data transfer rate in Figure 9 is assumed to be VD1 and the data transfer rate in Figure 10 is assumed to be VD2 ($>VD1$).

The slew rate of the driver circuit of the signal output device in Embodiment 1 is set to the best value sra in Figure 9(a) and to the best value srb ($>sra$) in Figure 10(a). The slew rate of the driver circuit of the conventional signal output device is fixed and Figure 9(b) shows the signal waveform output from the driver circuit whose slew rate is fixed to srb and Figure 10(b) shows the signal waveform output from the driver circuit whose slew rate is fixed to sra .

Because a small slew rate value sra is set for the driver circuit 53 in Embodiment 1 shown in Figure 9(a), the cross talk noise is reduced. Consequently, data can be latched correctly at both start and end of the strobe signal DST in the signal receiving circuit. On the contrary, because the slew rate is fixed to a large value srb for the conventional driver circuit shown in Figure 9(b), a large cross talk noise remains in the data signal DD. Consequently, wrong data may possibly be latched at both start and end of the strobe signal DST in the signal receiving circuit.

Furthermore, because the driver circuit in Embodiment 1 shown

in Figure 11(a) is set to a large slew rate value srb , both "L" and "H" level periods are secured for both strobe signal DST and data signal DD and the data signal DD is set on the "L" or "H" level at both start and end of the strobe signal DST. Consequently, data can be latched correctly in the signal receiving device. On the contrary, because the conventional driver circuit shown in Figure 10(b) is fixed to a small slew rate value sra , the "L" level period is not secured enough for both strobe signal DST and data signal DD. Consequently, wrong data may possibly be latched.

How to Correct Slew Rate by Sending Error Occurrence Rate

Figure 11 is a flow chart for describing how to correct a slew rate in Embodiment 1 according to the present invention. At first, if data transfer is started in a data transfer mode and at a data transfer rate and at a slew rate standard value of the driver circuit set respectively in the procedure shown in Figure 8, the signal I/O devices of both host system 1 and peripheral device 3 (HDD 3a and CD-ROM drive 3b) start a statistical processing of the data transfer error occurrence rate of errors detected in data transfer between the host system 1 and the peripheral device 3 in step S21 in Figure 11.

The signal output device for outputting data delimits transmit data at a given length and adds an error correction code to each delimited data before sending it. In this case, the error correction code is a CRC (Cyclic Redundancy Check) code. The CRC code can verify whether or not the object data is correct and can correct an error within the predetermined number of bits. Such error verification by the CRC code is done in the peripheral device 3 in data transfer between the host system 1 and the peripheral device 3.

For example, when data is sent from the signal output device of the peripheral device 3 to the signal receiving device of the host system 1, the signal receiving device of the host system 1 calculates the data (CRC verification data) used for CRC

verification according to the received CRC code word (CRC code attached data) and notifies this CRC verification data to the signal output device of the peripheral device 3. The signal output device of the peripheral device 3 also calculates the CRC verification data about the CRC code word sent to the host system 1 separately, so the signal output device of the peripheral device 3 executes CRC verification according to the CRC verification data calculated by itself and the CRC verification data notified from the host system 1, thereby determining whether or not a sending error has occurred. The peripheral device 3 then notifies the result to the host system 1 and takes statistics of the sending error occurrence rate. If a sending error is detected, the peripheral device 3 sends the same data again and executes other necessary processings.

When data is sent from the signal output device of the host system 1 to the signal receiving device of the peripheral device 3, the signal receiving device of the peripheral device 3 executes CRC verification according to the received CRC code word (CRC code attached data) so as to determine whether or not a sending error has occurred. The host system 1 then notifies the result to the host system 1 and takes statistics of the sending error occurrence rate. If a sending error is detected, the host system 1 sends the same data again and executes other necessary processings.

Next, each signal I/O device determines whether or not the sending error occurrence rate is below an allowable threshold E_{th} in step S22. The determination in this step S22 is done each time the predetermined number of CRC code attached data items is sent (each time a predetermined amount of data is sent) or each time data is sent by the predetermined number of times or at a predetermined time interval. The allowable threshold E_{th} is 0 or another predetermined value. If the sending error occurrence rate is below the allowable threshold E_{th} , control returns to step S21. If the allowable threshold E_{th} is exceeded, control goes to step S23.

If the sending error occurrence rate is determined to be over the allowable threshold E_{th} in step S22, the subject signal I/O device decreases the slew rate of the driver circuit 53 by one from the set standard value in the slew rate setting table (table value) in step S23.

Next, the signal I/O device takes statistics of the sending error occurrence rate after the change of the slew rate in step S24 in the same procedure as that in step S21, then determines whether or not the sending error occurrence rate is below the allowable threshold E_{th} after the change of the slew rate in step S25 in the same procedure as that in step S22. If the sending error occurrence rate is below the allowable threshold E_{th} after the change of the slew rate, control goes to step S42. If it is over the allowable threshold E_{th} , control goes to step S26.

If the sending error occurrence rate is below the allowable threshold E_{th} after the change of the slew rate in step S25, in step S42, the subject signal I/O device updates the slew rate standard value of the object signal sending condition in the slew rate setting table to the value changed in step S23. Control then returns to step S21.

If the sending error occurrence rate is determined to be over the allowable threshold E_{th} after the change of the slew rate in step S25, then the signal I/O device determines in step S26 whether or not the sending error occurrence rate after the change of the slew rate is decreased from that before the change of the slew rate. If it is determined to be decreased, control goes to step S27 and if not, control goes to step S32.

If it is determined in step S26 that the sending error occurrence rate after the change of the slew rate is decreased from that before the change of the slew rate, then the signal I/O device decreases the slew rate of the driver circuit 53 by one in step S27. Then, in step S28, the signal I/O device takes statistics of the sending error occurrence rate after the

slew rate is changed in step S27 in the same procedure as that in step S21. After that, in step S29, the signal I/O device determines whether or not the sending error occurrence rate is below the allowable threshold E_{th} after the slew rate is changed in step S27 in the same procedure as that in step S22. If it is below the allowable threshold E_{th} , control goes to step S42, where the slew rate standard value of the signal sending condition in the slew rate setting table is updated to the value changed in step S27. If it is over the allowable threshold E_{th} , control goes to step S30.

In step S30, the signal I/O device determines whether or not the sending error occurrence rate after the slew rate is changed in step S27 is decreased from that before the change of the slew rate. If it is decreased, control returns to step S27 and the signal I/O device further decreases the slew rate of the driver circuit 53 by one and if not, control goes to step S31.

In step S31, the signal I/O device increases the slew rate of the driver circuit 53 by one from the current value (a slew rate that minimizes the sending error occurrence rate within a smaller value than the table value). After this, control goes to step S42 and the signal I/O device updates the slew rate standard value of the object signal sending condition in the slew rate setting table to the value changed in step S31. Control then returns to step S21.

Next, if it is determined in step S26 that the sending error occurrence rate after the change of the slew rate is not decreased from that before the change of the slew rate, the signal I/O device increases the slew rate of the driver circuit 53 by one from the standard value set in the slew rate setting table (table value) in step S32.

Next, in step S33, the signal I/O device takes statistics of the sending error occurrence rate after the slew rate is changed in step S32 in the same procedure as that in step S21

and determines in step S34 whether or not the sending error occurrence rate is below the allowable threshold E_{th} after the slew rate is changed in step S32 in the same procedure as that in step S22. Then, if the sending error occurrence rate is below the allowable threshold E_{th} after the slew rate is changed in step S32, control goes to step S42 and if not, control goes to step S35.

If it is determined in step S34 that the sending error occurrence rate is below the allowable threshold E_{th} , in step S42, the signal I/O device updates the slew rate standard value of the object signal sending condition in the slew rate setting table to the value changed in step S32. Control then returns to step S21.

If it is determined in step S34 that the sending error occurrence rate is over the allowable threshold E_{th} , the signal I/O device determines whether or not the sending error occurrence rate after the slew rate is changed in step S32 is decreased from that before the change in step S35. If it is decreased, control goes to step S36 and if not, control goes to step S41.

If it is determined in step S35 that the sending error occurrence rate is not decreased from that before the slew rate is changed, the signal I/O device returns the slew rate of the driver circuit 53 to the standard value set in the slew rate setting table (table value) in step S41. Control then returns to step S21.

If it is determined in step S35 that the sending error occurrence rate is decreased from that before the slew rate is changed, the signal I/O device further increases the slew rate of the driver circuit 53 by one in step S36, then in step 37 takes statistics of the sending error occurrence rate after the slew rate is changed in step S36 in the same procedure as that in step S21 and determines in step S38 whether or not the sending error occurrence rate is below the allowable threshold

Eth after the slew rate is changed in step S36 in the same procedure as that in step S21. If it is below the allowable threshold Eth, control goes to step S42 and updates the slew rate standard value of the object signal sending condition in the slew rate setting table to the value changed in step S36. If not below the allowable threshold Eth, control goes to step S39.

The signal I/O device determines in step S39 whether or not the sending error occurrence rate after the slew rate is changed in step S36 is decreased from that before the change. If it is decreased, control returns to step S36 and the signal I/O device further increases the slew rate of the driver circuit 53 by one. If not decreased, control goes to step S40.

In step S40, the signal I/O device decreases the slew rate of the driver circuit 53 by one from the current value (a slew rate that minimizes the sending error rate within a larger value than the table value). Control then goes to step S42 and updates the slew rate standard value of the object signal sending condition in the slew rate setting table to the value changed in step S40. Control then returns to step S21.

As described above, the procedure shown in Figure 11 changes the slew rate in the following steps of;

[A] setting the slew rate of the driver circuit 53 to a standard value according to the predetermined data transfer rate, thereby starting signal sending;

[B] determining whether or not the data transfer error occurrence rate is below the allowable threshold Eth while the data transfer error occurrence is caused by a signal sent to the signal receiving device from the driver circuit 53 (steps S21 and S22);

[C] changing the slew rate of the driver circuit 53 if it is determined in [B] that the sending error occurrence rate is

over the allowable threshold E_{th} , then searching a slew rate value that decreases the sending error occurrence rate below the allowable threshold E_{th} or decreases the sending error occurrence rate in [B] (steps S23 to S40);

[D] setting the searched slew rate value as a new standard value if the slew rate value decreases the sending error occurrence rate below the allowable threshold E_{th} or decreases the sending error occurrence rate in [C] (step S42).

The step [C] in which a slew rate that decreases the sending error occurrence rate below the allowable threshold E_{th} or decreases it more is further divided into the following steps;

[C1] decreasing the slew rate of the driver circuit 53 from the standard value if the sending error occurrence rate is over the allowable threshold E_{th} in [B], then determining whether or not the sending error occurrence rate is decreased (steps S23 to S26);

[C2] searching a slew rate value that decreases the sending error occurrence rate below the allowable threshold E_{th} or minimizes it within a smaller value than the standard value if the sending error occurrence rate is decreased in [C1] (steps S25 and S27 to S31);

[C3] increasing the slew rate from the standard value if the sending error occurrence rate is not decreased in [C1], then determining whether or not the sending error occurrence rate is decreased (steps S32 to S35); and

[C4] searching a slew rate value that decreases the sending error occurrence rate below the allowable threshold E_{th} or minimizes it within a larger value than the standard value if the sending error occurrence rate is decreased in [C3] (steps S34 and S36 to S40).

The slew rate correction procedure described above is also

effective to obtain high signal integrity on every signal sending condition even when the slew rate standard value set in the slew rate setting table is not the best and the best slew rate is changed dynamically.

According to Embodiment 1 described above, because the signal output device is composed so as to include a driver circuit that can set a plurality of different slew rates and can set the best slew rate according to each signal sending condition comprising a predetermined data transfer rate and a type of the cable in use, high signal integrity can be obtained on each signal sending condition.

Furthermore, because the data transfer error occurrence rate is monitored while the error occurrence is caused by a signal sent to a signal receiving device from a driver circuit and the slew rate of the driver circuit is changed to a value that can decrease the sending error occurrence rate below a predetermined allowable threshold or decrease it more if the sending error occurrence rate is over the predetermined allowable threshold, high signal integrity can be obtained on each signal sending condition even when the object slew rate standard value set in the slew rate setting table is not the best and the best slew rate is changed dynamically.

Although the best slew rate is set according to a predetermined data transfer rate and a type of the cable in use in Embodiment 1 described above, the signal output device may be composed so as to set the best slew rate according to only a data transfer rate.

The best slew rate that can obtain high signal integrity also depends on the number of peripheral devices connected to the same cable. Consequently, the best slew rate may be set according to a signal sending condition. The condition consists of a data transfer rate and a type of the cable in use that are set according to the number of peripheral devices connected to the same cable and detected by the signal output

device of the host system or a peripheral device, as well as the number of the peripheral devices connected to the same cable.

Embodiment 2

The electrical properties (mutual conductance, threshold voltage, etc.) should preferably be the same between pMOS transistors and nMOS transistors of a driver circuit. However, those electrical properties may possibly be different between the pMOS transistors and nMOS transistors due to various conditions including the manufacturing process, etc. in some cases. In such a case, the same slew rate cannot be obtained at both start and end of an output signal of the driver circuit if the same timing is set for switching both a plurality of pMOS transistors and a plurality of nMOS transistors of the driver circuit as shown in (Figure 5) in Embodiment 1 described above.

In order to avoid such a trouble, the signal output device in Embodiment 2 is provided with a driver circuit that can adjust a slew rate at the start of its output signal from the driver circuit and a slew rate at the end of its output signal separately, thereby the same slew rate can be set at both start and end of its output signal even when electrical properties are different between transistors thereof.

Figure 12 is a block diagram of a driver circuit of the signal output device in Embodiment 2 according to the present invention. In Figure 12, the same symbols are given to the same parts as those shown in Figure 5. The driver circuit shown in Figure 12 is provided with pMOS transistors p1 to p4, nMOS transistors n1 to n4, delay circuits DL1 to DL6, switching circuits SW1 to SW6, and an inverter IV.

The driver circuit shown in Figure 12 is composed so that the switching timing of each of the pMOS transistors p1 to p4 can be adjusted separately from that of each of the nMOS

transistors n1 to n4, thereby the slew rate at the start of its output signal can be adjusted separately from that at the end of the output signal. The delay circuits DL1 to DL3 and the switching circuits SW1 to SW3 are combined so as to compose a device (a first device) for setting a slew rate at the start of the output signal from the driver circuit when the switching timing of each of the pMOS transistors p1 to p4 is set according to the values of the bits b1 to b3 of the slew rate control signal SRC. The delay circuits DL4 to DL6 and the switching circuits SW4 to SW6 are combined so as to compose a device (a second device) for setting a slew rate at the end of an output signal from the driver circuit when the switching timing of each of the nMOS transistors n1 to n4 is set according to the values of the bits b4 to b6 of the slew rate control signal SRC.

Because the slew rate at the start of an output signal from the driver circuit can be adjusted separately from that at the end of the output signal as described above, the same slew rate can be set for both start and end of the output signal even when the electrical properties differ between pMOS transistors and nMOS transistors.

The inverter IV inverts the transmit signal SIN entered to the signal input terminal "in" from the controller, thereby supplying the inverted transmit signal rSIN to the gate electrodes of the transistors p1 and n1, the input terminals of the delay circuits DL1 and DL4, as well as to the terminals A of the switching circuits SW1 to SW6 respectively.

The delay circuit DLk delays an input signal and supplies the delayed signal to the terminal B of the switching circuit SWk. In this case, the signal delay time of each of the delay circuits DL1 to DL6 is assumed to be T.

The slew rate control signal SRC entered to the terminal src from the interface controller is used to set a slew rate of the driver circuit. It is a 6-bit signal comprising b1 to b6. The

bit b_k ($k = 1, 2, \dots, 6$) of the slew rate control signal SRC is entered to the switching circuit SW k . Bits b_1 to b_3 are signals for controlling the switching timing of the pMOS transistors p_1 to p_4 so as to set a slew rate at the start of an output signal from the driver circuit. Bits b_4 to b_6 are signals for controlling the switching timing of the nMOS transistors n_1 to n_4 so as to set a slew rate at the end of the output signal.

The switching circuit SW k connects the terminal C to the terminal A or B according to the logical value of the bit b_k of the slew rate control signal SRC. In this case, the switching circuit SW k connects the terminal C to the terminal A at $b_k = "0"$ and to the terminal B at $b_k = "1."$ The terminals C of the switching circuits SW1 to SW3 are connected to the gate electrodes of the pMOS transistors p_2 to p_4 respectively. The terminals C of the switching circuits SW4 to SW6 are connected to the gate electrodes of the nMOS transistors n_2 to n_4 respectively.

The source electrodes of the transistors p_1 to p_4 are connected to the power supply VDD and the drain electrodes are connected to the output terminal "out" respectively. The source electrodes of the transistors n_1 to n_4 are connected to the ground GND and the drain electrodes are connected to the output terminal "out" respectively. The output terminal "out" is connected to the AT cable 2 (see Figures 3 and 4) and the transmit signal SOUT output from the driver circuit at a predetermined slew rate is supplied to the AT cable 2.

The transistor p_1 is switched according to the transmit signal rSIN and the transistor p_2 is switched according to a signal supplied from the switching circuit SW1. The transistor p_3 is switched according to a signal supplied from the switching circuit SW2. The transistor p_4 is switched according to a signal supplied from the switching circuit SW3. The transistor n_1 is switched according to the transmit signal rSIN. The transistor n_2 is switched according to a signal supplied from

the switching circuit SW4. The transistor n3 is switched according to a signal supplied from the switching circuit SW5. The transistor n4 is switched according to a signal supplied from the switching circuit SW6.

Figure 13 is a table for describing the operation of the driver circuit shown in Figure 12. The table shows the correspondence between set values of the switching circuits SW1 to SW6 and the slew rates of the object driver circuit. As shown in Figure 13, the driver circuit shown in Figure 12 enables the same slew rate to be set at both start and end of its output signal, as well as in the four steps of sr1 (max.), sr2 (<sr1), sr3 (<sr2), and sr4 (<sr3) according to the slew rate control signal SRC (bits b1 to b6).

The driver circuit shown in Figure 12 enables the slew rate at the start of its output signal to be set in five steps according to the set values of the switching circuits SW1 to SW3 and the slew rate at the end of its output signal to be set in five steps according to the set values of the switching circuits SW4 to SW6.

For example, if SW1-3 = (ABA) is described for a case that the switching circuit SW1 is set to the terminal A, the terminal B, and the terminal A, then the slew rate at the start of an output signal will be as shown below.

At SW1-3 = (AAA) ... rsr1 (max.)
 At SW1-3 = (AAB) ... rsr2 (<rsr1)
 At SW1-3 = (BAB) ... rsr3 (<rsr2)
 At SW1-3 = (ABB) ... rsr4 (<rsr3)
 At SW1-3 = (BBB) ... rsr5 (<rsr4)

At SW1-3 = (ABA) and (BAA), rsr2 is assumed just like at SW1-3 = (AAB). At SW1-3 = (BBA), rsr4 is assumed just like at SW1-3 = (ABB).

In the same way, the slew rate at the end of an output signal

from the driver circuit will be as shown below.

At SW4-6 = (AAA) ... fsr1 (max.)
 At SW4-6 = (AAB) ... fsr2 (<fsr1)
 At SW4-6 = (BAB) ... fsr3 (<fsr2)
 At SW4-6 = (ABB) ... fsr4 (<fsr3)
 At SW4-6 = (BBB) ... fsr5 (<fsr4)

The driver circuit shown in Figure 12 disables the same slew rate to be set at both start and end of its output signal due to a difference of electrical properties (mutual conductance, threshold voltage, etc.) between the pMOS transistors p1 to p4 and the nMOS transistors n1 to n4 when the same switching timing is set for the pMOS transistors p1 to p4 and the nMOS transistors n1 to n4. It is assumed that the slew rate becomes like $fsr1 > rsr1 \approx fsr2 > rsr2 \approx fsr3 > rsr3 \approx fsr4 > rsr4 \approx fsr5 > rsr5$ when the slew rates rsr1 to rsr5 at the start and slew rates fsr1 to fsr5 at the end of an output signal from the driver circuit are observed at each switch setting.

Figure 13 is a table for describing setting of the switching circuits of the driver circuit in the above case. When SW1-3 = (AAA) and SW4-6 = (AAB) are set, the same sr1 (max.) (= rsr1 = fsr2) is set for the slew rate of both start and end of an output signal from the driver circuit. When SW1-3 = (AAB) and SW4-6 = (BAB) are set, the same sr2 (= rsr2 = fsr3 < sr1) is set for the slew rate of both start and end of an output signal from the driver circuit. When SW1-3 = (BAB) and SW4-6 = (ABB) are set, the same sr3 (= rsr3 = fsr4 < sr2) is set for the slew rate of both start and end of an output signal from the driver circuit. And, when SW1-3 = (ABB) and SW4-6 = (BBB) are set, the same sr4 (= rsr4 = fsr5 < sr3) is set for the slew rate of both start and end of an output signal from the driver circuit.

In the above case, the driver circuit shown in Figure 12 can adjust the slew rate in four steps of sr1 to sr4. Any of the above switch settings is written as the best slew rate (standard value) to each signal sending condition in the slew

rate setting table (see Figure 7). For example, if $sr1$ is set for the slew rate of the driver circuit, $SW1-3 = (AAA)$ and $SW4-6 = (AAB)$ switch settings are written.

For example, if the slew rate control signal SRC is set to $b1 = b2 = "0," b3 = b4 = "1," b5 = "0,"$ and $b6 = "1"$ and switching circuits $SW1, SW2,$ and $SW5$ are set to the terminal A and switching circuits $SW3, SW4,$ and $SW6$ are set to the terminal B respectively, the driver circuit shown in Figure 12 will operate at a slew rate of $sr2$ at both start and end of the output signal. At this time, the inverted transmit signal $rSIN$ is supplied to the gate electrodes of the transistors $p1$ to $p3$ and $n1$ and $n3$ while a signal delayed by a time T from the inverted transmit signal $rSIN$ is supplied to the gate electrodes of the transistors $p4, n2,$ and $n4$ respectively.

When the level of the transmit signal SIN is changed from "L" to "H," the transistors $p1$ to $p3$ are turned on and the transistors $n1$ and $n3$ are turned off. A time T after that, the transistor $p4$ is turned on and the transistors $n2$ and $n4$ are turned off. With the switching operations of those transistors, the level of the transmit signal $SOUT$ is changed from "L" to "H."

When the level of the transmit signal SIN is changed from "H" to "L," the transistors $p1$ to $p3$ are turned off and the transistors $n1$ and $n3$ are turned on. A time T after that, the transistor $p4$ is turned off and the transistors $n2$ and $n4$ are turned on. With the switching operations of those transistors, the level of the transmit signal $SOUT$ is changed from "H" to "L."

Consequently, when the level of the transmit signal SIN is changed from "L" to "H," the driver circuit drives the AT cable 2 according to the switching states of the transistors $p1$ to $p3$, then a time T after that, the driver circuit drives the AT cable 2 with its maximum current driving performance obtained by the transistors $p1$ to $p4$, thereby the driver circuit

operates at a slew rate of $sr2(rsr2)$ at the start of its output signal. When the level of the transmit signal SIN is changed from "H" to "L," the driver circuit drives the AT cable 2 first according to the switching states of the transistors $n1$ and $n3$, then a time T after that, the driver circuit drives the AT cable 2 with its maximum current driving performance obtained by the transistors $n1$ to $n4$, thereby the driver circuit operates at a slew rate of $sr2(=sr3)$ at the end of its output signal.

In accordance with Embodiment 2 according to the present invention as described above, because the driver circuit is composed so that the slew rate at the start of its output signal can be adjusted separately from the slew rate of the end of the output signal, it is possible to set the best slew rate on each signal sending condition, thereby obtaining high signal integrity on each signal sending condition, as well as it is possible to set the same slew rate at both start and end of the output signal even when the electrical properties are different between transistors composing the driver circuit.

Advantages of the invention

As described above, according to the present invention, because the signal output device is provided with a driver circuit that can set a plurality of different slew rates and can set the best slew rate according to a predetermined data transfer rate, high signal integrity can be obtained on each data transfer rate (or each signal sending condition comprising a data transfer rate and a signal sending type).

Furthermore, because the rate of the data transfer error occurrence, which is caused by a signal sent to a signal receiving device from a driver circuit, is monitored so that the slew rate of the driver circuit is changed to a value that decreases the sending error occurrence rate below an allowable threshold or decreases it more if the sending error occurrence rate is over the allowable threshold, it is possible to obtain

high signal integrity at each data transfer rate (or on each signal sending condition comprising a data transfer rate and a signal sending line type) even when a slew rate standard value set in the slew rate setting table is not the best and when the best slew rate is changed dynamically.

Furthermore, because the slew rate at the start of an output signal from the driver circuit can be adjusted separately from the slew rate at the end of the output signal, the same slew rate can be set at both start and end of the output signal even when the electrical properties differ among the transistors of the driver circuit.

4. Brief Description of the Drawings:

Figure 1 is a block diagram of a computer system in Embodiment 1 according to the present invention;

Figure 2 shows tables for describing an ATA interface standard;

Figure 3 is a block diagram of a signal sending system conforming to the ATA interface composed of a signal I/O device of a host system, an ATA cable, and the signal I/O device of a peripheral device (HDD or CD-ROM drive) shown in Figure 1;

Figure 4 is a circuit diagram of a driver/receiver unit of the peripheral device (HDD or CD-ROM drive) shown in Figure 3;

Figure 5 is a circuit diagram of a driver circuit provided in the signal output device in Embodiment 1 according to the present invention;

Figure 6 shows a table for describing the operation of the driver circuit shown in Figure 5;

Figure 7 is a block diagram of a slew rate setting table of a driver circuit provided in the signal output device in Embodiment 1 according to the present invention;

Figure 8 is a flow chart of procedures for setting both data transfer mode and data transfer rate, as well as a procedure for setting a slew rate of a driver circuit in Embodiment 1 according to the present invention;

Figure 9 shows charts for the comparison between the signal waveform of the signal output device in Embodiment 1 according to the present invention and the signal waveform of the conventional signal output device (at a low data transfer rate);

Figure 10 shows charts for the comparison between the signal waveform of the signal output device in Embodiment 1 according to the present invention and the signal waveform of the conventional signal output device (at a high data transfer rate);

Figure 11 is a flow chart of the procedure for correcting a slew rate in Embodiment 1 according to the present invention;

Figure 12 is a circuit diagram of a driver circuit provided in the signal output device in Embodiment 2 according to the present invention; and

Figure 13 is a table for describing the operation of the driver circuit shown in Figure 12.

Description of symbols

- 1 ... Host System
- 2 ... ATA Cable
- 3 ... Peripheral Device
- 3a ... HDD
- 3b ... CD-ROM Drive
- 10 ... Mother Board
- 11 ... CPU
- 13 ... Main Memory
- 14 ... AT Controller

14a ... Driver/Receiver Unit
26 ... ATA Port
30 ... Card
31 ... ATA Interface Controller
31a ... Driver/Receiver Unit
32 ... MPU
33 ... Memory
40 ... Card
41 ... ATAPI Controller
41a ... Driver/Receiver Unit
42 ... MPU
43 ... Memory
51 ... Interface Controller
51a ... Driver/Receiver Unit
52 ... Driver/Receiver Circuit
53 ... Driver Circuit
DL1 to DL6 ... Delay Circuit
SW1 to SW6 ... Switching Circuit
p1 to p4 ... pMOS Transistor
n1 to n4 ... nMOS Transistor

CLAIMS

1. A signal output device, comprising:

a driver circuit for setting a plurality of different slew rates and relaying a signal to a signal sending line at a selected slew rate among said plurality of different slew rates;

a controller for selecting said selected slew rate of said driver circuit according to a predetermined data transfer rate, said controller being configured to set said selected slew rate of said driver circuit according to said predetermined data transfer rate and a type of said signal sending line, wherein said controller includes a memory system for storing a table containing a slew rate for each predetermined data transfer rate, said slew rate of said driver circuit being set with reference to said table.

2. The signal output device, according to claim 1, wherein said driver circuit is included on an integrated circuit with at least part of said controller.

3. The signal output device according to claim 1, wherein said driver circuit further comprises:

a plurality of CMOS circuits; and

a setting device for delaying a switching timing of each of a plurality of said CMOS circuits to control a wave shape of a transmission by a delay time set according to a control signal from said controller, said setting device including a delay circuit and a switching circuit.

4. The signal output device, according to claim 1, wherein said controller monitors a rate of data transfer error occurrence caused by a signal sent to a signal receiving device from said driver circuit and changes said slew rate of said driver circuit to a value that can decrease said data transfer error occurrence rate below a predetermined allowable threshold.

5. A signal output device, comprising:

a driver circuit for setting a plurality of different slew rates and relaying a signal to a signal sending line at a selected slew rate among said plurality of different slew rates; and

a controller for selecting said selected slew rate of said driver circuit according to a predetermined data transfer rate, said driver circuit being configured to adjust a first slew rate at the start of its output signal separately from a second slew rate at the end of said output signal, wherein said controller includes a memory system for storing a table containing a slew rate for each predetermined data transfer rate, said slew rate of said driver circuit being set with reference to said table.

6. The signal output device, according to claim 5, wherein said driver circuit further, comprises:

a plurality of first conductive transistors provided between a signal output terminal and a first power supply;

a plurality of second conductive transistors placed between said signal output terminal and a second power supply;

a first setting device for setting a turn-on timing of each of a plurality of said first conductive transistors according to a first control signal from said signal output device if the level of an inputted signal is changed from a first level to a second level; and

a second setting device for setting a turn-on timing of each of a plurality of said second conductive transistors according to a second control signal from said signal output device if the level of said inputted signal is changed from said second level to said first level.

7. A signal sending system, enabling a signal to be sent to a host system via a signal sending line, comprising:

a signal output device that can set a plurality of different data transfer rates and send a signal to an object device via a signal sending line at a selected data transfer rate, said signal output device including:

a driver circuit for setting a plurality of different slew rates and relaying a signal to a signal sending line at a predetermined slew rate; and

a controller for setting a slew rate of said driver circuit according to a predetermined data transfer rate from a signal output device provided for a host system, a type of said signal sending line, and a quantity of peripheral devices connected to said signal sending line.

8. The signal sending system, according to claim 7, wherein said signal sending system conforms to the ATA interface standard.

9. The signal sending system, according to claim 7, wherein said signal sending line is one of a plurality of signal sending lines included in a flat cable.

10. The signal sending system, according to claim 7, further comprising a peripheral device selected from the group consisting of a hard disk drive (HDD), a compact disc read only memory (CD-ROM) drive and a digital video disc (DVD) drive.

11. The signal sending system, according to claim 7, wherein said signal output device is mounted on a card of a peripheral device or on the mother board of said host system.

12. The signal sending system, according to claim 7, wherein said signal output device is mounted on a mother board of said host system.