Resistivity substrate). This HR substrate is advantageously combined with a charge-trapping layer (or “trap-rich layer”).

However, this type of substrate is not compatible with the use of transistors with a threshold voltage that must be controlled via a back-side gate (back-bias voltage). Indeed, the presence of this layer comprising trapped charges hinders back biasing (application of a potential difference to the back face).

The scientific publication entitled “Low loss Si-substrates enhanced using buried PN junctions for RF Applications” (M. Rack, L. Nyssens, and J-P. Raskin, IEEE Electron device letters, vol. 40, Issue 5) describes the formation of P-N junctions laterally arranged under the electrically insulating layer of a substrate intended for radiofrequency applications.

Laterally is understood to mean that two respectively P-doped and N-doped regions are arranged at the same depth of the substrate, with the junction between said regions being substantially perpendicular to the main surface of the substrate. Such a junction is obtained by implanting phosphorus over the whole substrate for N-type doping, followed by localized implantation of boron through a mask in order to form P-doped regions, then thermal treatment for activating the dopants.

Whilst a doped semiconductor is a good conductor, the junction hardly lets through any electrical current, thereby preventing the propagation of parasitic electric fields.

One disadvantage resulting from a lateral arrangement of the P-N junction as described in the scientific publication is that it requires a lithography step for forming the mask and two implantation steps, which represents a significant additional expense.

BRIEF DESCRIPTION OF THE INVENTION

The present disclosure seeks to propose a method for manufacturing a semiconductor-on-insulator structure that allows the aforementioned disadvantages to be overcome.

In particular, the present disclosure seeks to propose such a manufacturing method for manufacturing an FD-SOI structure exhibiting good radiofrequency performance capabilities.

An aspect of the present invention provides a method for manufacturing a semiconductor-on-insulator structure, comprising the following steps:

- providing an FD-SOI substrate successively comprising, from its base to its top:
  - a monocrystalline semiconductor substrate having electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and having first P- or N-type doping;
  - an electrically insulating layer having a thickness ranging between 20 nm and 400 nm;
  - a monocrystalline semiconductive layer having P-type doping;
- heat treating the FD-SOI substrate at a temperature greater than or equal to 1175°C for a time greater than or equal to 1 hour, in order to form a P-N junction in the

monocrystalline semiconductor substrate at a determined depth with respect to the electrically insulating layer,

- by diffusing P-type dopants from the monocrystalline semiconductive layer through the electrically insulating layer in said substrate; and
- if the monocrystalline semiconductor substrate is P-type doped, forming, in said monocrystalline semiconductor substrate, heat donors by precipitation of the interstitial oxygen; and

in order to form, in the monocrystalline semiconductor substrate, a first N-type doped region extending between the base of the monocrystalline semiconductor substrate and the P-N junction and a second P-doped region located between the first region and the electrically insulating layer.

The main technique for measuring interstitial oxygen in the silicon of a semiconductor substrate is infrared absorption using Fourier Transform InfraRed (FTIR) spectrometry.

This FTIR measurement provides a value of an absorption coefficient α_{OX} due to the interstitial oxygen. The interstitial oxygen concentration is computed on the basis of this absorption coefficient α_{OX}, in accordance with the method that is particularly described in the document entitled “A Study of Oxygen Precipitation in Heavily Doped Silicon” (1989), Graupner, Robert Kurt, Dissertations and Theses, Paper 1218.

According to this method, the oxygen concentration as atoms per cm^3 (at/cm^3) or as a fraction of the total number of atoms present in parts per million (ppma) is obtained by multiplying the absorption coefficient α_{OX} by a conversion factor.

The oxygen concentration referred to in the invention (old ppma) is obtained by using the first of the four conversion factors presented in the following list, called “old ASTM” (American Society for Testing), expressed as ppma:

Old ASTM	$ppma = 9.63\alpha_{OX}$
(ASTM F121-79)	$atoms/cm^3 = 4.81 \times 10^{17}\alpha_{OX}$
New ASTM	$ppma = 4.9\alpha_{OX}$
(ASTM F121-83)	$atoms/cm^3 = 2.45 \times 10^{17}\alpha_{OX}$
JEIDA	$ppma = 6.1\alpha_{OX}$
	$atoms/cm^3 = 3.03 \times 10^{17}\alpha_{OX}$
IOC-88	$ppma = 6.28\alpha_{OX}$
	$atoms/cm^3 = 3.14 \times 10^{17}\alpha_{OX}$

The manufacturing method according to embodiments of the invention has the different following features taken alone or according to their technically possible combinations:

- the monocrystalline substrate is made of silicon and/or the monocrystalline layer is a silicon layer;

- the FD-SOI substrate is obtained by transferring a layer of a donor substrate onto a recipient substrate, according to the following steps:
  - supplying:
    - the donor substrate comprising a monocrystalline semiconductive layer having P-type doping, and an embrittlement zone located in the monocrystalline silicon layer defining the layer to be transferred; and
    - the monocrystalline semiconductor recipient substrate, having electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and P- or N-type doping;
  - bonding the donor substrate onto the recipient substrate by means of an electrically insulating layer, the thickness of which ranges between 20 nm and 400 nm;
  - detaching the donor substrate along the embrittlement zone in order to form the FD-SOI substrate;
- the FD-SOI substrate is obtained by transferring a layer of a donor substrate onto a recipient substrate, according to the following steps:
  - supplying:
    - the donor substrate comprising a monocrystalline semiconductive layer having P-type doping; and
    - the monocrystalline semiconductor recipient substrate, having electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and P- or N-type doping;
  - bonding the donor substrate onto the recipient substrate by means of an electrically insulating layer, the thickness of which ranges between 20 nm and 400 nm;
  - thinning the donor substrate from the surface opposite the receiver substrate in order to form the transferred layer, so as to obtain the FD-SOI substrate;
- the embrittlement zone is formed by implanting atomic species in the donor substrate so as to define the transfer layer;
- the recipient substrate and the monocrystalline layer of the donor substrate are P-doped with boron;
- the P-N junction is formed at a depth ranging between 1 µm and 5 µm from the electrically insulating layer;
- the electrically insulating layer comprises a silicon oxide layer.

There is also disclosed a semiconductor-on-insulator structure obtained directly by implementing the previously described manufacturing method, wherein said semiconductor-on-insulator structure successively comprises, from its base to its top:

- a monocrystalline semiconductor substrate having electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and comprising:
  - a first region comprising N-type doping;
  - a second region arranged on the first region, comprising P-type doping, the second region being separated from the first region by a P-N junction;
- an electrically insulating layer;
- a monocrystalline semiconductive layer comprising P-type doping.

The structure as disclosed has the different following features taken alone or according to their technically possible combinations:

- the monocrystalline semiconductive layer is P-doped with boron;
- the P-N junction is located at a depth ranging between 1 μm and 5 μm from the electrically insulating layer;
- the electrically insulating layer comprises a silicon oxide layer;
- the monocrystalline substrate is made of silicon and/or the monocrystalline layer is a silicon layer.

DESCRIPTION OF THE FIGURES

Further advantages and features of the invention will become apparent upon reading the following description, which is provided by way of an illustrative and non-limiting example, with reference to the following appended figures, in which:

- figure 1 is a diagram of an FD-SOI substrate;

- figure 2 is a diagram of a semiconductor-on-insulator structure comprising a P-N junction, according to the invention;

- figure 3 is a diagram that illustrates the inversion of the doping of a portion of the monocrystalline substrate with high electrical resistivity;

- figure 4 is a diagram that illustrates the diffusion of the dopant from the monocrystalline layer through the underlying electrically insulating layer;

- figure 5A is a diagram that illustrates the formation of an embrittlement zone by implanting atomic species in a donor substrate, according to a first embodiment;

- figure 5B is a diagram that illustrates the bonding of the donor substrate onto a recipient substrate according to the first embodiment;

- figure 5C is a diagram that illustrates the detachment of the donor substrate along the embrittlement zone, and the transfer of a layer from the donor substrate onto the recipient substrate, according to the first embodiment;

- figure 6A is a diagram that illustrates the bonding of the donor substrate onto a recipient substrate according to a second embodiment;

CLAIMS

1. A method for manufacturing a semiconductor-on-insulator structure, comprising the following steps:

- providing a Fully-Depleted Silicon-On-Insulator (FD-SOI) substrate successively comprising, from its base to its top:
  - a monocrystalline semiconductor substrate having an electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and having first P- or N-type doping;
  - an electrically insulating layer having a thickness ranging between 20 nm and 400 nm;
  - a monocrystalline semiconductive layer having P-type doping;
- heat treating the FD-SOI substrate at a temperature greater than or equal to 1175°C for a time greater than or equal to 1 hour, in order to form a P-N junction in the monocrystalline semiconductor substrate at a determined depth with respect to the electrically insulating layer,
  - by diffusing P-type dopants from the monocrystalline semiconductive layer through the electrically insulating layer in said substrate; and
  - if the monocrystalline semiconductor substrate has P-type doping, forming, in said monocrystalline semiconductor substrate, heat donors by precipitation of the interstitial oxygen;

in order to form, in the monocrystalline semiconductor substrate, a first region having N-type doping extending between the base of the monocrystalline semiconductor substrate and the P-N junction and a second P-doped region located between the first region and the electrically insulating layer.

2. The manufacturing method as claimed in claim 1, wherein the monocrystalline semiconductor substrate is made of silicon and/or the monocrystalline semiconductive layer is a silicon layer.

3. The manufacturing method as claimed in claim 1 or claim 2, wherein the FD-SOI substrate is obtained by transferring a layer of a donor substrate onto a recipient substrate, according to the following steps:

- supplying:
  - the donor substrate comprising the monocrystalline semiconductive layer having P-type doping, and an embrittlement zone located in the monocrystalline semiconductive layer defining a layer to be transferred; and

- the recipient substrate having an electrical resistivity ranging between 500 Ω.cm and 30 k Ω.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and first P- or N-type doping;

- bonding the donor substrate onto the recipient substrate by means of the electrically insulating layer, the thickness of which ranges between 20 nm and 400 nm;

- detaching the donor substrate along the embrittlement zone in order to form the FD-SOI substrate.

4. The manufacturing method as claimed in claim 1 or claim 2, wherein the FD-SOI substrate is obtained by transferring a layer of a donor substrate onto a recipient substrate, according to the following steps:

- supplying:
  - the donor substrate comprising the monocrystalline semiconductive layer having P-type doping; and
  - the recipient substrate having an electrical resistivity ranging between 500 Ω.cm and 30 kΩ.cm, an interstitial oxygen content ranging between 20 and 40 old ppma, and P- or N-type doping;

- bonding the donor substrate onto the recipient substrate by means of the electrically insulating layer, the thickness of which ranges between 20 nm and 400 nm;

- thinning the donor substrate from the surface opposite the recipient substrate in order to form the transferred layer, so as to obtain the FD-SOI substrate.

5. The method as claimed in claim 3, wherein the embrittlement zone is formed by implanting atomic species in the donor substrate so as to define the layer to be transferred.

6. The method as claimed in any one of claims 3 to 5, wherein the recipient substrate and the monocrystalline semiconductive layer of the donor substrate are P-doped with boron.

7. The method as claimed in any one of the preceding claims, wherein the P-N junction is formed at a depth ranging between 1 μm and 5 μm from the electrically insulating layer.

8. The method as claimed in any one of the preceding claims, wherein the electrically insulating layer comprises a silicon oxide layer.