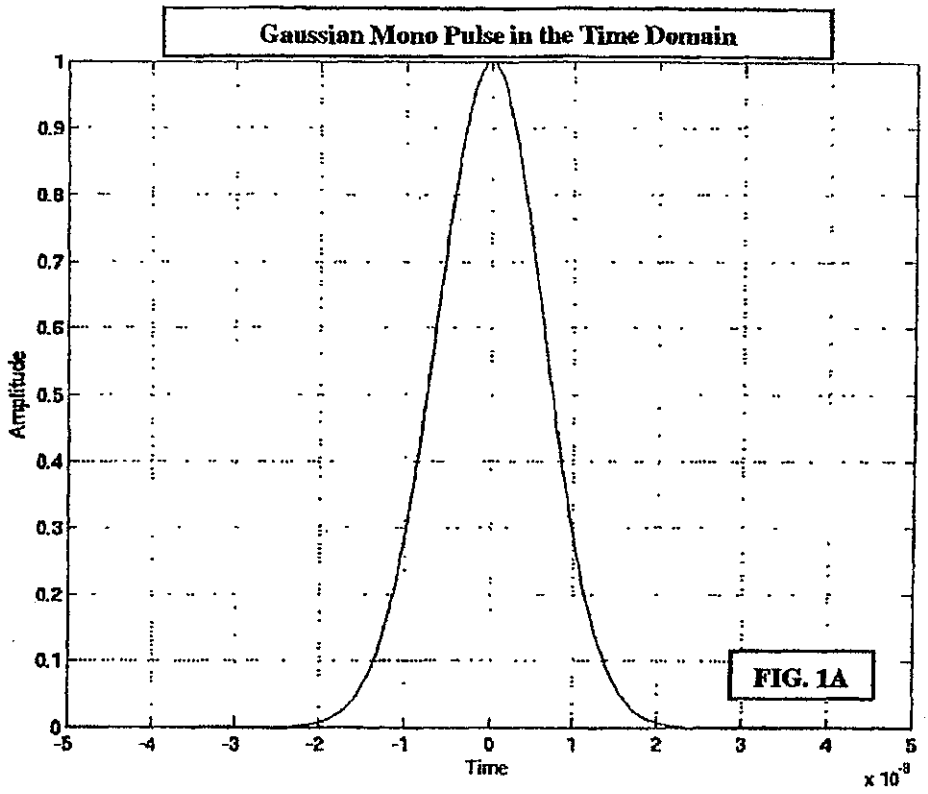

Gaussian Mono Pulse in the Time Domain
Amplitude
Time
x 10^-8

FIG. 1A

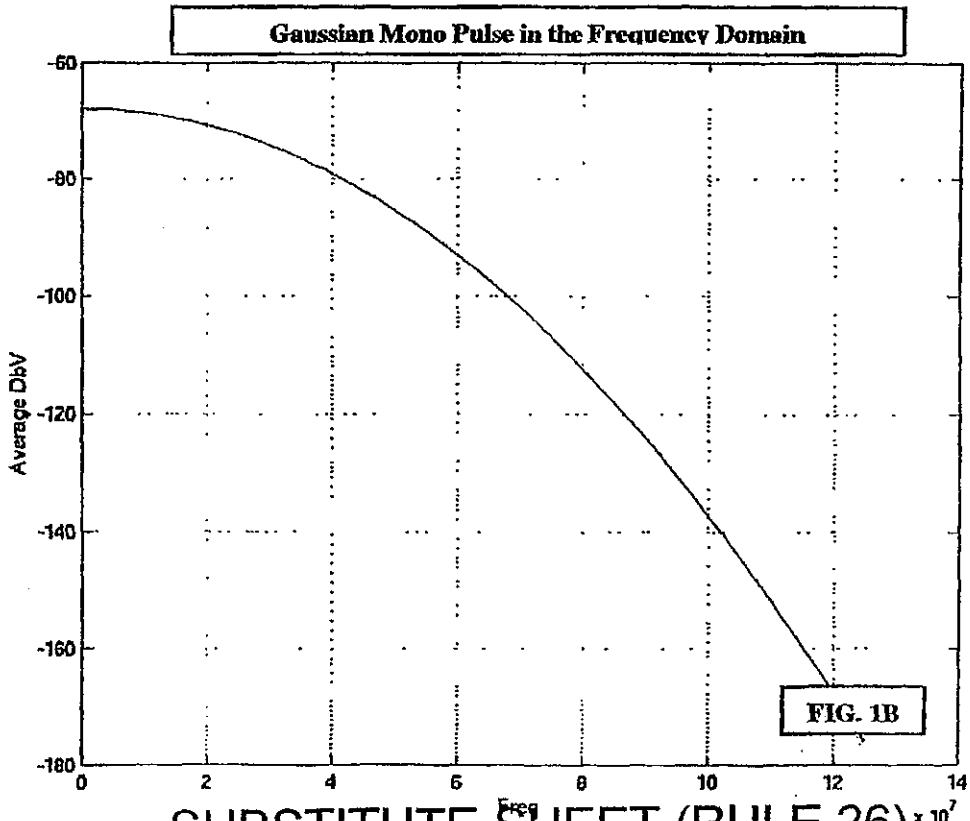

Gaussian Mono Pulse in the Frequency Domain
Average DbV
Freq
x 10^7

FIG. 1B

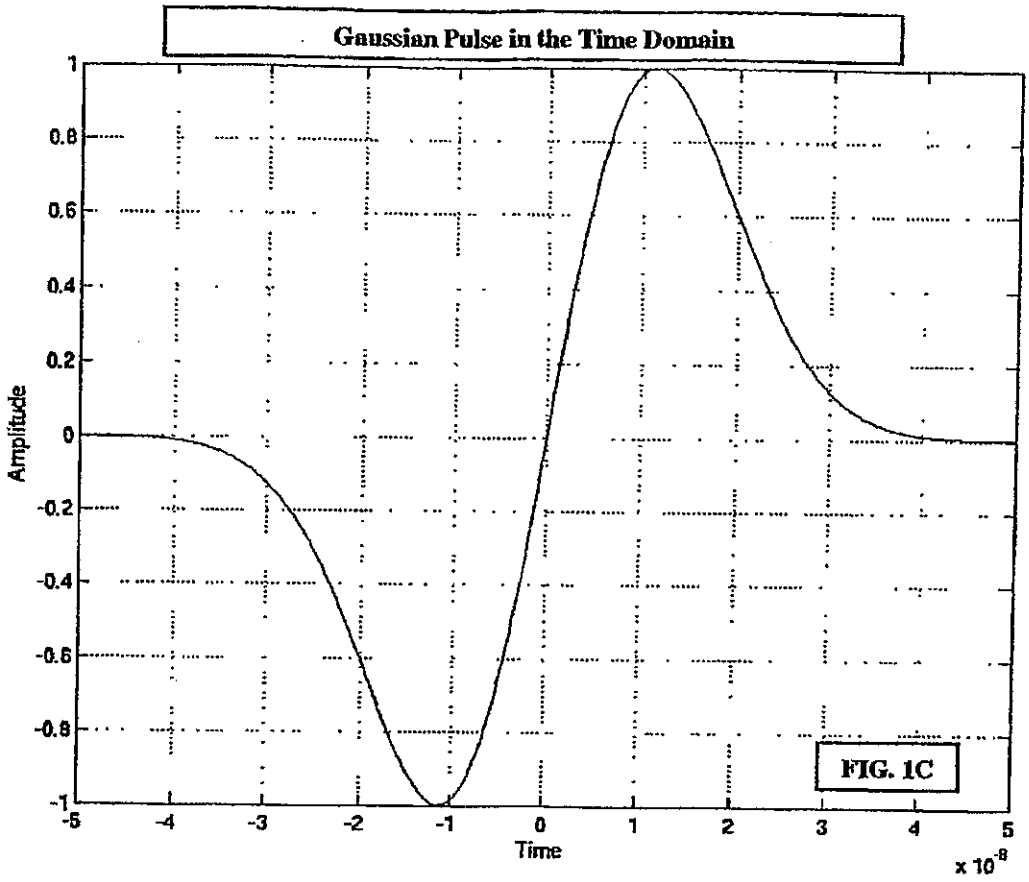

Gaussian Pulse in the Time Domain
Amplitude
Time
x 10^-8

FIG. 1C

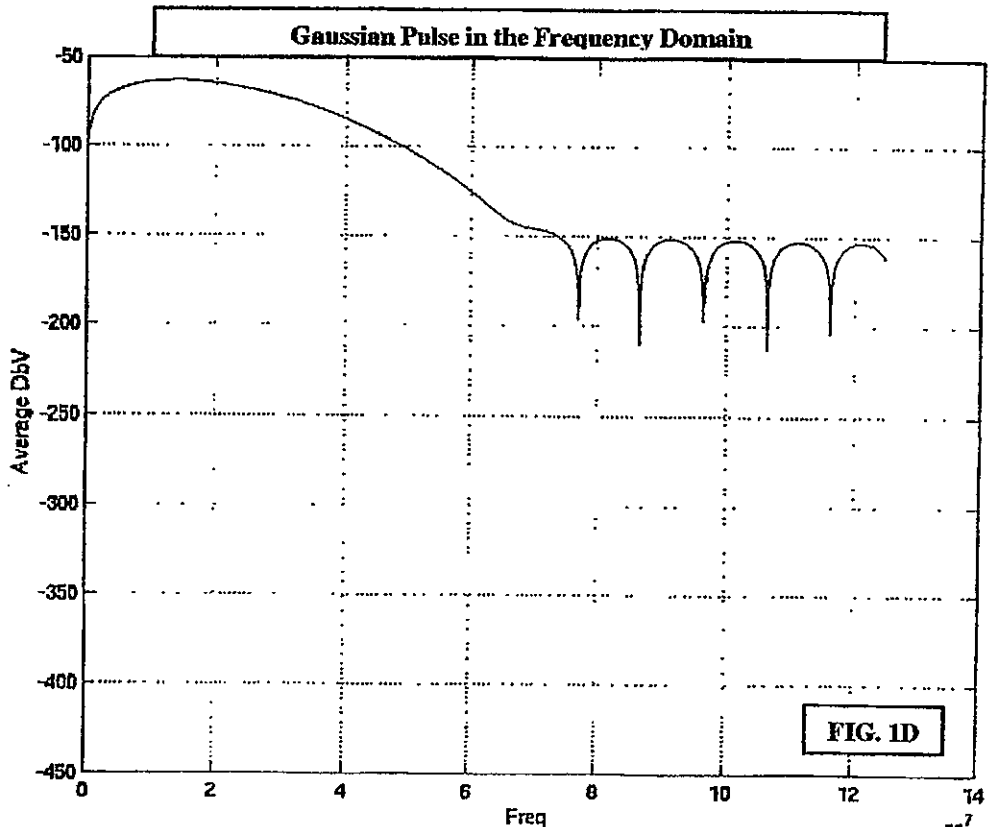

Gaussian Pulse in the Frequency Domain
Average DbV
Freq
x 10^7

FIG. 1D

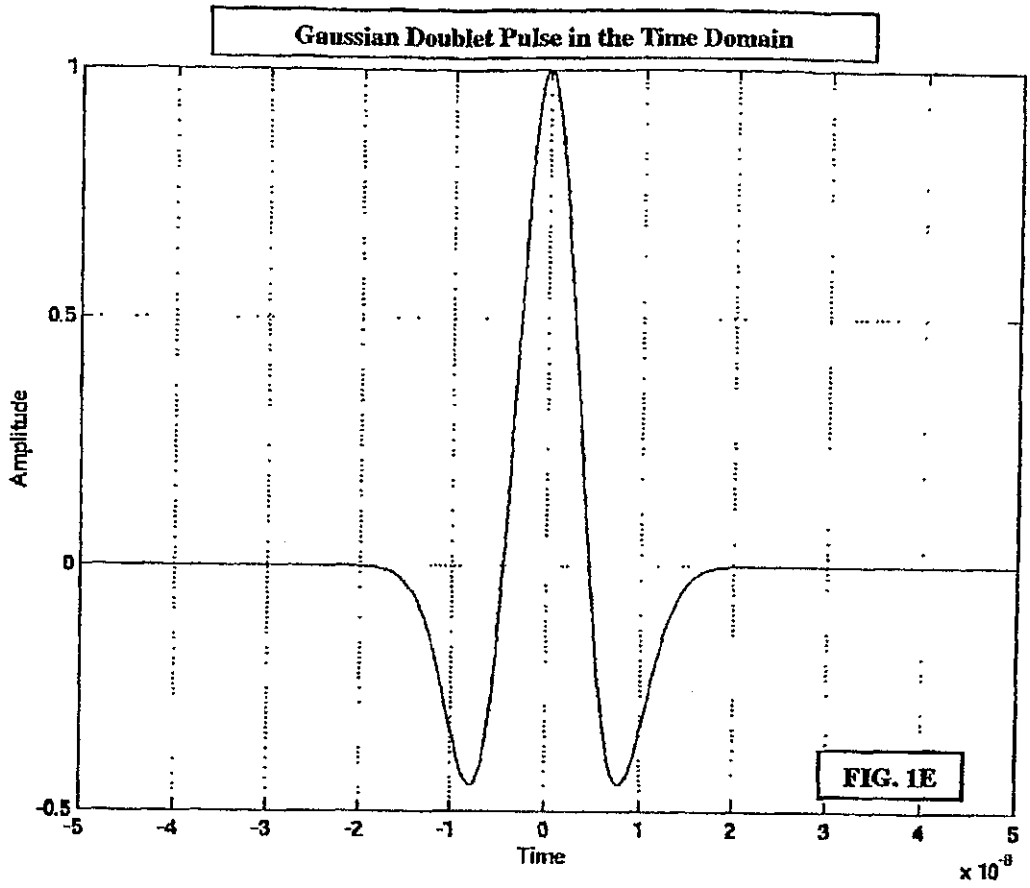

Gaussian Doublet Pulse in the Time Domain
Amplitude
Time
x 10^-8

FIG. 1E

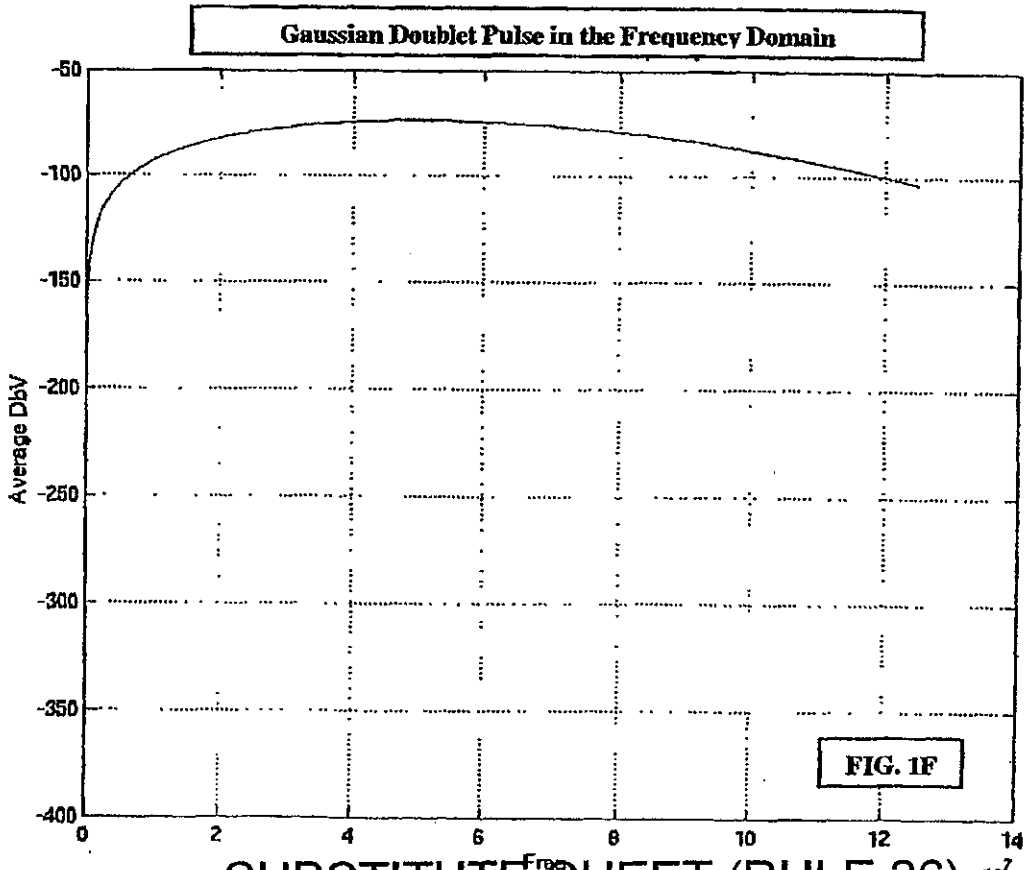

Gaussian Doublet Pulse in the Frequency Domain
Average DbV
Freq
x 10^7

FIG. 1F

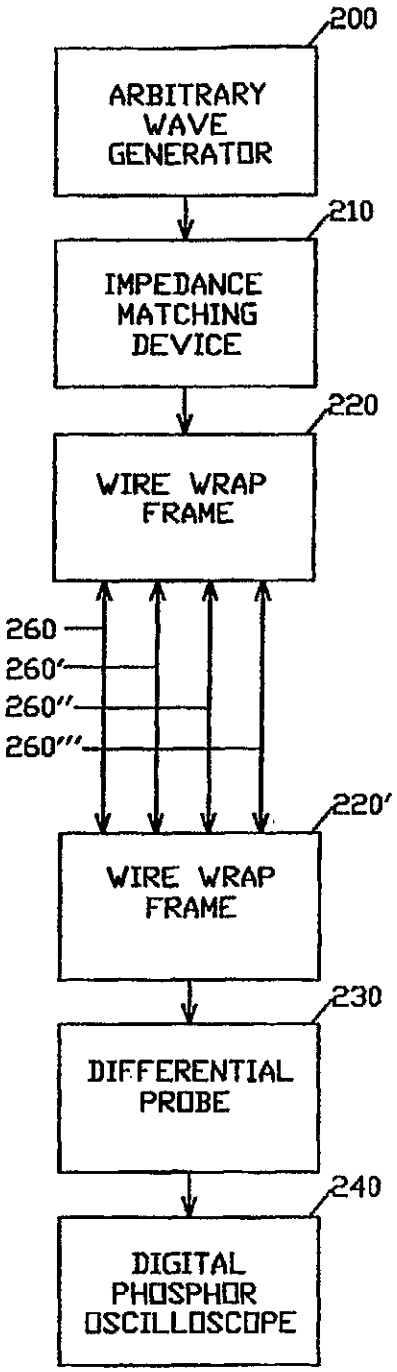

200
ARBITRARY WAVE GENERATOR
210
IMPEDANCE MATCHING DEVICE
220
WIRE WRAP FRAME
260
260'
260''
260'''
220'
WIRE WRAP FRAME
230
DIFFERENTIAL PROBE
240
DIGITAL PHOSPHOR OSCILLOSCOPE

FIG. 2A

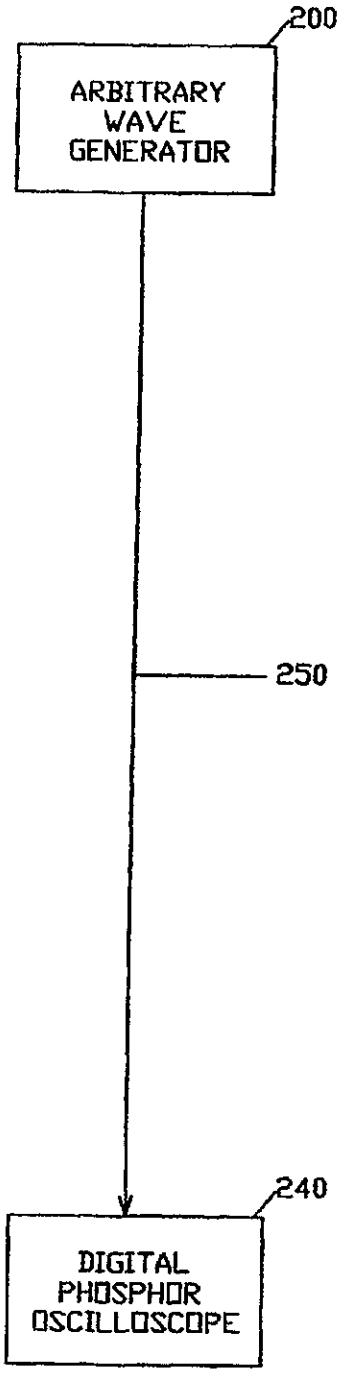

200
ARBITRARY WAVE GENERATOR
250
240
DIGITAL PHOSPHOR OSCILLOSCOPE

FIG. 2B

FIG. 3

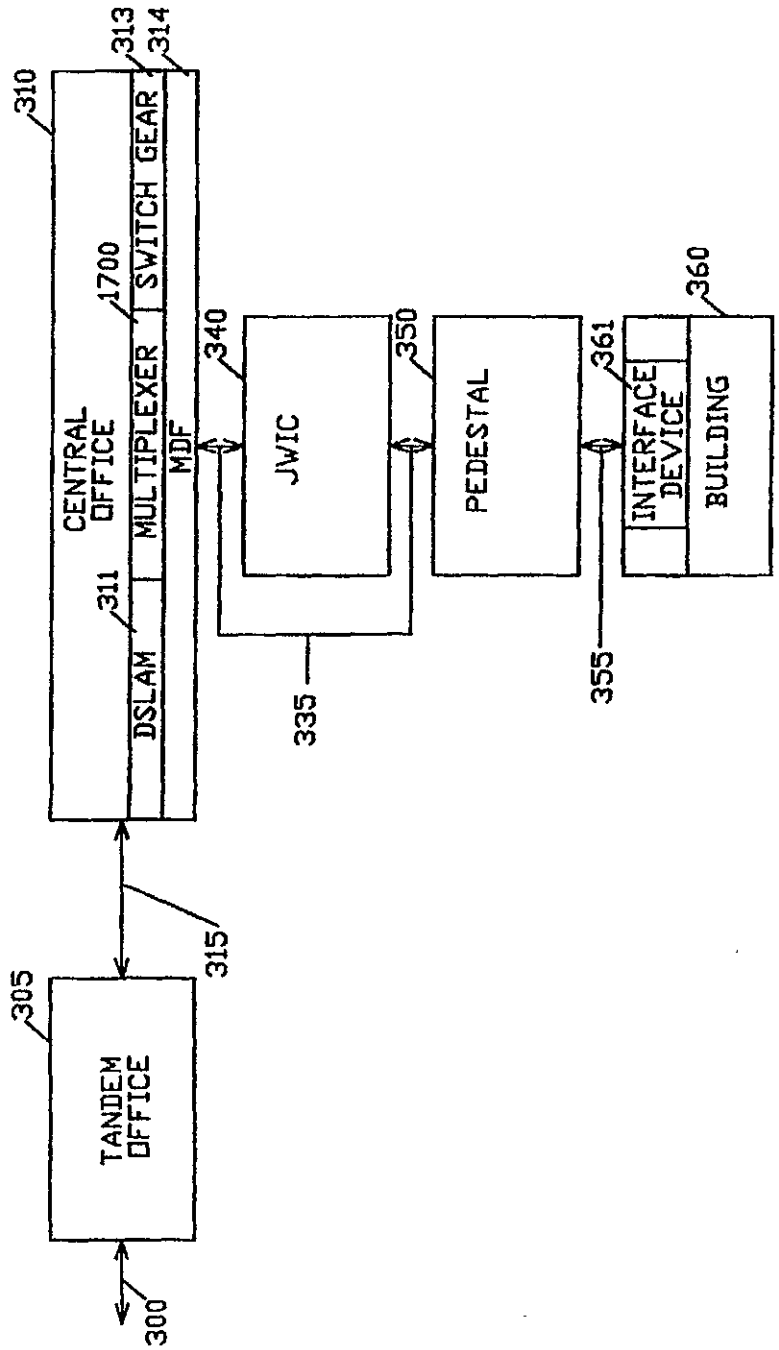
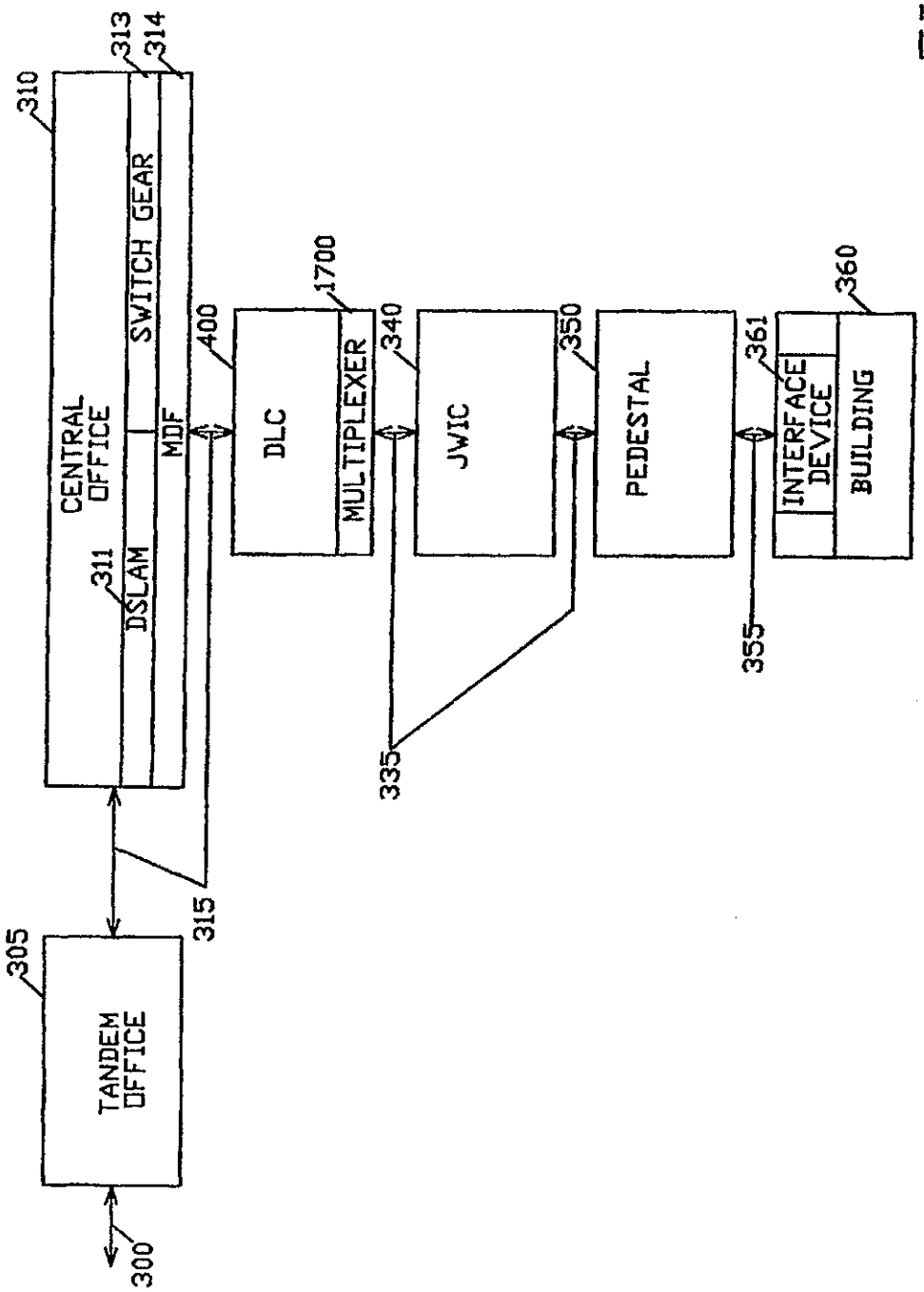

310
313
314
CENTRAL OFFICE
1700
SWITCH GEAR
MULTIPLEXER
MDF
311
DSLAM
340
JWIC
350
PEDESTAL
360
361
INTERFACE DEVICE
BUILDING
335
355
315
305
TANDEM OFFICE
300

FIG. 4


310
313
314
CENTRAL OFFICE
SWITCH GEAR
MDF
311
DSLAM
400
DLC
1700
MULTIPLEXER
340
JWIC
350
PEDESTAL
361
INTERFACE DEVICE
360
BUILDING
355
335
315
305
TANDEM OFFICE
300

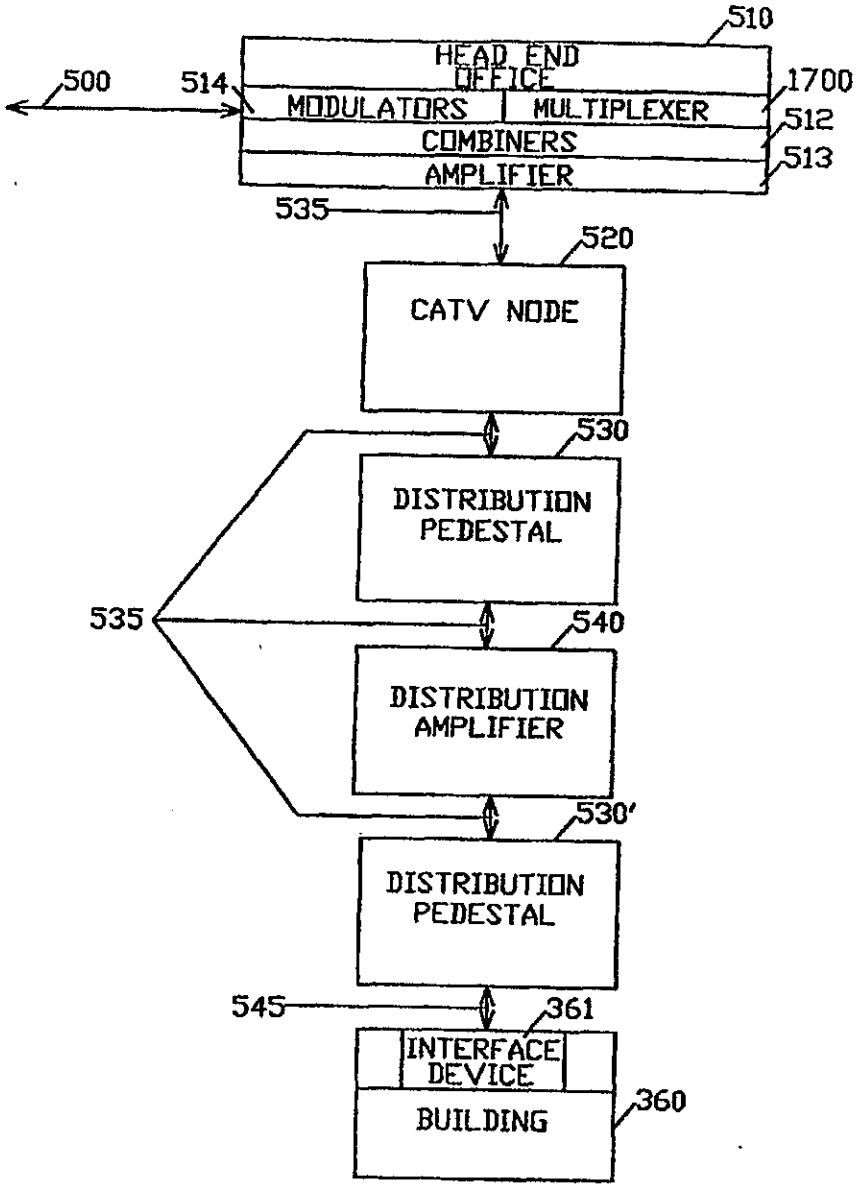
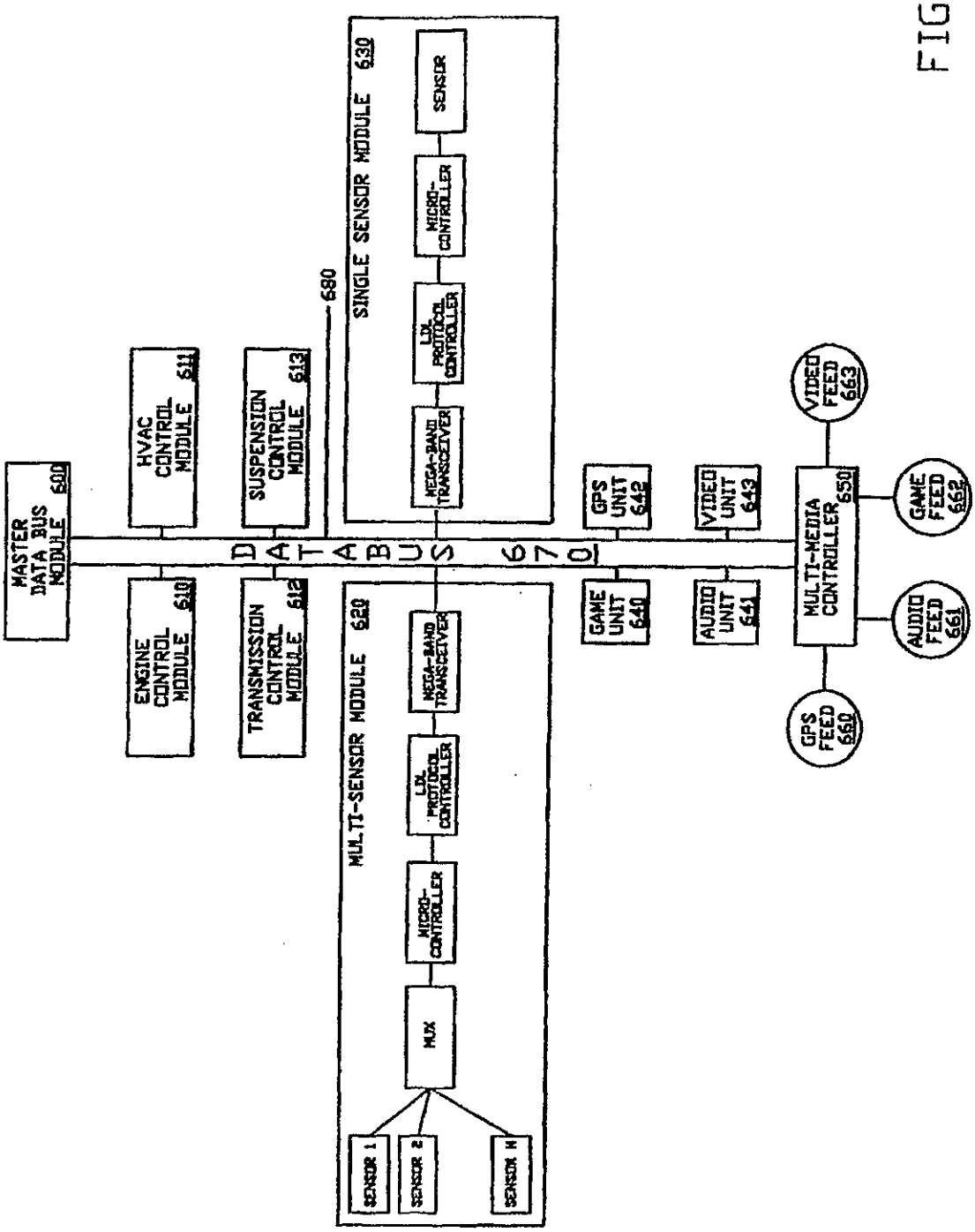

510
HEAD END OFFICE
500
514
MODULATORS
MULTIPLEXER
1700
512
COMBINERS
513
AMPLIFIER
535
520
CATV NODE
530
DISTRIBUTION PEDESTAL
535
540
DISTRIBUTION AMPLIFIER
530'
DISTRIBUTION PEDESTAL
545
361
INTERFACE DEVICE
BUILDING
360

FIG. 5

FIG. 6


MASTER DATA BUS MODULE 600
HVAC CONTROL MODULE 611
SUSPENSION CONTROL MODULE 613
680
SINGLE SENSOR MODULE 630
SENSOR
MICRO-CONTROLLER
LIN PROTOCOL CONTROLLER
MEGA-BAND TRANSCEIVER
VIDEO FEED 663
GPS UNIT 642
VIDEO UNIT 643
MULTI-MEDIA CONTROLLER 650
GAME FEED 662
AUDIO FEED 661
GPS FEED 660
DATA BUS 670
ENGINE CONTROL MODULE 610
TRANSMISSION CONTROL MODULE 612
MULTI-SENSOR MODULE 620
MEGA-BAND TRANSCEIVER
LIN PROTOCOL CONTROLLER
MICRO-CONTROLLER
MUX
SENSOR 1
SENSOR 2
SENSOR N
GAME UNIT 640
AUDIO UNIT 641

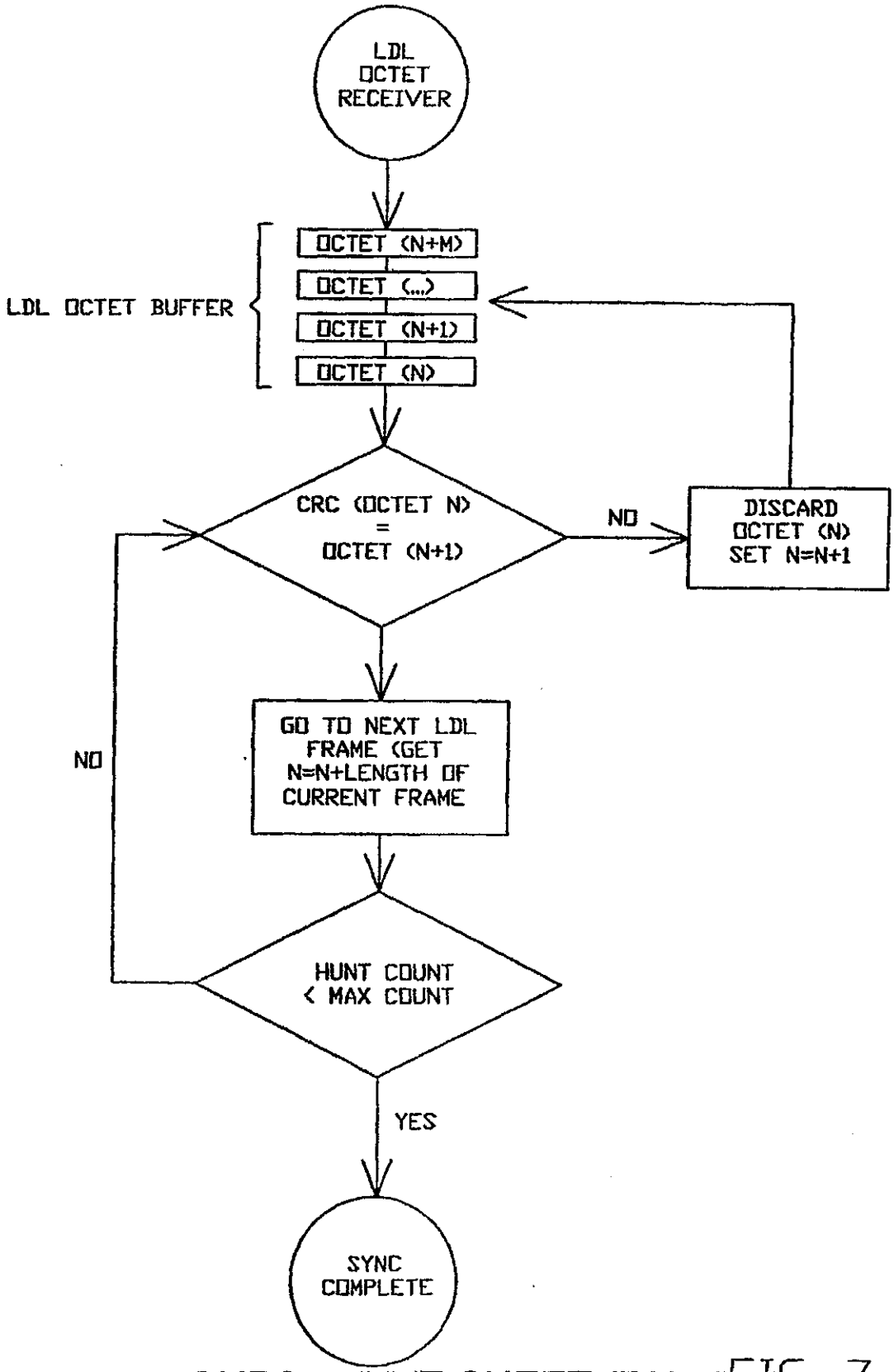

LDL OCTET RECEIVER
LDL OCTET BUFFER
OCTET (N+M)
OCTET (...)
OCTET (N+1)
OCTET (N)
CRC (OCTET N) = OCTET (N+1)
NO
DISCARD OCTET (N) SET N=N+1
NO
GO TO NEXT LDL FRAME (GET N=N+LENGTH OF CURRENT FRAME
HUNT COUNT < MAX COUNT
YES
SYNC COMPLETE

FIG. 7

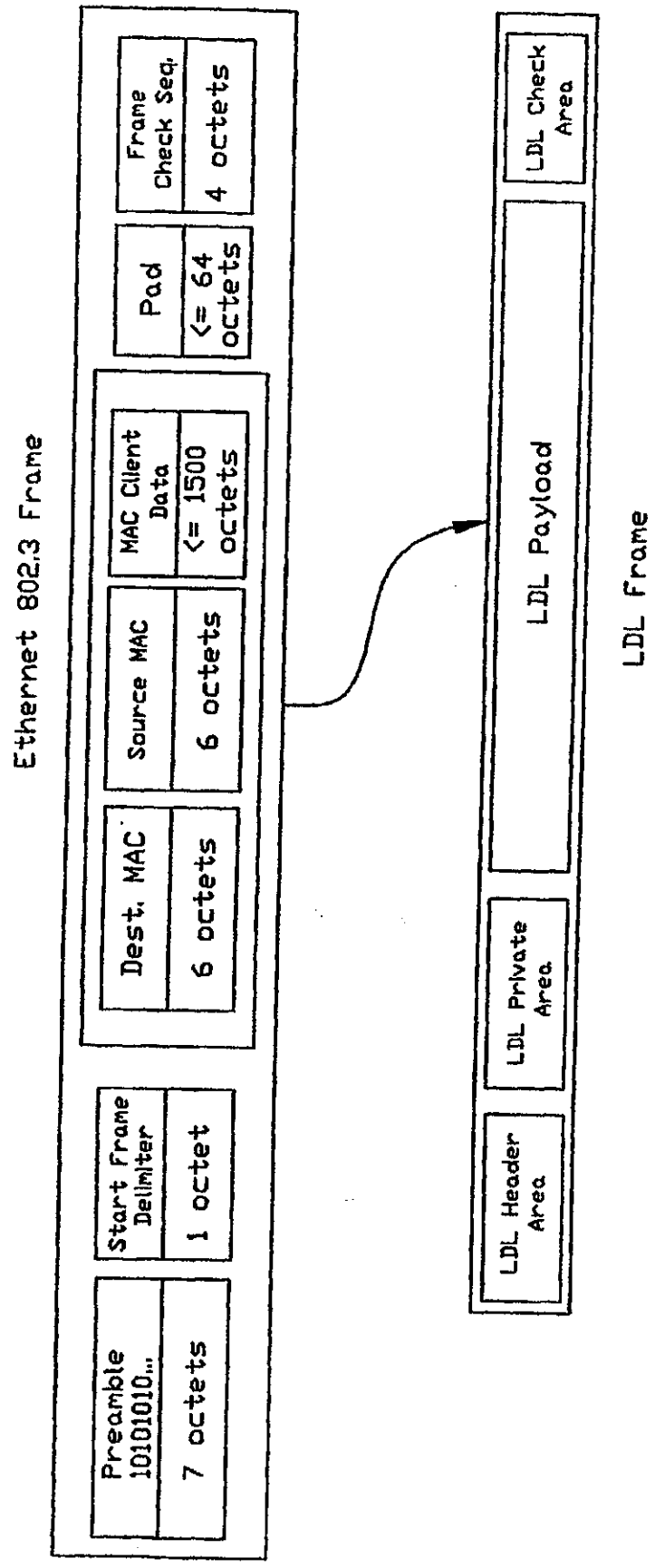

Ethernet 802.3 Frame
Preamble 10101010...
7 octets
Start Frame Delimiter
1 octet
Dest. MAC
6 octets
Source MAC
6 octets
MAC Client Data
<= 1500 octets
Pad
<= 64 octets
Frame Check Seq.
4 octets
LDL Frame
LDL Header Area
LDL Private Area
LDL Payload
LDL Check Area

FIG. 8

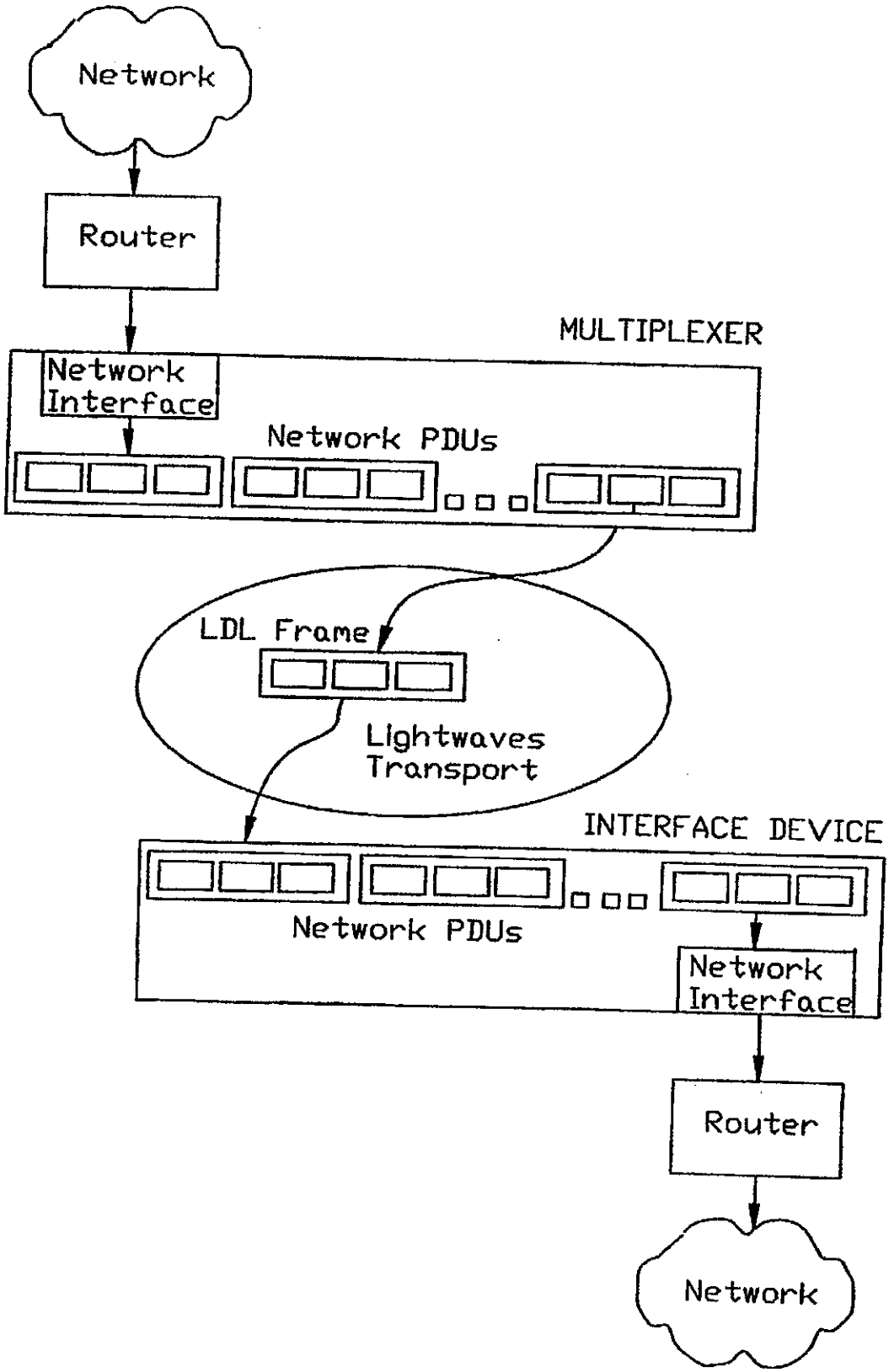

Network
Router
MULTIPLEXER
Network Interface
Network PDUs
LDL Frame
Lightwaves Transport
INTERFACE DEVICE
Network PDUs
Network Interface
Router
Network

FIG. 9

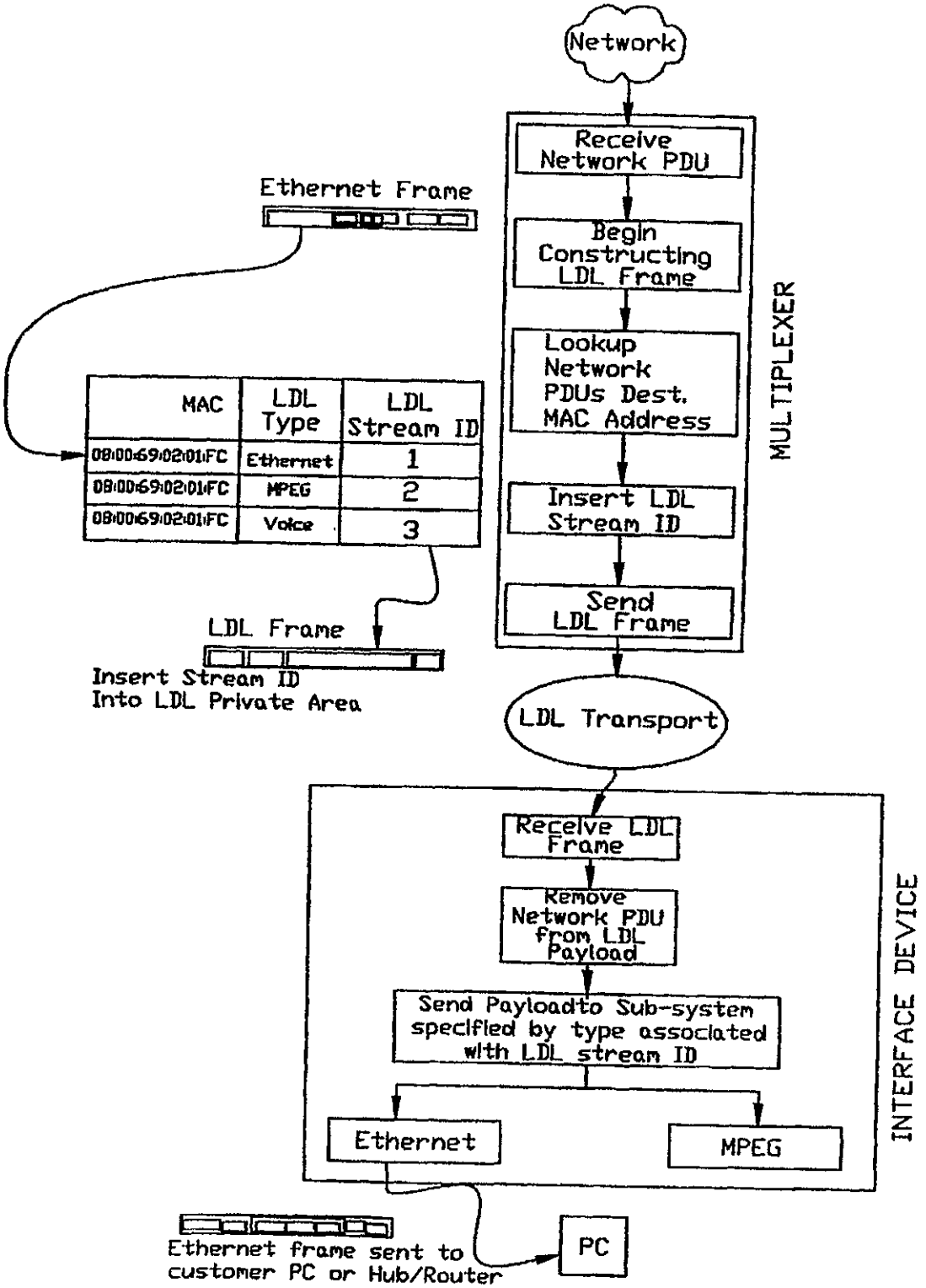

Network
Receive Network PDU
Begin Constructing LDL Frame
Lookup Network PDUs Dest. MAC Address
Insert LDL Stream ID
Send LDL Frame
MULTIPLEXER
Ethernet Frame
MAC
LDL Type
LDL Stream ID
08:00:69:02:01:FC
Ethernet
1
08:00:69:02:01:FC
MPEG
2
08:00:69:02:01:FC
Voice
3
LDL Frame
Insert Stream ID Into LDL Private Area
LDL Transport
Receive LDL Frame
Remove Network PDU from LDL Payload
Send Payloadto Sub-system specified by type associated with LDL stream ID
Ethernet
MPEG
INTERFACE DEVICE
Ethernet frame sent to customer PC or Hub/Router
PC

FIG. 10

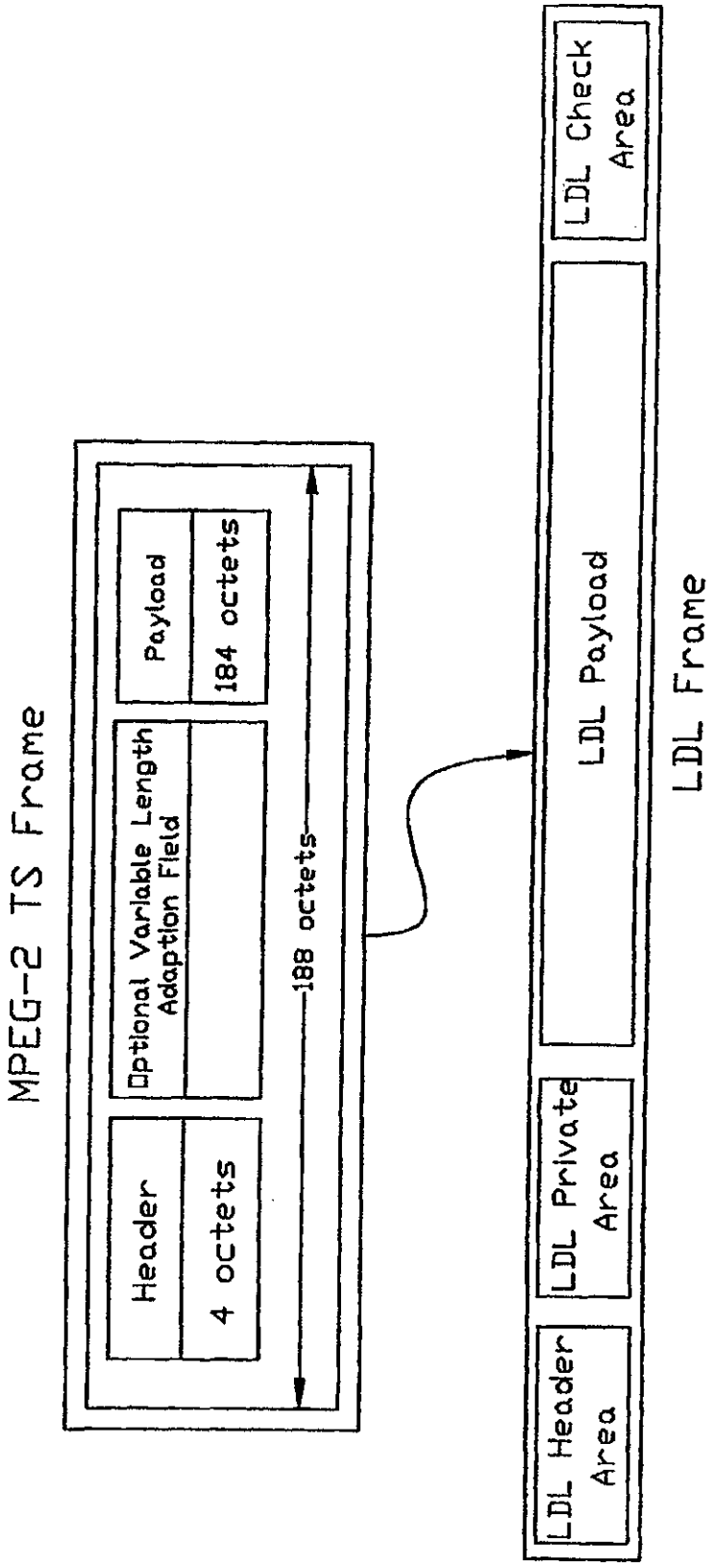

MPEG-2 TS Frame
Header
4 octets
Optional Variable Length Adaption Field
Payload
184 octets
188 octets
LDL Frame
LDL Header Area
LDL Private Area
LDL Payload
LDL Check Area

FIG. 11

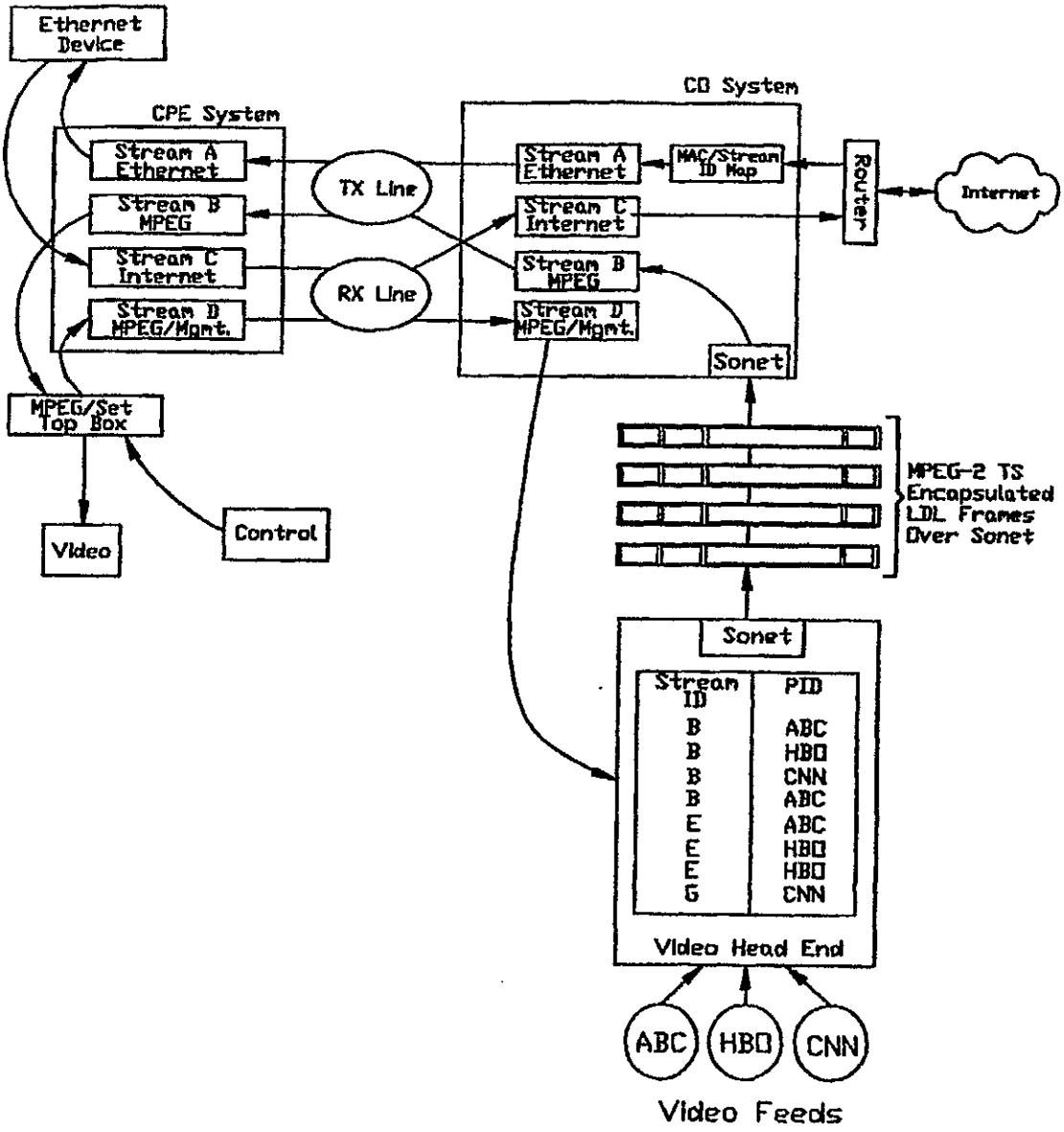

Ethernet Device
CPE System
Stream A Ethernet
Stream B MPEG
Stream C Internet
Stream D MPEG/Mgmt.
TX Line
RX Line
CO System
Stream A Ethernet
MAC/Stream ID Map
Router
Internet
Stream C Internet
Stream B MPEG
Stream D MPEG/Mgmt.
Sonet
MPEG/Set Top Box
Video
Control
MPEG-2 TS Encapsulated LDL Frames Over Sonet
Sonet
Stream ID
PID
B ABC
B HBO
B CNN
B ABC
E ABC
E HBO
E HBO
G CNN
Video Head End
ABC
HBO
CNN
Video Feeds

FIG. 12

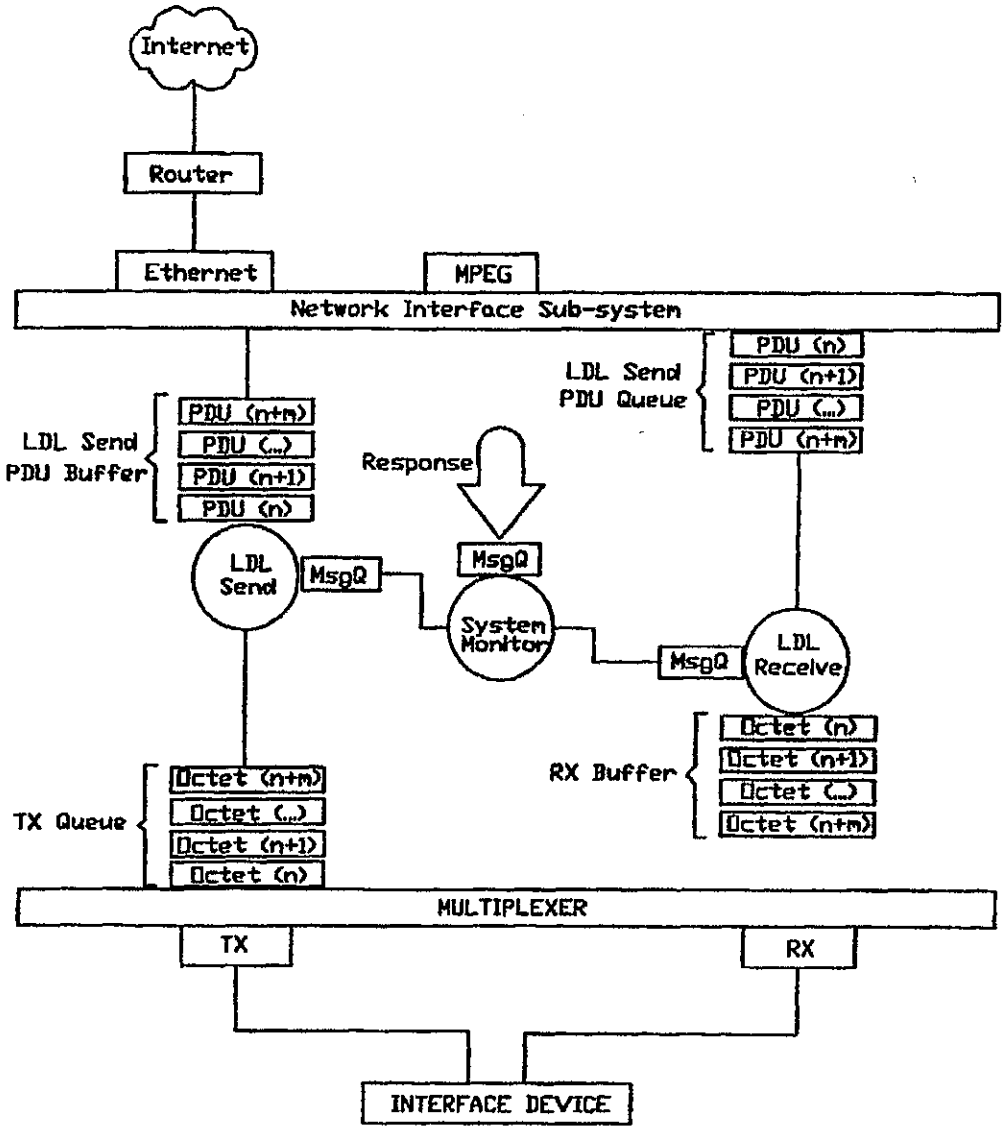

Internet
Router
Ethernet
MPEG
Network Interface Sub-system
LDL Send PDU Queue
PDU (n)
PDU (n+1)
PDU (...)
PDU (n+m)
LDL Send PDU Buffer
PDU (n+m)
PDU (...)
PDU (n+1)
PDU (n)
Response
LDL Send
MsgQ
MsgQ
System Monitor
MsgQ
LDL Receive
RX Buffer
Octet (n)
Octet (n+1)
Octet (...)
Octet (n+m)
TX Queue
Octet (n+m)
Octet (...)
Octet (n+1)
Octet (n)
MULTIPLEXER
TX
RX
INTERFACE DEVICE

FIG. 13

FIG. 14

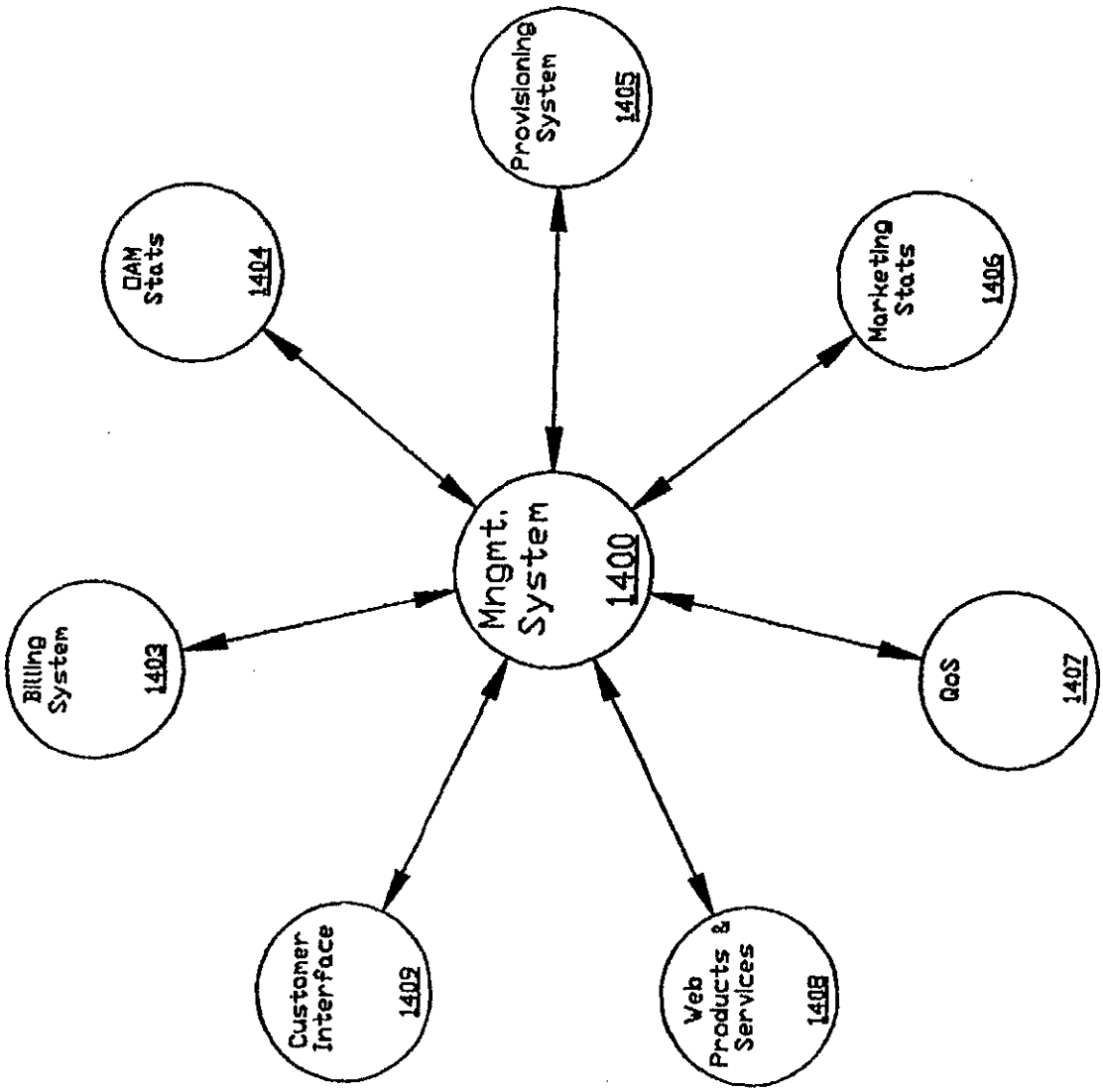
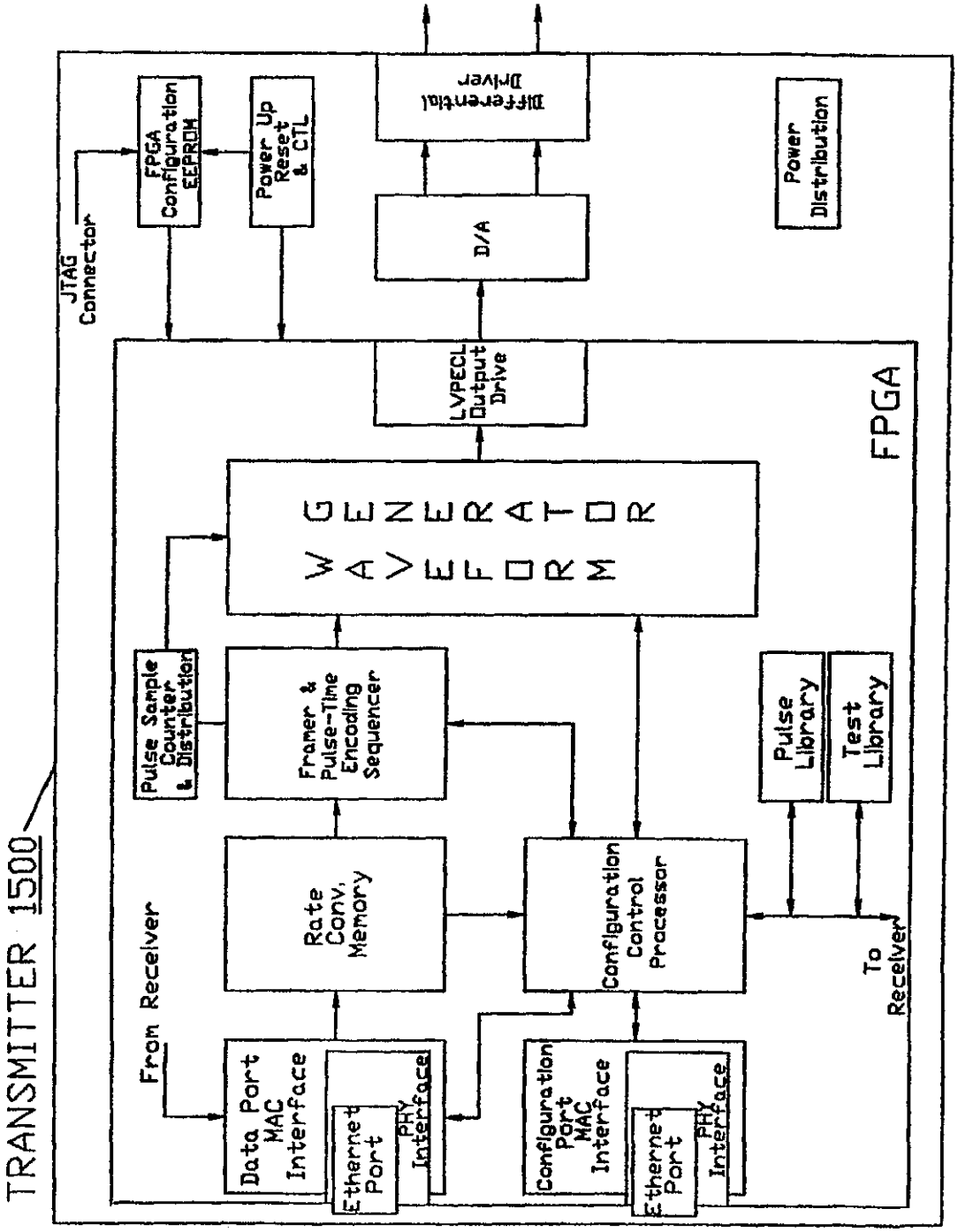

Provisioning System 1405
OAM Stats 1404
Marketing Stats 1406
Mngmt. System 1400
Billing System 1403
QoS 1407
Customer Interface 1409
Web Products & Services 1408

FIG. 15


TRANSMITTER 1500
FPGA
JTAG Connector
FPGA Configuration EEPROM
Power Up Reset & CTL
Differential Driver
D/A
Power Distribution
LVPECL Output Drive
WAVEFORM GENERATOR
Pulse Sample Counter & Distribution
Framer & Pulse-Time Encoding Sequencer
Pulse Library
Test Library
Rate Conv. Memory
Configuration Control Processor
From Receiver
To Receiver
Data Port MAC Interface
Ethernet Port
PHY Interface
Configuration Port MAC Interface
Ethernet Port
PHY Interface

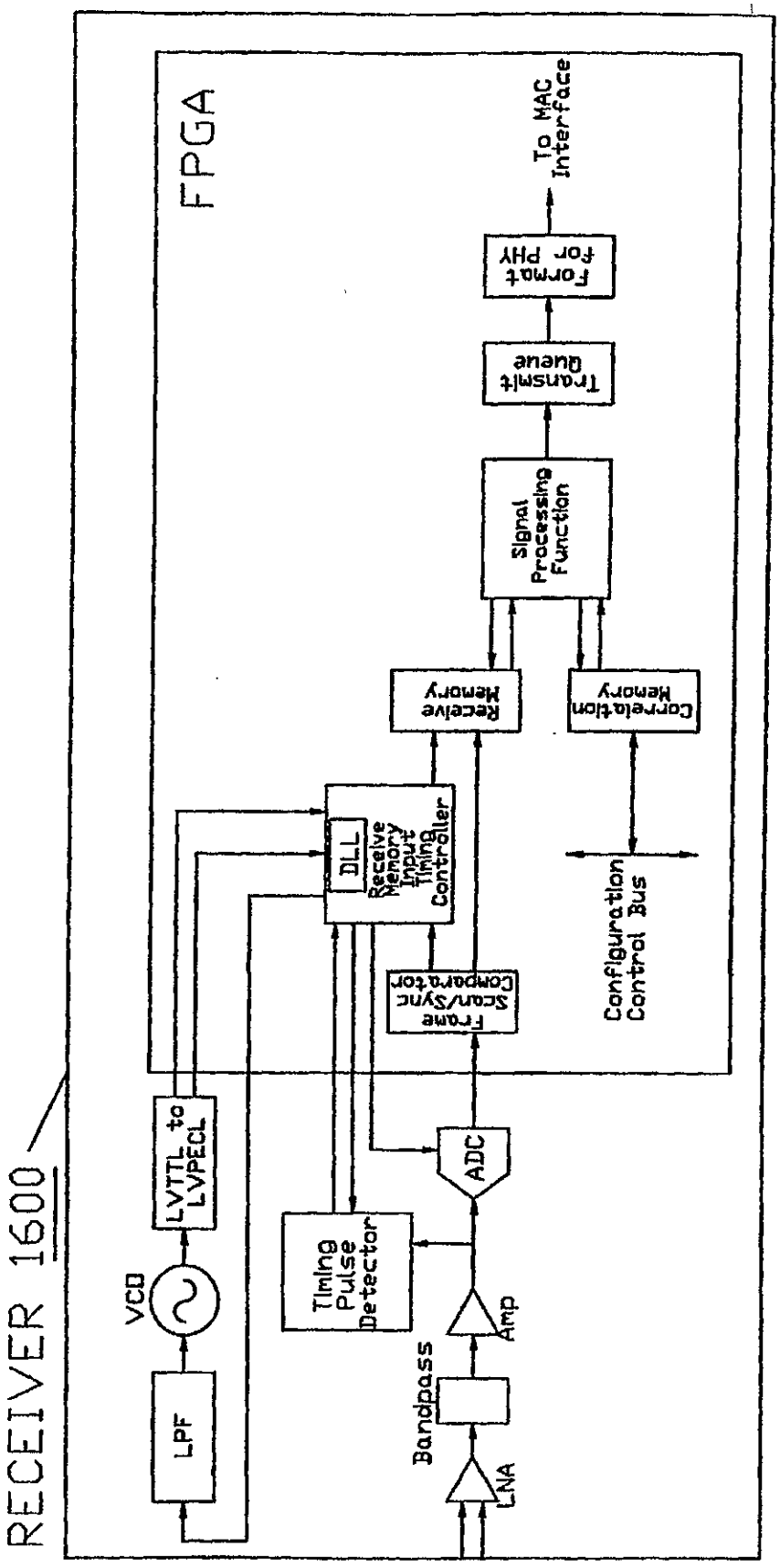

RECEIVER 1600
FPGA
To MAC Interface
Format for PHY
Transmit Queue
Signal Processing Function
Receive Memory
Correlation Memory
DLL
Receive Memory Input Timing Controller
Frame Scan/Sync Comparator
Configuration Control Bus
LVTTL to LVPECL
VCO
LPF
ADC
Timing Pulse Detector
Amp
Bandpass
LNA

FIG. 16

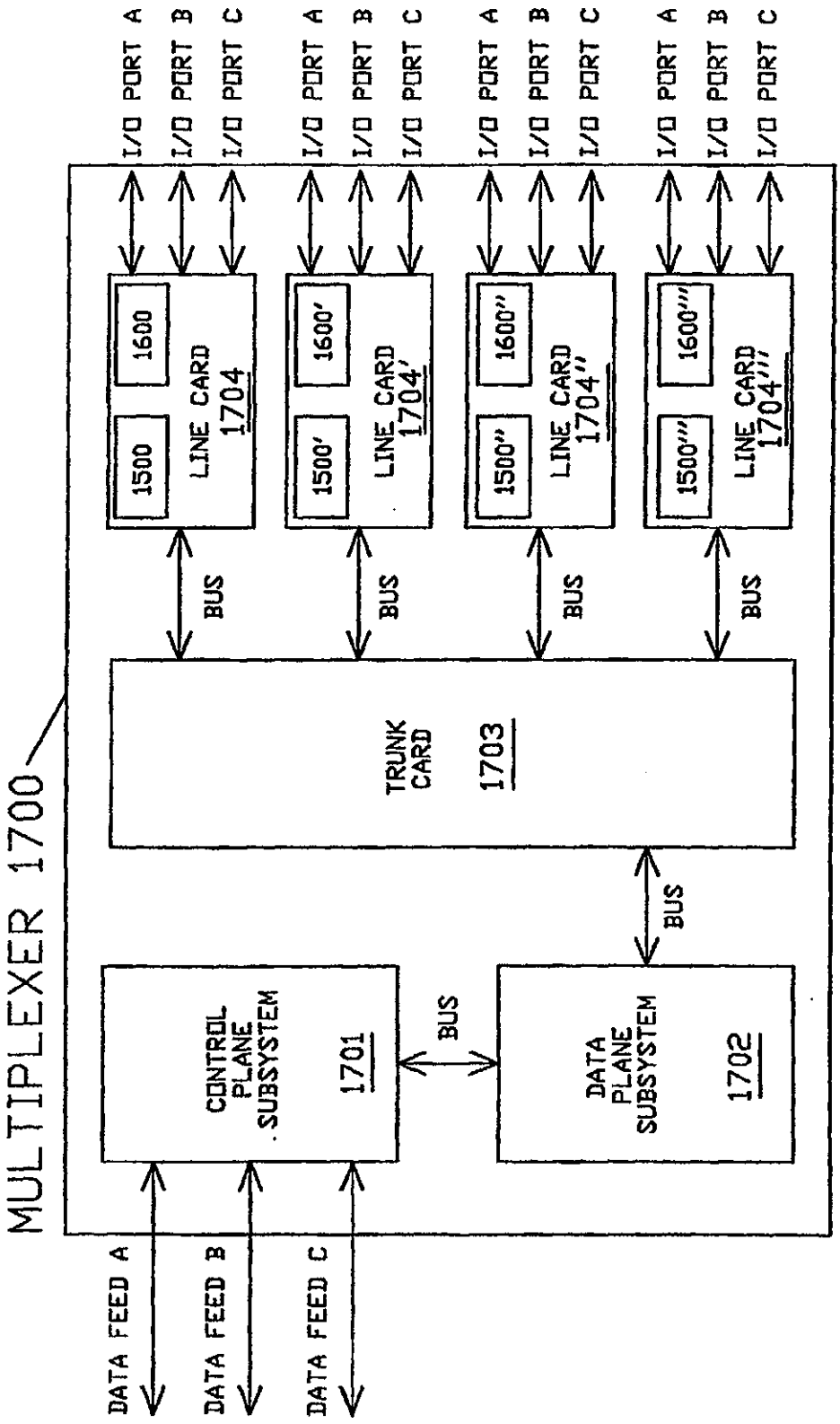

MULTIPLEXER 1700
I/O PORT A
I/O PORT B
I/O PORT C
1600
1500
LINE CARD 1704
1600'
1500'
LINE CARD 1704'
1600''
1500''
LINE CARD 1704''
1600'''
1500'''
LINE CARD 1704'''
BUS
TRUNK CARD 1703
CONTROL PLANE SUBSYSTEM 1701
DATA PLANE SUBSYSTEM 1702
DATA FEED A
DATA FEED B
DATA FEED C

FIG. 17

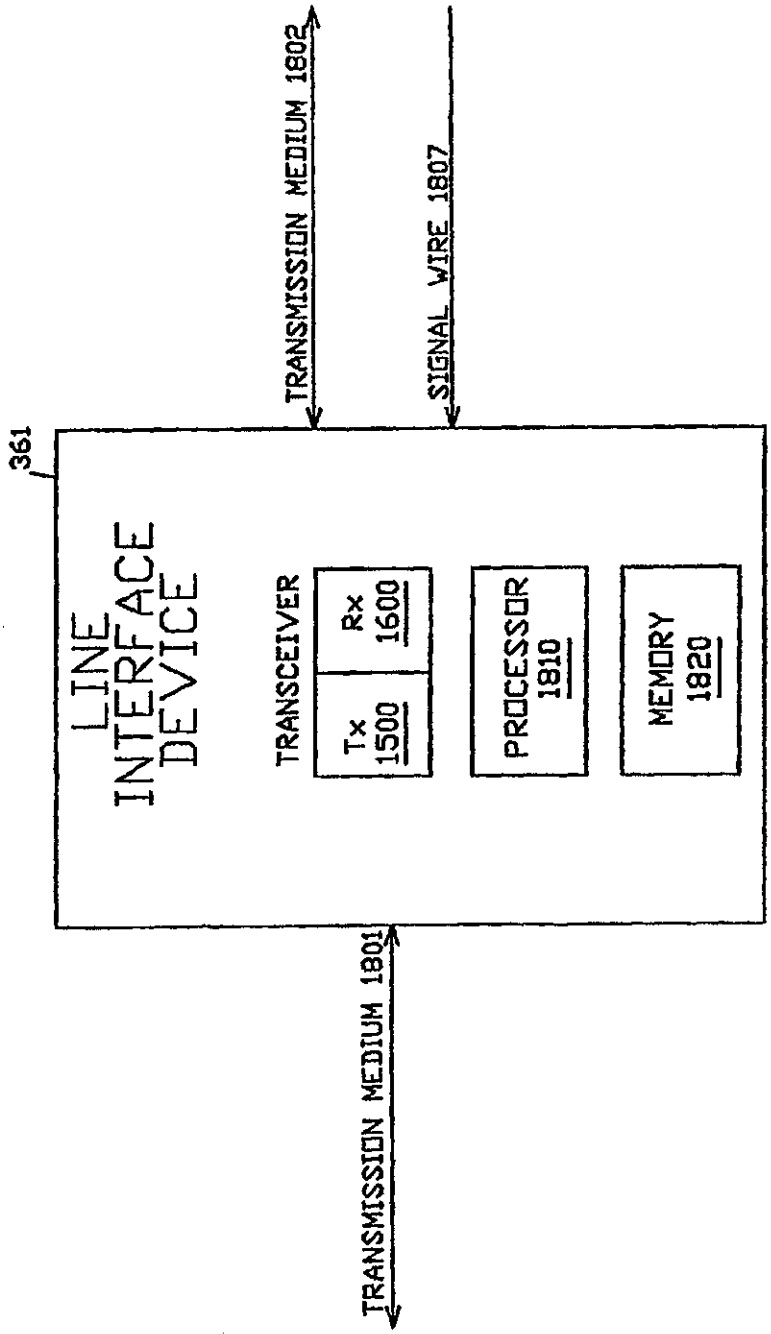

361
LINE INTERFACE DEVICE
TRANSCEIVER
Tx 1500
Rx 1600
PROCESSOR 1810
MEMORY 1820
TRANSMISSION MEDIUM 1802
SIGNAL WIRE 1807
TRANSMISSION MEDIUM 1801

FIG. 18